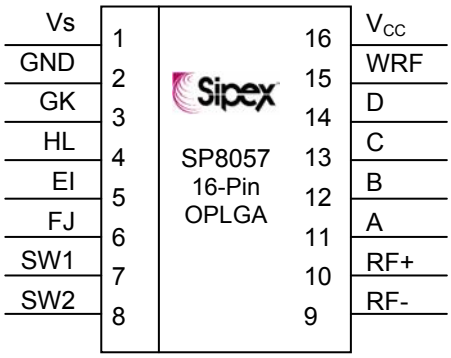
High Speed 11-channel Photo Detector IC

FEATURES

- Dual wavelength 650 and 780nm
- Data channel bandwidth 150 MHz
- Selectable gain settings
- Group delay error 1ns up to 86MHz
- 250V/μs Slew rate
- Small 16-pin OPLGA package



APPLICATION

- DVD-RAM with CD-RW capability
- DVD+/-RW with CD-RW capability
- Writable data storage optical devices

GENERAL DESCRIPTION

The SP8057 is an eleven-channel photo detector IC (PDIC) specially designed for high speed DVD-RAM and DVD+/-RW applications and can operate at wavelengths of 650 and 780 nm. The device contains three photo diode (sensor) arrays, with each having four sensors (A – D, E – H, and I – L respectively). The eleven channels consist of four high speed channels (A, B, C, and D), four slow channels (EI, FJ, GK, and HL), two fast channels with paraphase output (RF+ and RF-), and one additional WRF channel. The four slow channels output is the sum of signals from two sensors of the same sensor array (E + I, F + J, G + K, and H + L). The WRF channels output is four times the sum of A + B + C + D channels, while the output signal of paraphase channels RF+ and RF- is only 0.5 of this sum. Low noise operation enables data recovery at very low signal levels.

The SP8057 has two logic inputs for gain control that operate as three-state logic input (Low, Mid, and High states). These states are used to select gain factors that affect all channels.

The SP8057 is manufactured with an advanced 10GHz BICMOS technology.

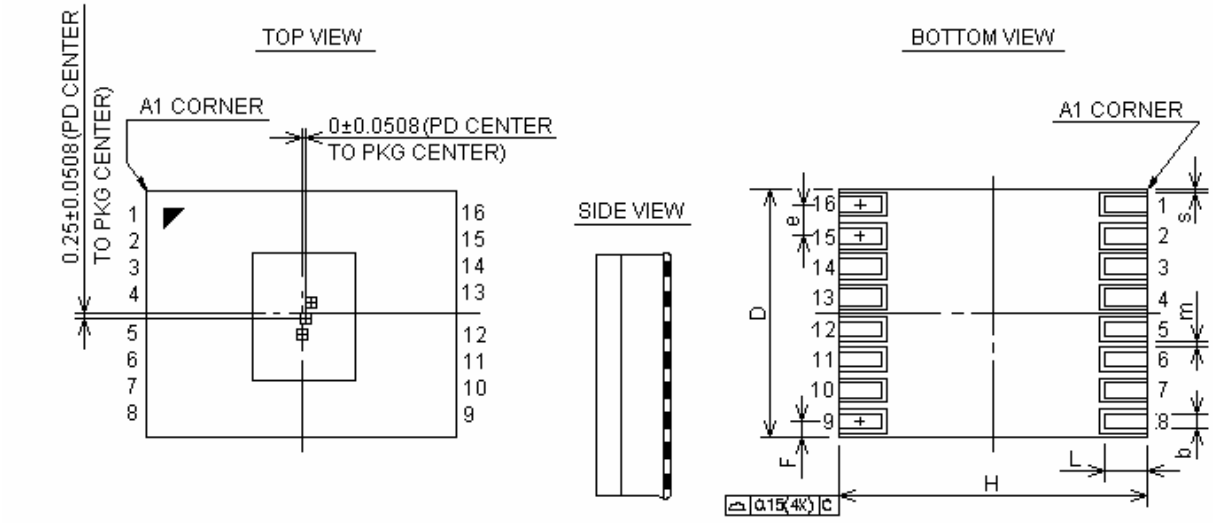
PIN ASSIGNMENTS

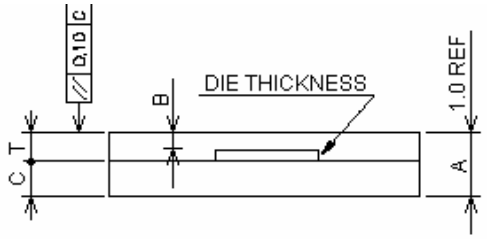
Pin #	Pin Name	Pin Function
1	Vs	Reference voltage. Bypass to GND with ceramic capacitor 0.1uF
2	GND	Ground pin
3	GK	Output of GK channel (sum of G + K sensor signals)
4	HL	Output of HL channel (sum of H + L sensor signals)
5	EI	Output of EI channel (sum of E + I sensor signals)
6	FJ	Output of FJ channel (sum of F + J sensor signals)
7	SW1	Logic input of Gain Controller. Allows three states – low, high, and middle - Z
8	SW2	Logic input of Gain Controller. Allows three states – low, high, and middle - Z
9	RF-	Output of RF- channel. RF- = - 0.5 x (A + B +C + D)
10	RF+	Output of RF+ channel. RF+ = 0.5 x (A + B + C + D)
11	A	Output of A channel
12	B	Output of B channel
13	C	Output of C channel
14	D	Output of D channel
15	WRF	Output of WRF channel. WRF = 4 x (A + B + C + D)
16	V_{CC}	Supply voltage. Bypass to GND with ceramic capacitor 0.1uF

BOARD LAYOUT AND GROUNDING

To obtain the best performance from the SP8057, a printed circuit board with ground plane is required. High quality, low series resistance ceramic 0.1uF bypass capacitors should be used at the Vcc and Vs pins (pins 1 and 16). These capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypassing capacitors must be kept short and should be made as wide as possible.

OPLGA 16 PACKAGE DIMENSIONS





NOTE: DIE THICKNESS 0.2 mm (8mil)

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.20	0.25	0.30
C	–	0.56	–
D	3.85	4.00	4.15
B	0.19		0.32
H	4.90	5.00	5.10
e	–	0.5	–
F	0.17	0.25	0.33
L	0.60	0.70	0.80
T	–	0.45	–
s	0.05	–	–
m	0.10	–	–

ORDERING INFORMATION

Part number	Temperature range	Package Type
SP8057DG	-30 + 80^{0}C	16-pin OPLGA