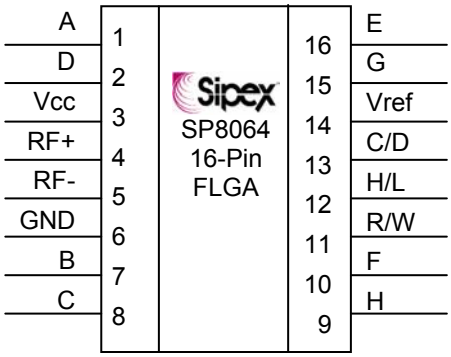
High Speed 10-channel Photo Detector IC

FEATURES

- Dual wavelength 650nm and 780nm
- Data channel bandwidth 120 MHz (-3dB)
- Nine selectable gain settings
- Group delay error less than 0.5ns up to 72MHz
- 6ns settling time
- 16-pin Molded FLGA package



APPLICATION

- x16 DVD +R Read and Write
- x12 DVD +RW Read and Write
- x4 DVD Dual layer write
- X48 CD Read
- X48 CD-R Write

GENERAL DESCRIPTION

The SP8064 is a ten-channel photo detector IC (PDIC) designed for DVD and CD applications operating at wavelengths of 650 and 780 nm. The device contains three photo diode (sensor) arrays, one of them with four identical sensors A – D and the other two with two sensors (E, F and G, H respectively). The ten channels consist of four high speed channels (A, B, C, and D), four slow channels (E, F, G, and H), and two RF channel with balanced differential outputs (RF+ and RF-). Channels A through D are high bandwidth data channels, while E through H are used to generate tracking information. The RF channels output the sum of A + B + C + D channels with identical weights given to all channels.

Three Gain select inputs (R/W, H/L, C/D) allow setting of eight gain modes and a Power Down mode with low power consumption if H/L and C/D inputs are left floating or driven to Hi-Z and low logic levels respectively.

The SP8064 is manufactured with an advanced 10GHz BICMOS technology.

GAIN MODE SELECTION

Gain Mode	R/W	H/L	C/D
Writing DVD+R	0	0	0
Writing CD-R (sample)	0	0	1
Writing CD-R (average)	0	Hi-Z	1
Writing DVD+RW	0	1	0
Writing CD-RW	0	1	1
Reading DVD-ROM	1	0	0
Reading CD-ROM	1	0/Hi-Z	1
Reading DVD+RW	1	1	0
Reading CD-RW	1	1	1
Power Down Mode*	X	Hi-Z	0

* If no logic inputs are applied to gain select pins, Power Down Mode is default mode.

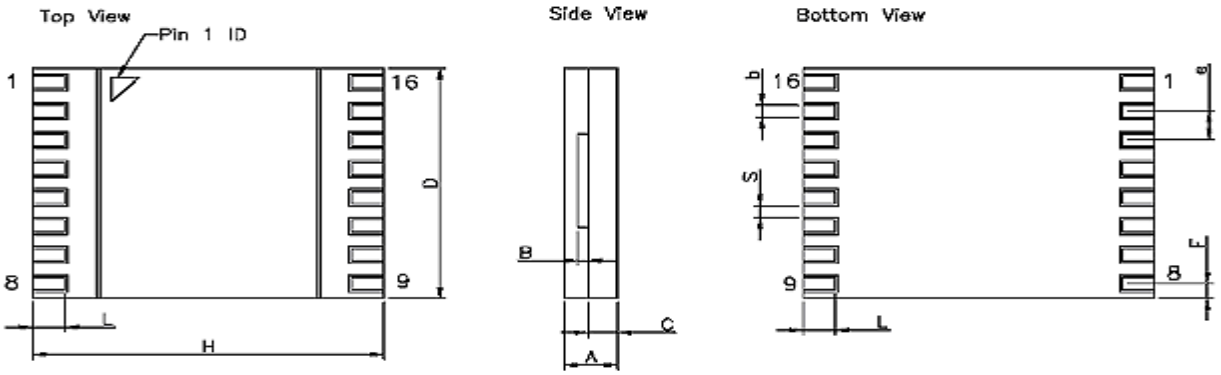
PIN ASSIGNMENTS

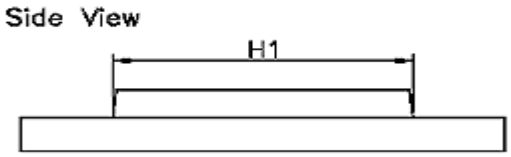
Land #	Pin Name	Pin Function
1	A	Output of A channel
2	D	Output of D channel
3	Vcc	Supply voltage. Bypass to GND with ceramic capacitor 0.1uF
4	RF+	Output of RF+ channel. RF+ = A + B + C + D
5	RF-	Output of RF- channel. RF- = - (A + B + C + D)
6	GND	Ground pin
7	B	Output of B channel
8	C	Output of C channel
9	H	Output of H channel
10	F	Output of F channel
11	R/W	Mode switch input.
12	H/L	Mode switch input.
13	C/D	Mode switch input.
14	Vref	Reference voltage. Bypass to GND with ceramic capacitor 0.1uF
15	G	Output of G channel
16	E	Output of E channel

BOARD LAYOUT AND GROUNDING

To obtain the best performance from the SP8064, a printed circuit board with ground plane is required. Ground pins (pin #6) should be connected to the ground plane. High quality, low series resistance ceramic 0.1uF bypass capacitors should be used at the Vcc and Vref pins (pins #3 and #14). These capacitors must be located as close to the pins as possible. A Vref decoupling capacitor to ground should be used. The traces connecting the pins to the ground plane, Vcc, Vref, and bypassing capacitors must be kept short and should be made as wide as possible.

Molded FLGA 16L PACKAGE DIMENSIONS

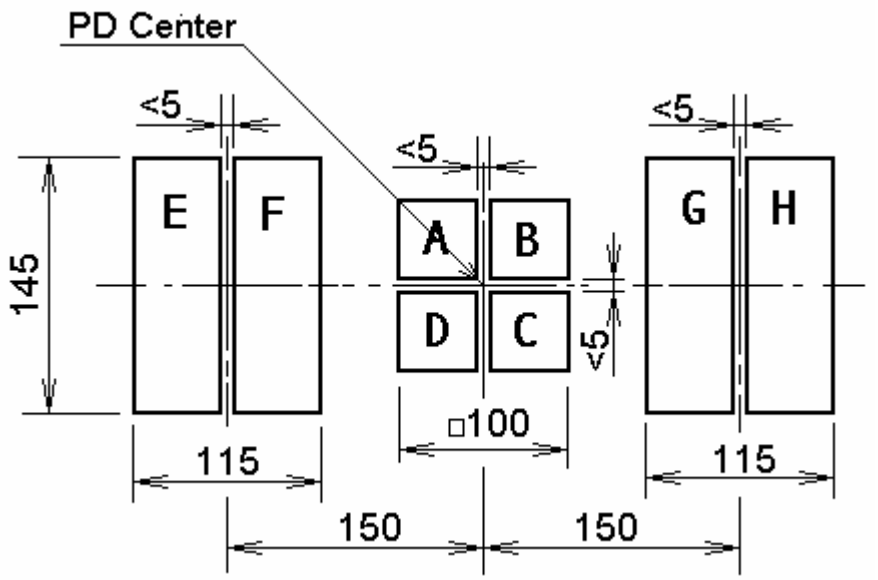




NOTE :
1. ALL DIMENSION ARE IN MILLIMETERS.
2. Die thickness : 0.20mm (8mil).

SYMBOLS	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.90	1.00	1.10
B	0.19	——	0.25
b	0.23	0.28	0.33
c	——	0.56	——
D	5.10	5.20	5.30
e	——	0.65	——
H	6.50	6.60	6.70
H1	4.10	4.20	4.30
L	0.50	0.60	0.70
F	0.245	0.325	0.405
S	0.20	——	——

PHOTO DETECTOR PATTERN



Note: 1. Detector size units: μm
2. Separation between segments < 5 μm

ORDERING INFORMATION

Part number	Temperature range	Package Type
SP8064CG1	0 + 70^{0}C	16-pin Molded Flexible Land Grid Array (FLGA)

