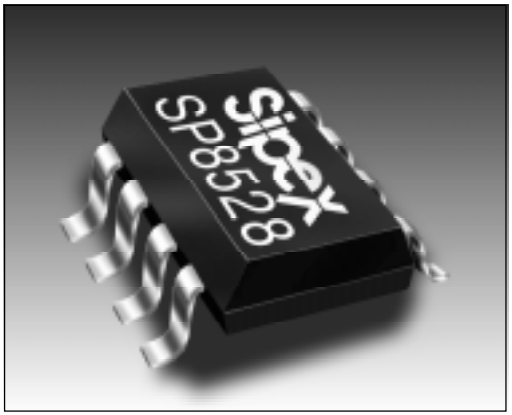
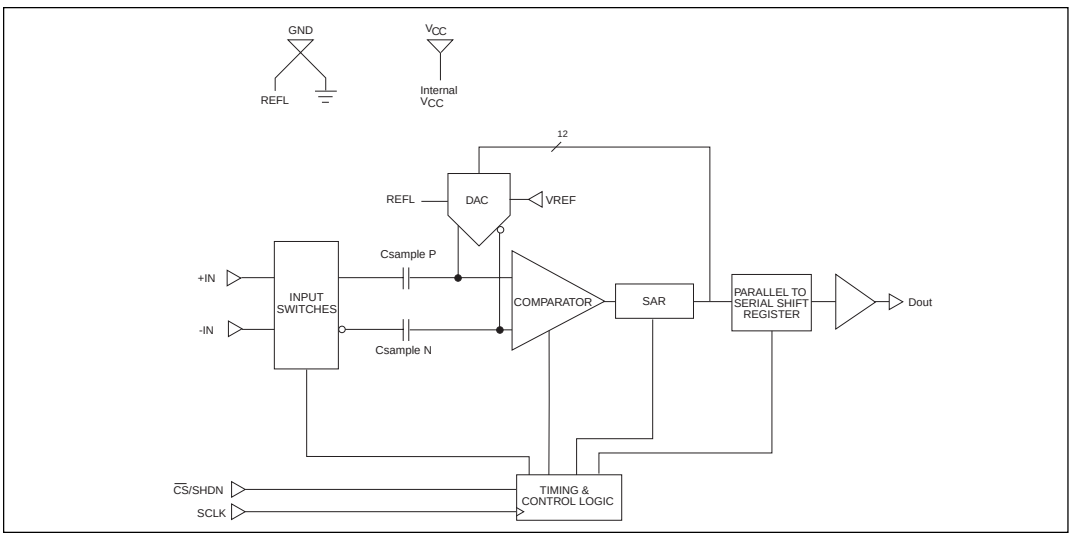
Micropower Sampling 12-Bit A/D Converter

- Low Cost
- 12-Bit Serial Sampling ADC
- Guaranteed ±1.0 LSB Max INL
- Guaranteed No Missing Codes
- 8-Pin NSOIC Plastic Package
- Low Power @ 230µA including Automatic Shutdown: 1nA (typ)
- Full differential input stage
- Single Supply 3.0V to 5.5V operation
- Half Duplex Digital Serial Interface
- Sample Rate: 30.12µS
- Pin Compatible Upgrade to LTC 1286



DESCRIPTION

The **SP8528** is a very low power 12-Bit A/D converter. The **SP8528** typically draws 230µA of supply current when sampling at 33.2 kHz. Supply current drops linearly as the sample rate is reduced. The ADC automatically powers down when not performing conversions, drawing only leakage current. The **SP8528** is available in 8-Pin NSOIC packages, specified over Commercial and Industrial temperature ranges. The **SP8528** is best suited for Battery-Operated Systems, Portable Data Acquisition Instrumentation, Battery Monitoring, and Remote Sensing applications. The serial port allows efficient data transfer to a wide range of microprocessors and microcontrollers over 3 wires.



SP8528 Block Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

(TA=+25˚C unless otherwise noted) .....
VCC to GND 7.0V
Vin to GND ..... -0.3 to VCC +0.3V
Digital input to GND ..... -0.3 to VCC +0.3V
Digital output to GND ..... -0.3 to VCC +0.3V
Operating Temperature Range
Commercial (J, K Version) ..... 0˚C to 70˚C
Industrial (A, B Version) ..... -40˚C to +85˚C
Lead Temperature (Solder 10Sec) ..... +300˚C
Storage Temperature ..... -65˚C to +150˚C
Power Dissipation to 70˚C 500mW

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

Unless otherwise noted the following specifications apply for VCC=5V or 3.3V with limits applicable for Tmin to Tmax. Typical applies for Ta=25˚C.

	VCC=5.0V			VCC=3.3V				
PARAMETERS	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
DC ACCURACY								
Resolution		12			12		Bits	
Integral Linearity								
J,A		±0.6	±2.0		±0.6	±2.0	LSB	
K,B		±0.6	±1.0		±0.6	±1.0	LSB	
Differential Linearity Error								
J,A		±0.75	±2.0		±0.75	±2.0	LSB	
K,B		±0.75	±1.0		±0.75	±1.0	LSB	No Missing Codes
Gain Error								
J,A		±2.0	±10		±2.0	±10	LSB	
K,B		±2.0	±8		±2.0	±8	LSB	
Offset Error								
J,A		±1.5	±5		±3.0	±8	LSB	
K,B		±1.5	±3		±3.0	±5	LSB	
ANALOG INPUT								
Input Signal FS Range	0		V_{ref}	0		V_{ref}		
Input Impedance								
On Channel		20			20		pF	In Parallel with 100MΩ
		100			100		MΩ	
Off Channel		3			3		pF	In Parallel with 100MΩ
		100			100		MΩ	
Input Bias Current		.001	1		.001	1	µA	
Analog Input Range	-.05		V_{CC}+.05	-.05		V_{CC}+.05	Volts	
CONVERSION SPEED								
Sample Time		1.5			1.5		clock cycles	See Timing Diagrams
Conversion Time		12			12		clock cycles	See Timing Diagrams
Complete Cycle			33.2			22.2	kHz	See Timing Diagrams
Clock Period	2.0			3.0			µS	See Timing Diagrams
Clock High Time	.9			1.4			µS	See Timing Diagrams
Clock Low Time	.9			1.4			µS	See Timing Diagrams

SPECIFICATIONS (cont.)

Unless otherwise noted the following specifications apply for VCC=5V or 3.3V with limits applicable for Tmin to Tmax. Typical applies for Ta=25°C.

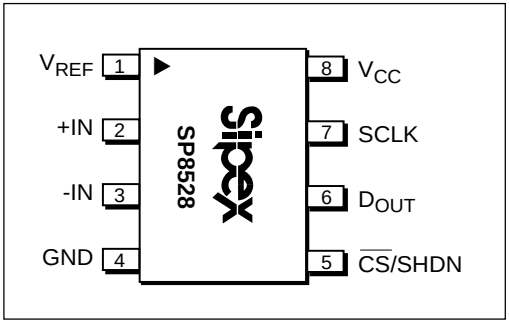
PARAMETERS	VCC=5.0V MIN.	TYP.	MAX.	VCC=3.3V MIN.	TYP.	MAX.	UNITS	CONDITIONS
DIGITAL INPUTS								
Input Low Voltage, VIL			0.8			0.8	Volts	V_{DD}=5V ±5%
Input High Voltage, VIH	2.0			2.0			Volts	V_{DD}=5V ±5%
Input Current IIN			±2.0			±2.0	µA	
Input Capacitance		3.0			3.0		pF	
DIGITAL OUTPUTS								
Data Format								
Data Coding								See Timing Diagram
VOH	4.0			2.0			Volts	V_{DD}=5V ±5%, IOH=-0.4mA
VOL			0.4			0.4	Volts	V_{DD}=5V ±5%, IOL=+1.6mA
AC ACCURACY								
Spurious free Dynamic Range (SFDR)		86			86		dB	For all FFT's (Full Differential Mode) If V_{CC} = 5V fsample = 31.25kHz fin = 15kHz
Total Harmonic Distortion (THD)		-83			-80		dB	
Signal to Noise & Distortion (SINAD)		73			72		dB	If V_{CC} = 3.3V fsample = 20.8kHz fin = 5kHz
Signal to Noise (SNR)		73.5			72.5		dB	
SAMPLING DYNAMICS								
Acquisition Time to 0.01%		2	3		3	4.5	µs	
-3dB Small Signal BW		4			3		MHz	
Aperture Delay		20			30		nS	
Aperture Jitter		150			150		pS	
Common-Mode Rejection Ratio	70	80		70	80		dB	f_{CM} = 15kHz @ 5 volts 2.8kHz @ 3.3 volts
POWER SUPPLIES							Volts	
V_{CC}	+3.0	+5.0	+5.5	+3.0	+3.3	+5.5		
I_{CC} Operation Mode		230	400		80	300	µA	($\overline{CS}$=0) 33.2kHz, 5V conversion rate. 22.2kHz 3.3 volts
Shutdown Mode		.001	0.5		.001	0.5	µA	($\overline{CS}$=1)
Power Dissipation								
Operating Mode		1.15	2		0.26	0.99	mW	
Shutdown Mode		.005	10		.003	6.6	µW	
TEMPERATURE RANGE								
Commercial		0° to +70°C			0° to +70°C		°C	
Industrial		-40° to +85°C			-40° to +85°C		°C	
Storage		-65° to +150°C			-65° to +150°C		°C	

SPECIFICATIONS (cont.)

Recommended Operating Conditions

SYMBOL	PARAMETERS	VCC=5.0V MIN.	VCC=5.0V TYP.	VCC=5.0V MAX.	VCC=3.3V MIN.	VCC=3.3V TYP.	VCC=3.3V MAX.	UNITS
V_{CC}	Supply Voltage	+3.0	+5.0	+5.5	+3.0	+3.3	+5.5	Volts
f_{CLK}	Clock Frequency			500			333	kHz
t_{CVC}	Total Cycle Time	30.1			45.15			µS
t_{suCS}	Setup Time CSv Before CLK^	100			150			nS
t_{WHCLK}	CLK High Time	.9			1.4			µS
T_{WHCLK}	CLK Low Time	.9			1.4			µS
T_{WHCS}	$\overline{CS}$ High Time between Data Transfers Cycles	100			150			nS

PIN DESCRIPTION



PIN ASSIGNMENTS

Pin 1- V_{REF} - Reference Voltage

Pin 2- +IN - Positive Input

Pin 3- -IN - Negative Input

Pin 4- GND - Ground

Pin 5- $\overline{CS}$/SHDN - Chip Select Bar/Shutdown

Pin 6 - D_{OUT} - Data Out

Pin 7- SCLK - Serial Clock

Pin 8- V_{CC} - Supply

DESCRIPTION

The **SP8528** is a 12 bit full differential sampling ADC with a serial data interface. The ADC samples and converts 12 bits of data in 30.1 µS with a 5V supply voltage applied. The **SP8528** will also operate at a 3.3V supply at 45.15 µS throughput. The device automatically shuts down to a ±0.5 µA (MAX) level as soon as the chip is deselected ($\overline{CS}$=1). Serial data output is available in an MSB first or LSB first format.

FEATURES

The input sampling scheme is full differential, where the maximum full scale range is V_{REF}. The signal is applied between +IN and -IN. The signals applied at each input may both be dynamic. This is in contrast with pseudo differential devices which must have input low held at a constant level during conversion. The converter will provide significant common mode rejection because of the full differential sampling. Each input independently must remain between ground and Vcc to avoid clamping the inputs. For proper conversion the differential input (+IN - -IN) must be less than or equal to Vref.

The device uses a capacitive DAC architecture which provides the sampling behavior. This results in full Nyquist performance at the fastest throughput rate (33.2kHz) the device is capable of.

The power supply voltage is variable from 3.0V to 5.5V which provides supply flexibility. At the 5.0V supply level, conversion plus sampling time is 30.1 µS and supply current is 230 µA (1.15 mW). With a 3.3V supply the conversion plus sampling time is 45.15 µS and current is reduced to 80 µA (0.26 mW).

ADC TRANSFER FUNCTION

INPUT VOLTAGE (+IN - -IN)	INPUT VOLTAGE AT V_{REF} = 5V	OUTPUT CODE
0 LSB	0V	000000000000
1 LSB	0.00122V	000000000001
2048 LSB	2.5000V	100000000000
4094 LSB	4.9976V	111111111110
4095 LSB	4.9988V	111111111111

The device features automatic shutdown and will shutdown to a ±0.5 µA power level as $\overline{CS}$ is brought high (de-selected). Power is proportional to conversion duty cycle and varies from 230 µA at 30.1 µS (Duty cycle = 100%) to 5.75 µA at 1.2 ms (Duty cycle = 2.5%).

Examples:

Conversion rate	I_{CC} @ 5V	Duty Cycle
30.1 µS	230 µA	100%
60.2 µS	115 µA	50%
120 µS	57.5 µA	25%
1.20 mS	5.75 µA	2.5%

The device can be configured such that it delivers serial data MSB first requiring 15 clock periods for a full conversion. Alternately, the device can be programmed to deliver 12 bits of data MSB first, followed by the same 12 bits of data LSB first. This sequence will require 26 clock periods to complete. Please refer to the timing diagram.

Circuit Operation

The **SP8528** is a SAR converter with full differential sampled front end, capacitive DAC, precision comparator, Successive Approximations Register, control logic and data output register. After the input is sampled and held the conversion process begins. The DAC MSB is set and its output is compared with the signal input, if the DAC output is less than the input, the comparator outputs a one which is latched into the SAR and simultaneously made available at the ADC serial output pin. Each bit is tested in a similar manner until the SAR contains a code which represents the signal input to within ±1/2 LSB. During this process the SAR content has been shifted out of the ADC serially. If the MSB first format was chosen, the data will appear at the DOUT pin MSB through LSB in 15 clock periods. If LSB first data is desired, 26 SCLK's are needed to complete a transfer. The LSB appears at clock 15, with successive bits clocked out until the MSB appears at clock 26. All subsequent SCLK's with $\overline{CS}$ = 0 shift out 0. Note that the Chip Select Bar pin must be toggled high

between conversions. The DOUT pin will be in a high impedance state whenever Chip Select Bar is high. After Chip Select Bar has been toggled and brought low again, the converter begins a new conversion.

Single Ended or Full Differential Operation

The **SP8528** has a balanced full differential front end. The **SP8528** can be used in this manner, or it can be used in single-ended circuits as well. For single-ended systems, simply tie the -IN to the Reference Low of the input signal, which is allowed to range from 0V to V_{CC}. For a full differential sampling configuration, both inputs are sampled and held simultaneously. Because of the balanced differential sampling, dynamic common mode noise riding along the input signal is cancelled above and beyond DC noise. This is a significant improvement over psuedo-differential sampling schemes, where the low side of the input must remain constant during the conversion, and therefore only DC noise (i.e. signal offset) is cancelled. If AC common mode noise is left to be converted along with the differental component, the output signal will be degraded.

Full differential sampling allows flexibility in converting the input signal. If the signal low-side is already tied to a ground elsewhere in the system, it can be hardwired to the low side input (i.e., -IN) which acts as a signal ground sense, breaking a potential ground loop. It is also possible to drive the inputs balanced differential, as long as both inputs are within the power rails. In this configuration, both the high and low signals have the same impedance looking back to ground, and therefore pick up the same noise along the physical path from signal source (i.e., sensor, transducer, battery) to the converter. This noise becomes common mode, and is cancelled out by the differential sampling of the **SP8528**.

Layout Considerations

To preserve the high resolution and linearity of the **SP8528** attention must be given to circuit board layout, ground impedance and bypassing.

A circuit board layout which includes separate analog and digital ground planes will prevent the coupling of noise into sensitive converter circuits and will help to preserve the dynamic performance of the device. In single ended mode, the analog input signal should be referenced to the ground pin of the converter. This prevents any voltage drops that occur in the power supply's common return from appearing in series with the input signal.

In full differential mode, the high and low side board traces should run close to each other, with the same layout. This will insure that any noise coupling will be common mode, and cancelled by the converters (patent pending) full differential architecture.

If separate analog and digital ground planes are not possible, care should be used to prevent coupling between analog and digital signals. If analog and digital lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated by a circuit board trace which is connected to common.

The reference pin on the **SP8528** should be kept as clean as possible. A noise signal of 1.22mV (for VREF = 5.0V) will produce 1 lsb of error in the output code. For convenience, the VREF pin can be tied to the VCC pin, but now the same care should be taken with the VCC pin as with the VREF pin. Whether or not VCC is tied to VREF, the VCC pin should always be bypassed to the GROUND pin with a parallel combination of a 6.8µF tantalum and a 0.1µF ceramic capacitor. To maintain maximum system accuracy, the supply connected to the VCC pin should be well isolated from digital supplies and wide load variations. A separate conductor from the supply regulator to the A/D converter will limit the effects of digital switching elsewhere in the system. Power supply noise can degrade the converters performance. Especially corrupting are noise and spikes from a switching power supply.

To avoid introducing distortion when driving the A/D converter input, the input signal source should be able to charge the **SP8528's** equivalent 20 pF of input capacitance from zero volts to the signal level in 1.5 clock periods.

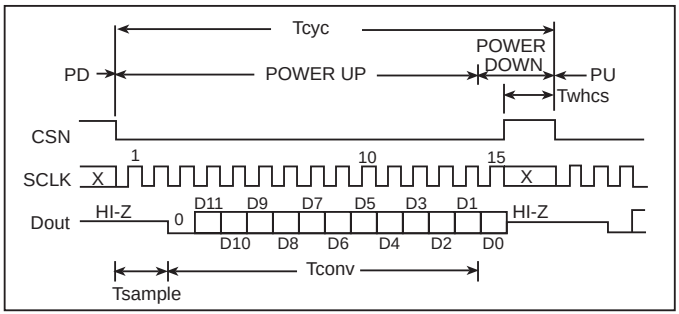


FIGURE 1. MSB FIRST TIMING

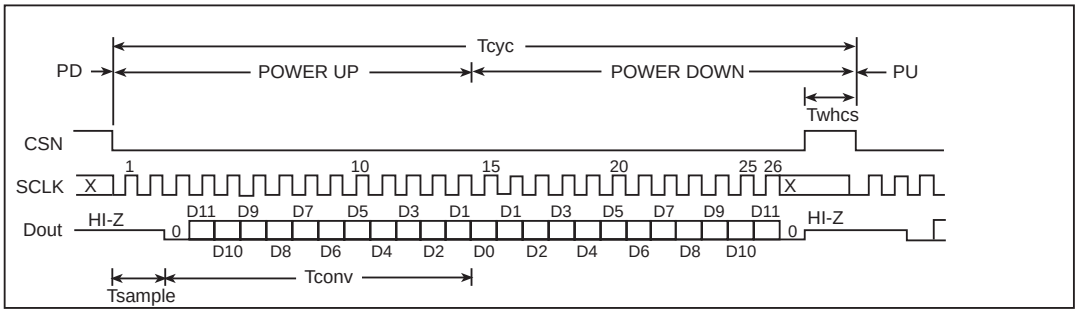


FIGURE 2. LSB FIRST TIMING

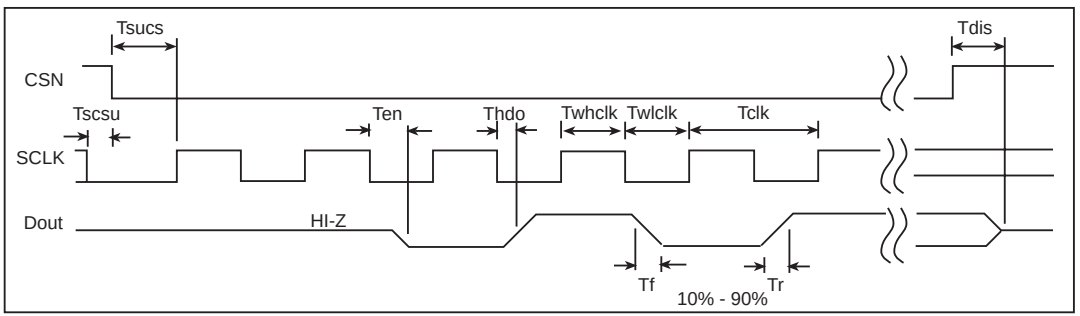


FIGURE 3. DETAILED TIMING

SP8528 Timing Diagram

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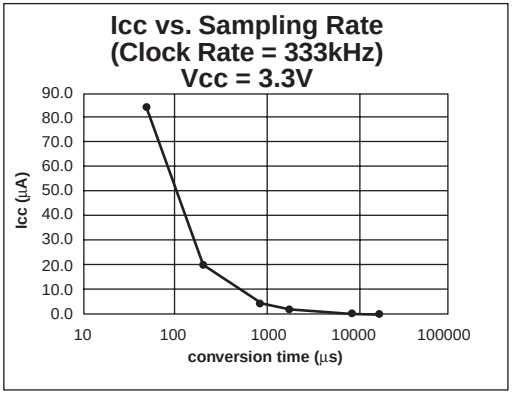
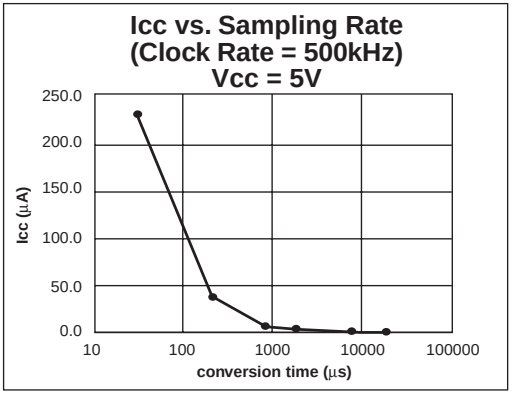
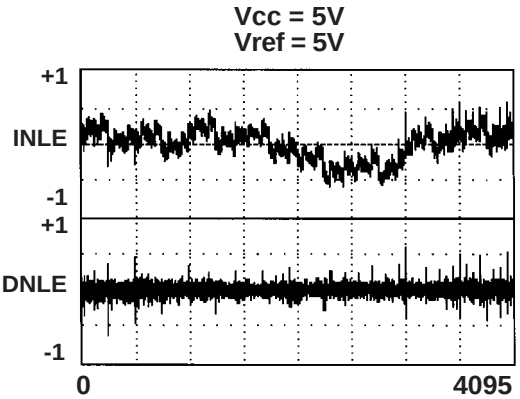
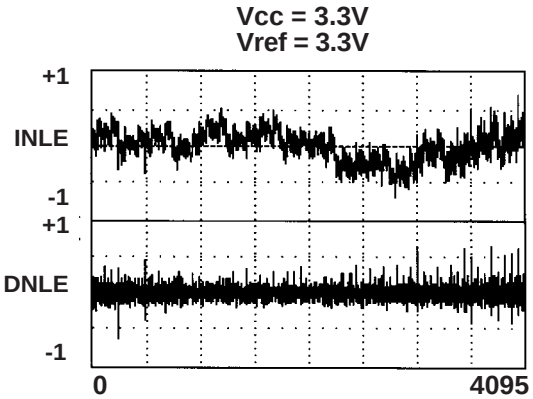
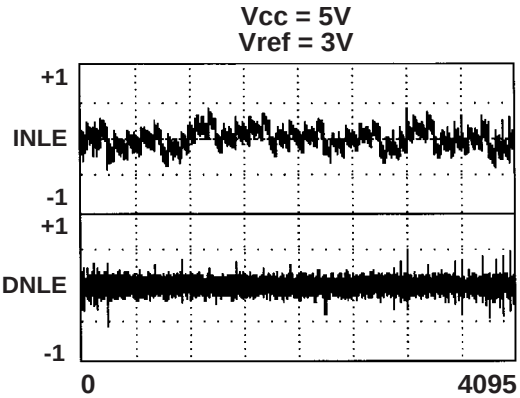
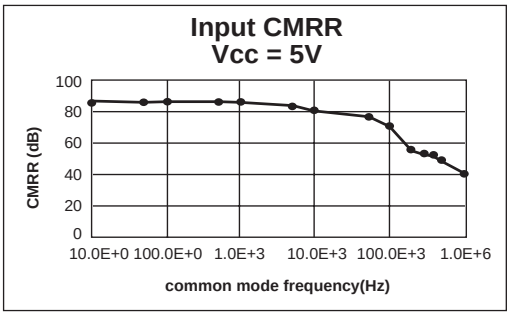




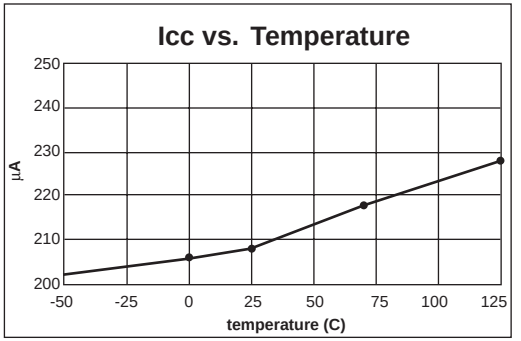


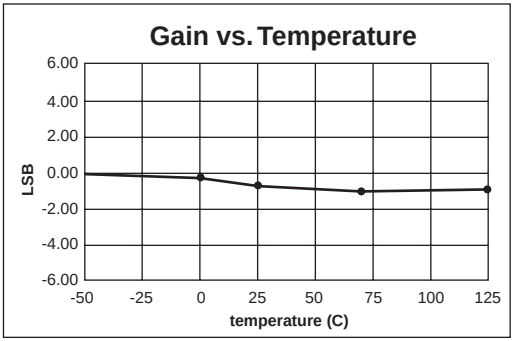


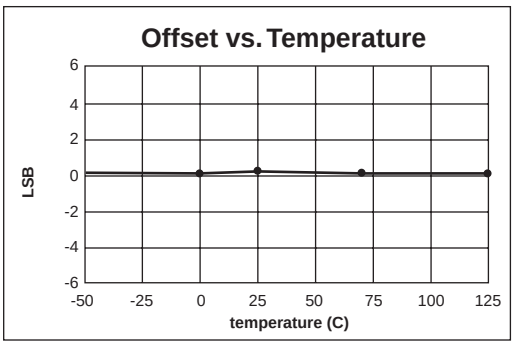


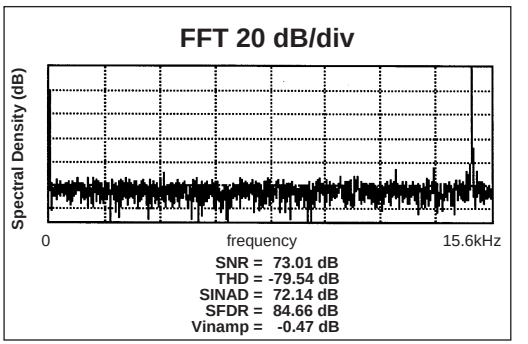


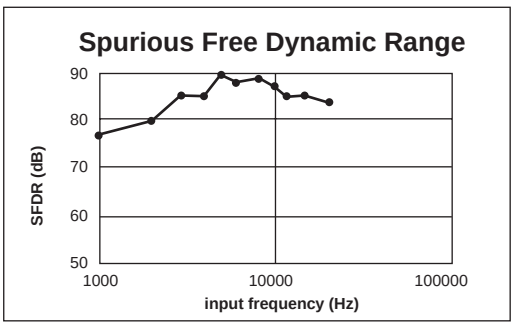
For all plots, V_{CC} = 5V, Conversion Rate = 31.25kHz.

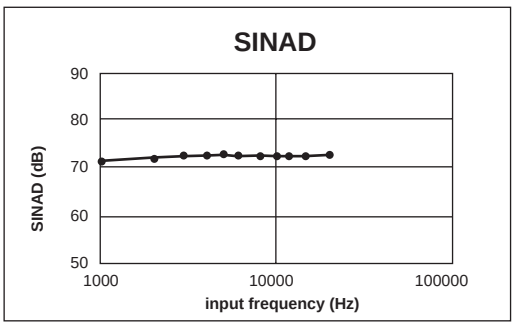


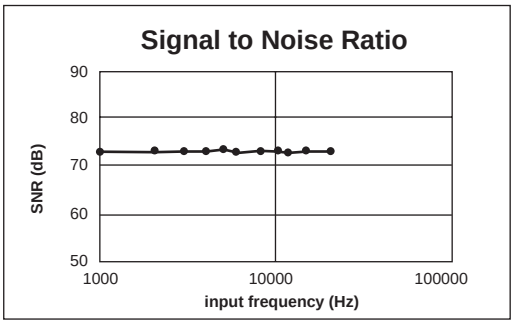


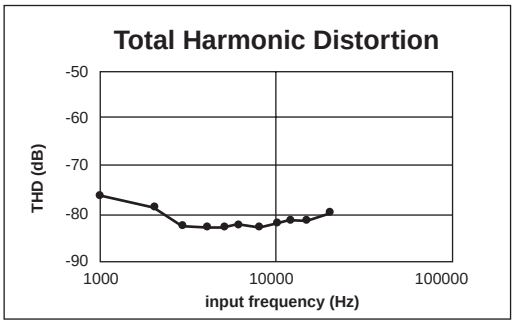












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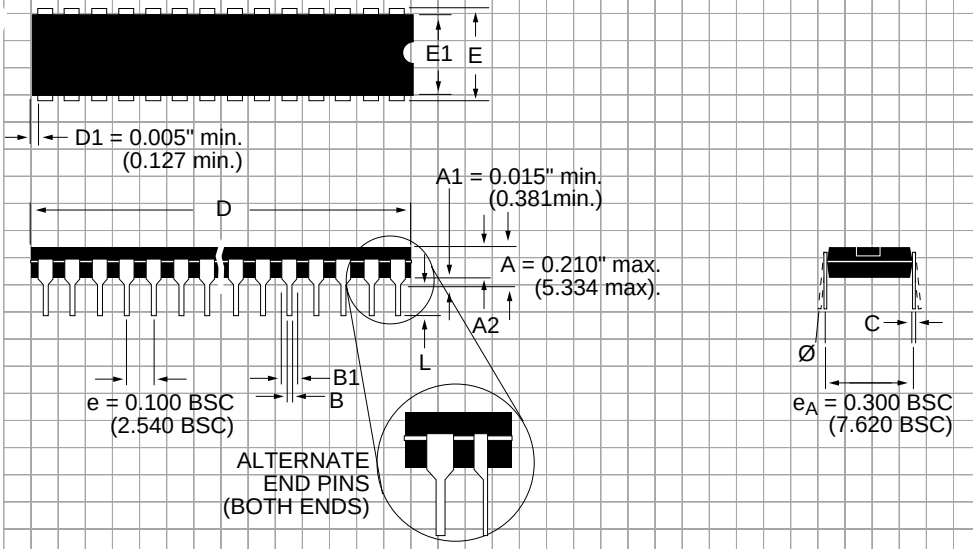
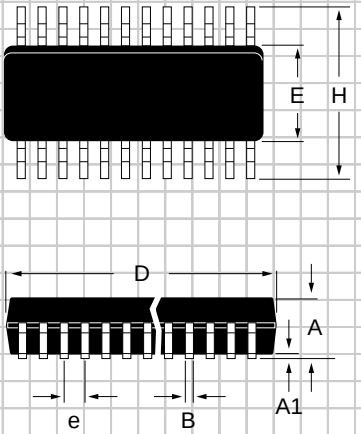
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

ORDERING INFORMATION

Model	Linearity (LSB)	Temperature Range	Package
SP8528BN	±1.0	–40˚C to +85˚C	8-pin, 0.3" Plastic DIP
SP8528KN	±1.0	–0˚C to +70˚C	8-pin, 0.3" Plastic DIP
SP8528BS	±1.0	–40˚C to +85˚C	8-pin, 0.15" Plastic SOIC
SP8528KS	±1.0	–0˚C to +70˚C	8-pin, 0.15" Plastic SOIC
SP8528AN	±2.0	–40˚C to +85˚C	8-pin, 0.3" Plastic DIP
SP8528JN	±2.0	–0˚C to +70˚C	8-pin, 0.3" Plastic DIP
SP8528AS	±2.0	–40˚C to +85˚C	8-pin, 0.15" Plastic SOIC
SP8528JS	±2.0	–0˚C to +70˚C	8-pin, 0.15" Plastic SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

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