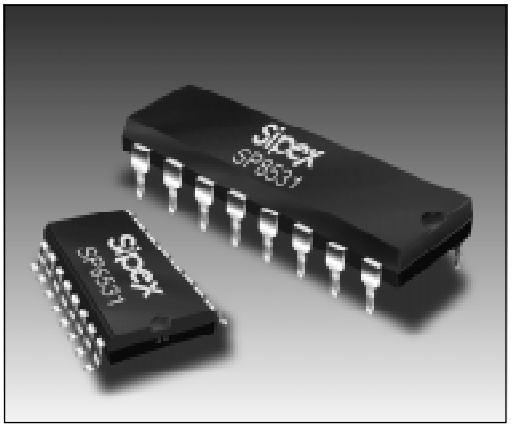
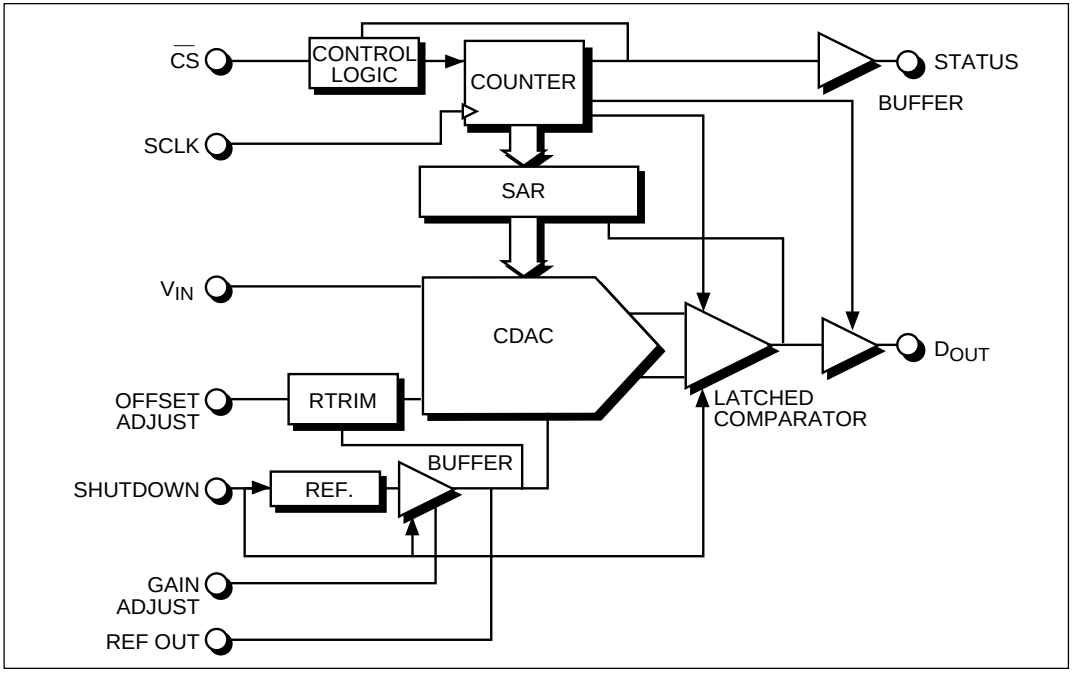
12-Bit Sampling Serial Out Analog to Digital Converter

- 12 Bit Resolution
- Single +5Volt Supply
- Internal Reference, 1.25V
- Unipolar 0 to +2.5 Volt Input Range
- Fast, 3.75 µs Conversion Time
- Fast Power Shutdown/Turn-On Mode
- 3-Wire Synchronous Serial High Speed Interface
- 2µA Shutdown Mode (10µW)
- Low Power CMOS 60mW typical



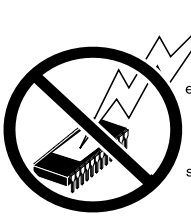
DESCRIPTION

The **SP8531** is a sampling 12-Bit serial out analog to digital converter. The device contains a high speed 12-Bit analog to digital converter, internal reference, and sample/hold circuitry. The **SP8531** is available in 16-pin PDIP and SOIC packages, specified over Commercial and Industrial temperature ranges.



ABSOLUTE MAXIMUM RATINGS

(TA=+25˚C unless otherwise noted) .....
VDD to DGND ..... -0.3V to +7V
VDA to AGND ..... -0.3V to +7V
Vin to AGND ..... -0.3V to VDA +0.3V
Digital Input to VSS ..... -0.3V to VDD+0.3V
Digital Output to VSS ..... -0.3V to VDD+0.3V
Operating Temp. Range
Commercial (J,K Version) ..... 0˚C to 70˚C
Industrial (A,B Version) ..... -40˚C to +85˚C
Storage Temperature ..... -65˚C to 150˚C
Lead Temperature(Solder 10 sec) ..... +300˚C
Power Dissipation to +70˚C 500mW
Derate Above 70˚C ..... 10mW/ ˚C



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

Unless otherwise noted the following specifications apply for V_{DD} = 5V with limits applicable for T_A = 25˚C.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC Accuracy					
Resolution		12		Bits	
Integral Linearity					
J, A		±0.6	±1.0	LSB	
K ,B		±0.4	±0.75	LSB	
Differential Linearity Error					
J, A		±0.5	±1.0	LSB	No Missing Codes
K ,B		±0.5	±1.0	LSB	No Missing Codes
Gain Error					
J, A		±0.2	±1.0	%FSR	Externally Trimmable to Zero
K,B		±0.1	±0.5	%FSR	Externally Trimmable to Zero
Offset Error					
J, A		±4	±7	LSB	Externally Trimmable to Zero
K,B		±3	±5	LSB	Externally Trimmable to Zero
Analog Input		0 to 2.5		Volts	
Input Impedance		600K		Ohms	4 MHz Clock Rate
Conversion Speed					
Sample Time	400			ns	
Conversion Time	3.75			µs	
Complete Cycle	4.25			µs	
Conversion					
Rate:			235	KHz	
Clock Speed			4	MHz	

SPECIFICATIONS (continued)

Unless otherwise noted the following specifications apply for V_{DD} = 5V with limits applicable for T_A = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Reference Output		1.25		Volts	
Ref. Out Temp. Coef.					
J, A		30		ppm/°C	
K,B		20		ppm/°C	
Ref.Out Error		±4	±25	mV	
Output Current		1		mA	
Digital Inputs					
Input Low Voltage , VIL			0.8	Volt	VDD= 5V ±5%
Input High Voltage , VIH	2.0			Volt	VDD= 5V ±5%
Input Current IIN		±1		µA	
Input Capacitance		3		pF	
Digital Outputs					
Data Format (1)					
Data Coding (2)					
VOH	4.0			Volt	VDD=5V±5%, IOH=-0.4mA
VOL			0.4	Volt	VDD=5V±5%, IOL=+1.6mA
AC Accuracy					fin=47KHz,VDD=5.0V @ 25°C, SCLK=4MHz
Spurious Free Dynamic Range (SFDR)		83		dB	
Total Harmonic Distortion (THD)		-80		dB	
Signal to Noise & Distortion (SINAD)		71		dB	
Signal to Noise (SNR)		72		dB	
Sampling Dynamics					
Acquisition Time to 0.01%		200		ns	For a ±FS step change at input
-3dB Small Signal BW		13		MHz	
Aperture Delay		35		ns	
Aperture Jitter		10		ps RMS	

SPECIFICATIONS (continued)

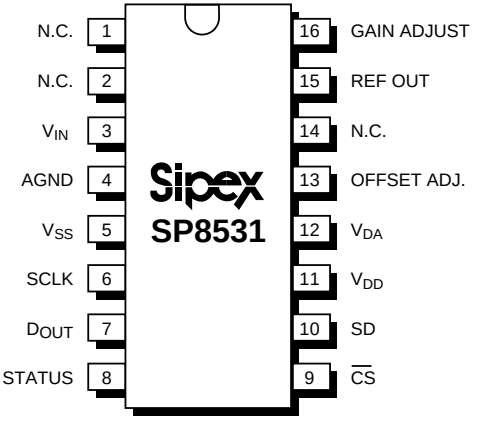
Unless otherwise noted the following specifications apply for V_{DD} = 5V with limits applicable for T_A = 25˚C.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supplies					
VDD	4.75		5.25	Volts	
Supply Current					
Operating Mode		11.5	17	mA	SD=0, VDD=+5.0V
Shutdown Mode		0.01	2	µA	SD=1, V_{DD} = +5.0V
Power Dissipation					
Operating Mode		60	85	mW	SD=0
Shutdown Mode		0.05	10	µW	SD=1
Power Turn On			20	µS	Via Shutdown Control to 1 LSB settling error.
Temperature Range					
Commercial	0	to	+70	˚C	
Industrial	-40	to	+85	˚C	
Storage	-65	to	+150	˚C	

(1) Data Format is 12-Bit Serial
(2) Data Coding is Binary (See Timing Diagram)

PIN ASSIGNMENTS

Pin 1-N.C.-No Connection
Pin 2-N.C.-No Connection
Pin 3-VIN - Analog Input
Pin 4-AGND-Analog Ground
Pin 5-VSS-Digital Ground
Pin 6-SCLK-Serial Clock Input
Pin 7-DOUT Digital Data Output
Pin 8-STATUS- High During Conversion
Pin 9-$\overline{CS}$-Chip Select Bar Input -
High Deselects chip -Low Selects chip
Pin 10-SD-Shutdown Input, logic low=power up, logic high = powerdown
Pin 11-VDD Digital +5V supply
Pin 12-VDA Analog +5V supply
Pin 13-OffADJ- External Offset Adjust
Pin 14-N.C.-No Connection
Pin 15-REFOUT-Voltage Reference Output
Pin 16-GAINADJ-External Gain Adjustment



FEATURES

The **SP8531** is a sampling, 12-Bit serial out data acquisition system. The device contains a high speed 12-bit analog to digital converter, internal reference, and sample and hold circuitry.

The **SP8531** is fabricated in Sipex' Bipolar Enhanced CMOS Process that permits state-of-the-art design using bipolar devices in the analog/linear section and extremely low power CMOS in the digital/logic section.

CIRCUIT OPERATION

Figure 1 shows a simple circuit required to operate the **SP8531**. The conversion is controlled by the user supplied signal Chip Select Bar ($\overline{CS}$) which selects and deselects the device, and a system clock (SCLK).

A high level applied to $\overline{CS}$ asynchronously clears the internal logic, puts the sample & hold (CDAC) into sample mode and places the DOUT (Data Output) pin in a high impedance state.

Conversion is initiated by falling edge on $\overline{CS}$ in slave mode at which point the input voltage is held and a conversion is started. A delay of 90ns is required between the falling edge of $\overline{CS}$ and the first rising of SCLK.

The device responds to the shut down signal asynchronously so that a conversion in progress will be interrupted and the resulting data will be erroneous. A 20 µSec minimum delay is required between the falling edge of shut down and initiation of a conversion.

Data Format

16 bits of data are sent for each conversion. The data is shipped with 4 leading "0"s, and then 12 bits of data, MSB first. Data changes on the falling edge of SCLK and is stable on the rising edge of SCLK.

Continuous stand alone operation is obtained by holding $\overline{CS}$ low. In this mode an oscillator is connected directly to the SCLK pin. The SCLK signal along with the STATUS output Signal are used to synchronize the host system with the converter's data. In this mode there is a single dead SCLK cycle between the 16th clock of one conversion and the first clock of the following conversion for the **SP8531**. At a clock frequency of 4 MHz the **SP8531** provides a throughput rate of 235KHz.

In slave mode operation, $\overline{CS}$ is brought high between each conversion so that all conversions are initiated by falling edge on $\overline{CS}$.

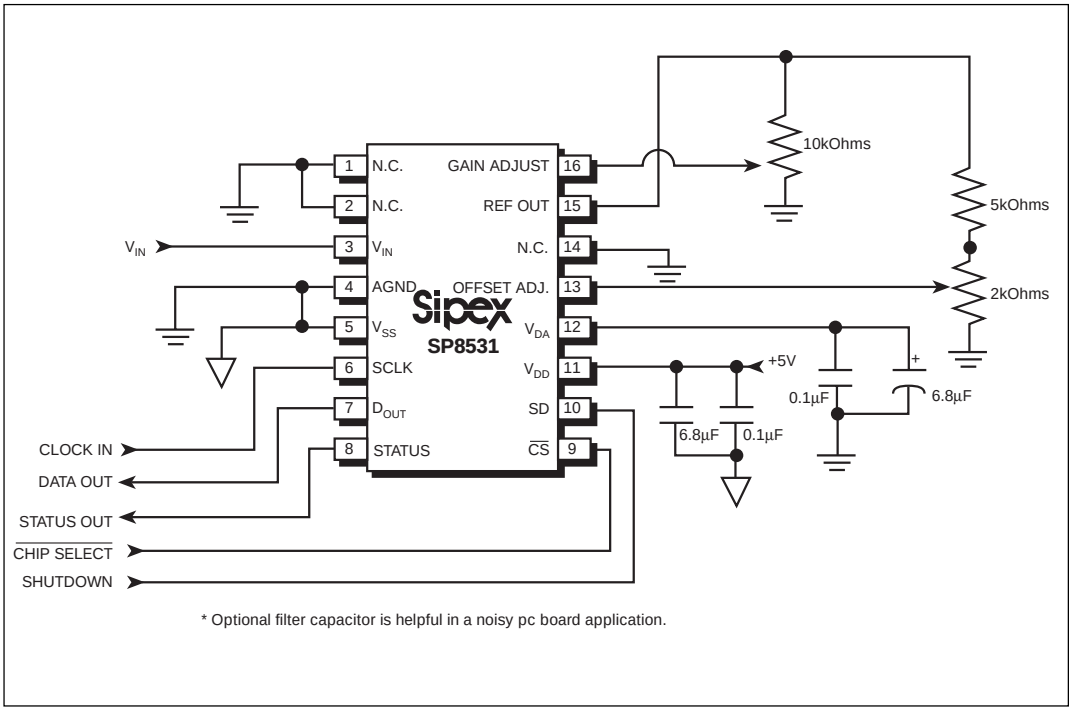


Figure 1. Operating Circuit

Input Impedance

The input of the **SP8531** can be modeled as a resistor in series with a ground referenced DC voltage source of 1.0 volt. Note that the input resistor is a switched capacitor resistor and so its value is inversely proportional to conversion rate. When the ADC is in free running mode with a 4 MHz clock applied (a conversion rate of 235 Ksps) the input resistance is nominally 600K. At a conversion rate of 117.5 Ksps the input resistor value would double to 1.2 megohms. In order to avoid introducing an unadjusted gain error greater than 1 lsb, the device must be driven by a source whose resistance is 4096 times smaller than its input impedance. At the 4 MHz clock rate this would require a source whose resistance was less than 146 Ohms.

Layout Considerations

Because of the high resolution and linearity of the **SP8531**, system design considerations such as ground path impedance and contact resistance become very important.

To avoid introducing distortion when driving the analog inputs of these devices, the source resistance must be very low, or constant with signal level. Note that in the operating circuit there is no connection made between VDA (Pin 12) and the system power supply. This is because the analog supply pin (VDA) is connected internally to the digital supply pin (VDD) through a ten ohm resistor.

This ten ohm resistor when combined with a parallel combination of 6.8µF tantalum and 0.1µF ceramic capacitor between VDA and analog ground, will provide some immunity to noise which resides on the system supply. To maintain maximum system accuracy, the supply connected to the VDD pin should be well isolated from digital supplies and wide load variations.

To limit effects of digital switching elsewhere in a system, it often makes sense to run a separate +5V supply conductor from the supply

regulator to any analog components requiring +5V including the **SP8531**. Noise on the power supply lines can degrade the converters performance, especially corrupting are noise and spikes from a switching power supply.

The ground pins (AGND and VSS) on the **SP8531** are separated internally and should be connected to each other under the converter. Applying the technique of using separate analog and digital ground planes is usually the best way to preserve dynamic performance and reduce noise coupling into sensitive converter circuits. Where any compromise must be made the common return of the analog input signal should be referenced to the AGND pin of the converter. This prevents any voltage drops that might occur in the power supply's common return from appearing in series with the input signal.

Coupling between analog and digital lines should be minimized by careful layout. For instance, if analog and digital lines must cross they should do so at right angles. Parallel analog and digital lines should be separated from each other by a trace connected to common.

If external gain and offset potentiometers are used, the potentiometers and related resistors should be located as close to the **SP8531** as possible.

Minimizing "Glitches"

Coupling of external transients into an analog to digital converter can cause errors which are difficult to debug. In addition to the above discussions on layout considerations, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance from a system using the **SP8531** converter. These potential system problem sources are particularly important to consider when developing a new system, and looking for causes of errors in breadboards.

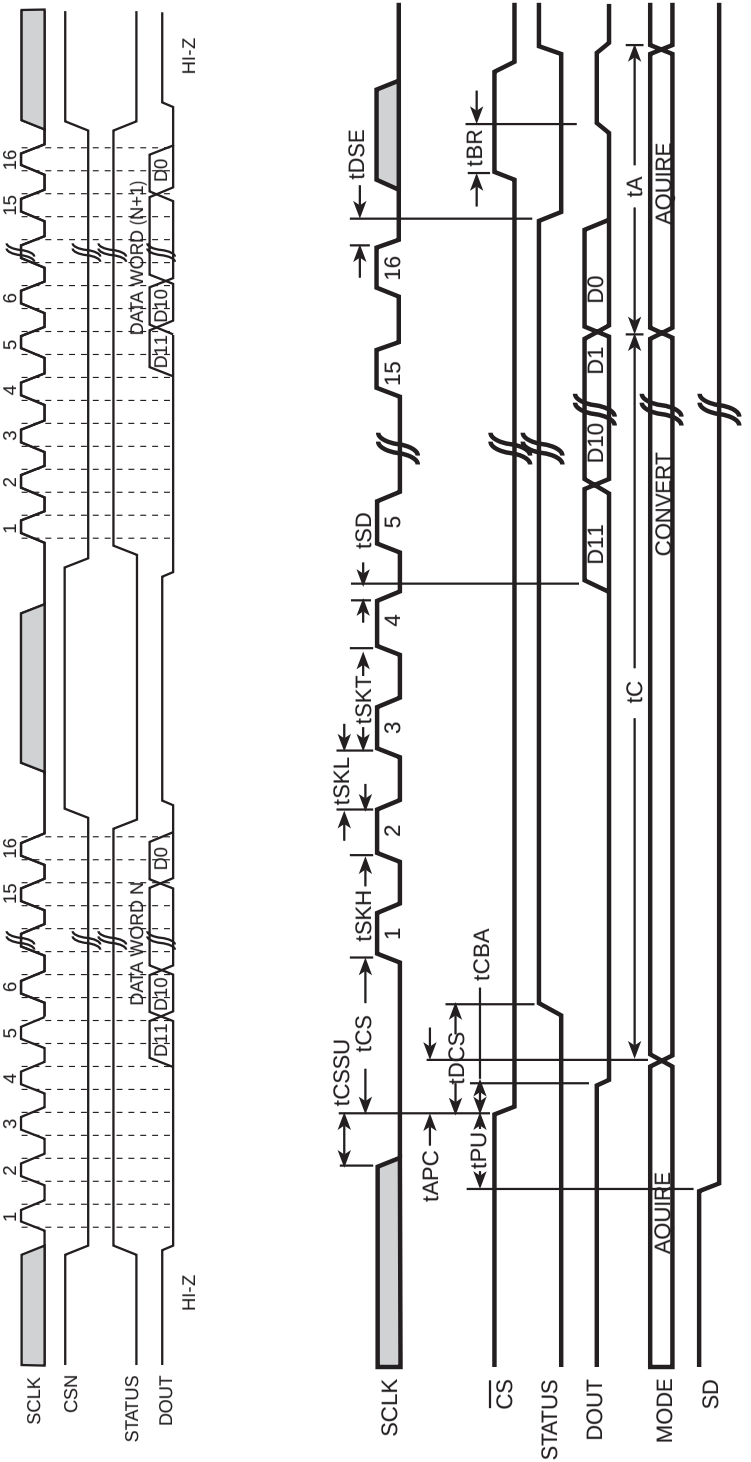
First, care should be taken to avoid transients during critical times in the sampling and conversion process. Since the **SP8531** has a internal sample/hold function, the signal that puts the device into hold state ($\overline{CS}$ going low) is critical, as it would be on any sample/hold amplifier. The $\overline{CS}$ falling edge should have a 5 to 10 ns transition time, low jitter, and have minimal ringing, especially during the first 20ns after it falls.

TIMING CHARACTERISTICS

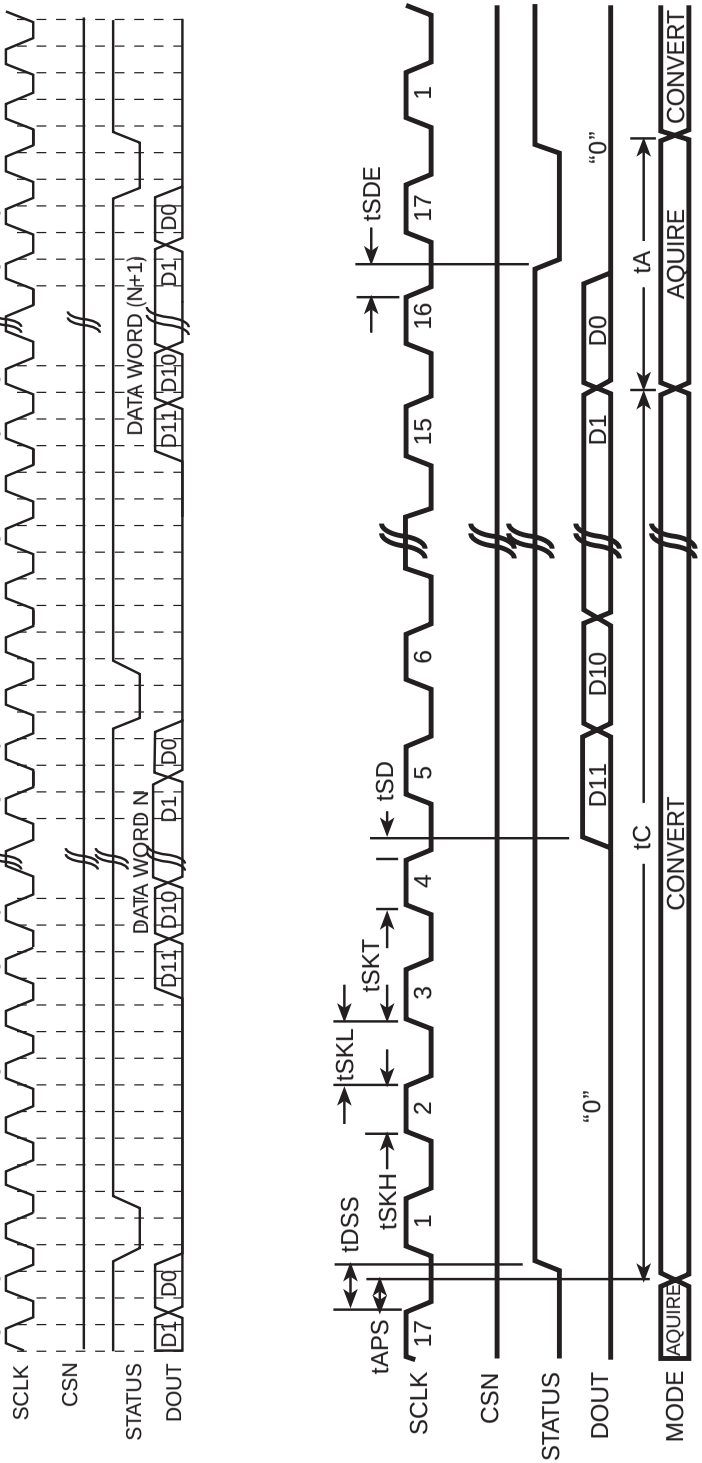
(Typical @ 25°C with V_{DD} = +5V, unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	COND.
Thoughput Time (tTP=tA+tC)	4.25			µs	
Acquisition Time (tA) (2 SCLK Periods)	400	500		ns	
Conversion Time (tC) (15 SCLK Periods)	3.75			µs	
SCLK Low Pulse Width (tSKL)	110	125		ns	
SCLK High Pulse Width (tSKH)	110	125		ns	
SCLK Period (tSKT)	250			ns	
Bus Access Time (tCBA)		51		ns	
Bus Relinquish Time (tBR)		45		ns	
Setup Time -SCLK Falling to CSN Falling (tCSSU)	0			ns	
CSN Low Before SCLK Rises (tCS)	90			ns	
SCLK Falling to Data Valid (tSD)		50		ns	
CSN Falling to status Rising (tDCS)		69		ns	
SCLK 17 Falling to Status Rising Free Run (tDSS)		70		ns	
SCLK 16 Falling to Status Falling (tDSE)		45		ns	
Delay SD Low to initiate Conversion (tPU)		5		µs	
Aperture Delay Slave-Mode (tAPC)		30		ns	
Aperture Delay Free-Running Mode (tAPS)		35		ns	

TIMING DIAGRAMS



Slave Mode



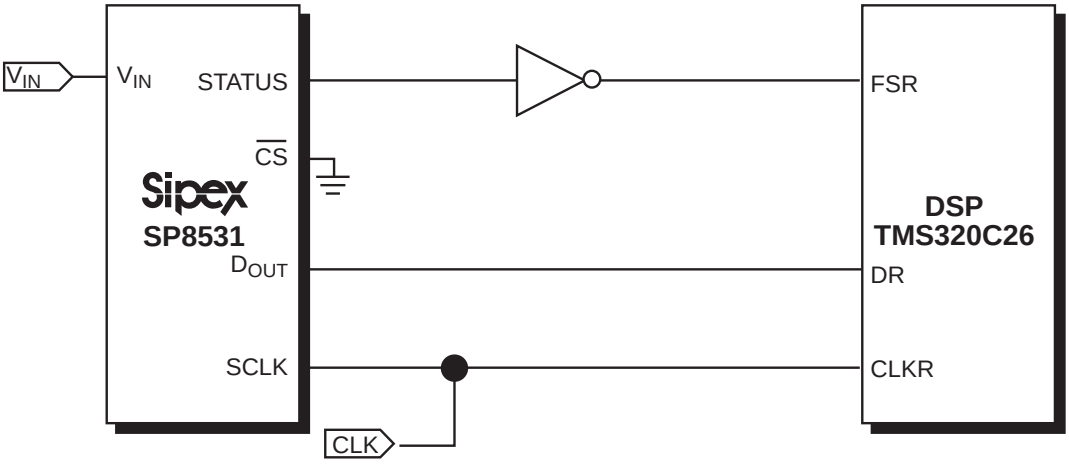
Free Running Mode

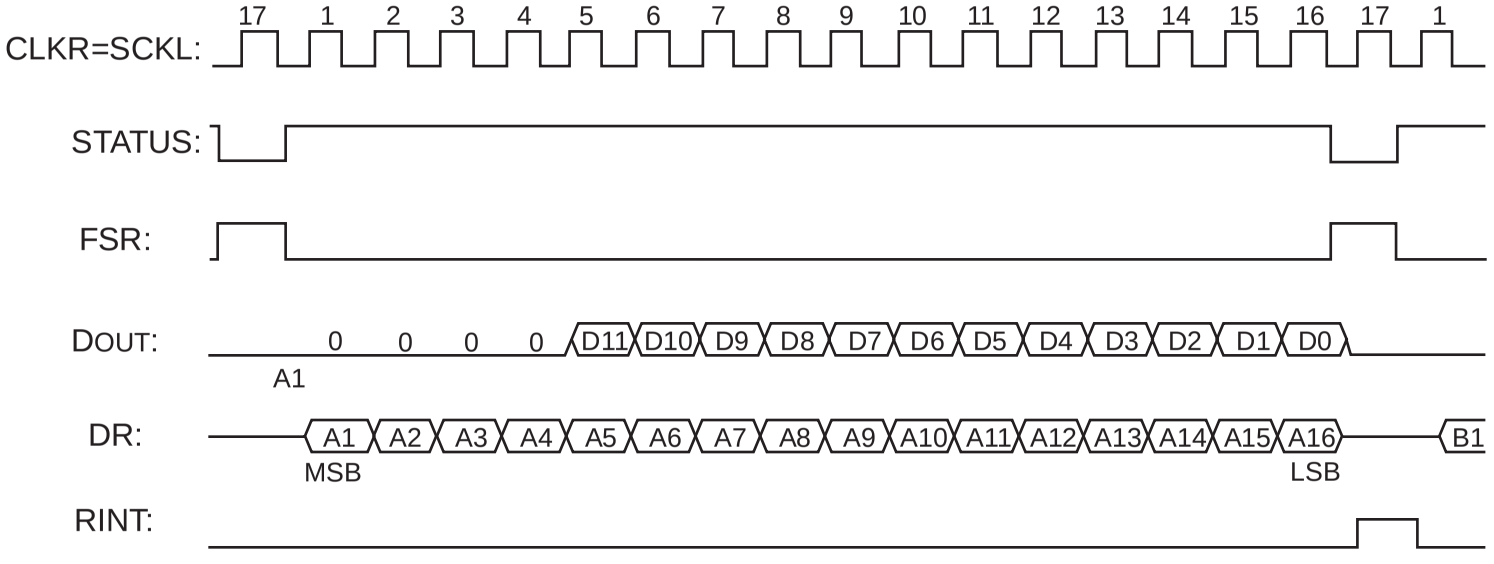
Communication to DSP TMS320C26 in Free-Run

To use free-run mode the chip select on the **SP8531** must be low and is therefore tied to ground. Since status gives a low pulse before the start of conversion, this signal is used to provide the necessary Frame Sync Receive (FSR) pulse to start reading the data. All it needs is an inverter to provide for the correct logic level.

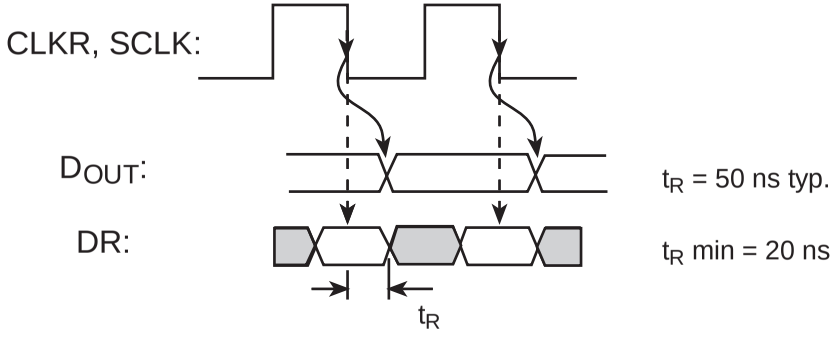
The Data Out (Dout) can be connected directly to the Data Receive (DR) of the DSP and both elements use the same externally provided clock. The minimal hold time for DR after falling edge of CLKR is 20ns where the typical hold time for the **SP8531** is 50ns making the data read valid.

Note that although the **SP8531** is essentially a 12 bit converter, it sends 16 bits with the four MSB's as zero's.



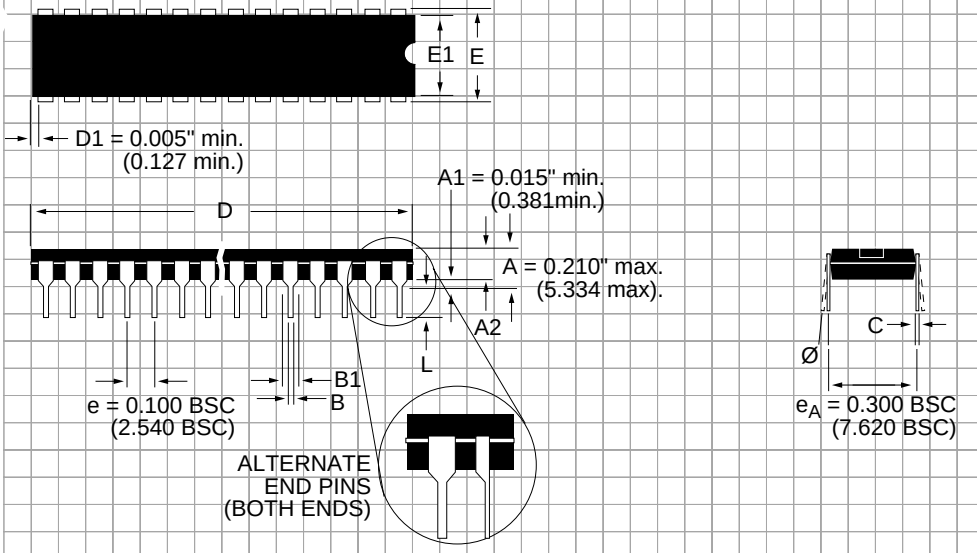


TIMING DIAGRAM FOR SP8531 TO DSP TMS320C26



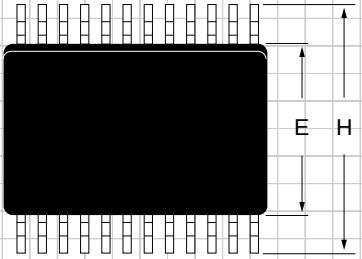
```
THIS PROGRAM  IS USED  FOR SERIAL  COMMUNICATION BETWEEN THE
SP8531 AND THE DSP TMS320C26 WITH THE DSP AS SLAVE.

        .INCLUDE        "MMREGS.ASM"
        .PS             0FA0Ah  ;ADDRESS FOR RINT
        B               RINT    ;RINT (RECEIVE INTERRUPT)

        .PS             0FB00h  ;START ADRES OF PROGRAM
        .ENTRY                  ;START PROGRAM HERE
        LDPK            0       ;DIRECT PAGE POINTER
        CONF            1       ;CONFIGURE MODE 1
START   LRLK            AR0,400h ;ADDRESS TO SAVE TO
        SFSM                    ;USE FRAME SYNCHRONIZATION
        LAC             IMR     ;---\
        ORK             11h     ;    ---- INTERRUPT MASK
        SACL            IMR     ;---/
        EINT                    ;ENABLE INTERRUPTS
LOOP    IDLE                    ;WAIT FOR AN INTERRUPT
        B               LOOP    ;GO BACK TO LOOP

        ;HERE BEGINS RECEIVE INTERRUPT ROUTINE :
RINT    LAC             DRR     ;READ DATA
        LARP            AR0
        SACL            *+      ;STORE DATA ON ADRES AR0
        .END
```

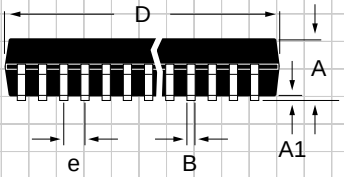

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

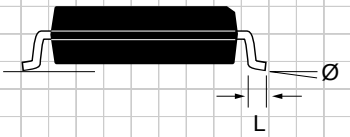


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)







DIMENSIONS (Inches) Minimum/Maximum (mm)	14–PIN	16–PIN	18–PIN	20–PIN	24–PIN	28–PIN
A	0.090/0.104 (2.29/2.649))	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649))	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.348/0.363 (8.83/9.22)	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)	0.496/0.512 (12.60/13.00)	0.599/0.614 (15.20/15.59)	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC))	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

ORDERING INFORMATION

Model segment Model	INL Linearity (LSB)	Temperature Range	Package Types
SP8531JN	±1.0	0˚C to +70˚C	16-pin, 0.3" Plastic DIP
SP8531JS	±1.0	0˚C to +70˚C	16-pin, 0.3" SOIC
SP8531KN	±0.75	0˚C to +70˚C	16-pin, 0.3" Plastic DIP
SP8531KS	±0.75	0˚C to +70˚C	16-pin, 0.3" SOIC
SP8531AN	±1.0	-40˚C to +85˚C	16-pin, 0.3" Plastic DIP
SP8531AS	±1.0	-40˚C to +85˚C	16-pin, 0.3" SOIC
SP8531BN	±0.75	-40˚C to +85˚C	16-pin, 0.3" Plastic DIP
SP8531BS	±0.75	-40˚C to +85˚C	16-pin, 0.3" SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600