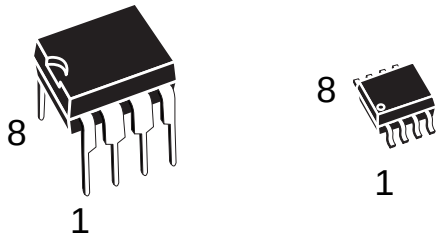
M34S32

32K Serial I^2C Bus EEPROM With User-Defined Read-Only Block and 32-Byte OTP Page

PRELIMINARY DATA

- TWO WIRE I^2C SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- COMPATIBLE WITH I^2C EXTENDED ADDRESSING
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
- HARDWARE WRITE CONTROL
- USER-DEFINED READ-ONLY BLOCK
- 32 BYTES OTP PAGE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD and LATCH-UP PERFORMANCES

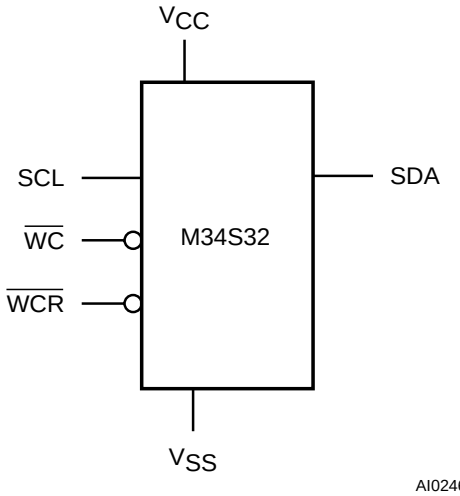
Figure 1. Delivery Forms



PSDIP8 (BN)
0.25 mm Frame

S08 (MN)
150 mil Width

Figure 2. Logic Diagram



DESCRIPTION

The M34S32 is a 32K bit electrically erasable programmable memory (EEPROM), organized as 4096 x 8 bits.

Table 1. Signal Names

SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
$\overline{WCR}$	Write Control of Control Register
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 3. DIP Pin Connections

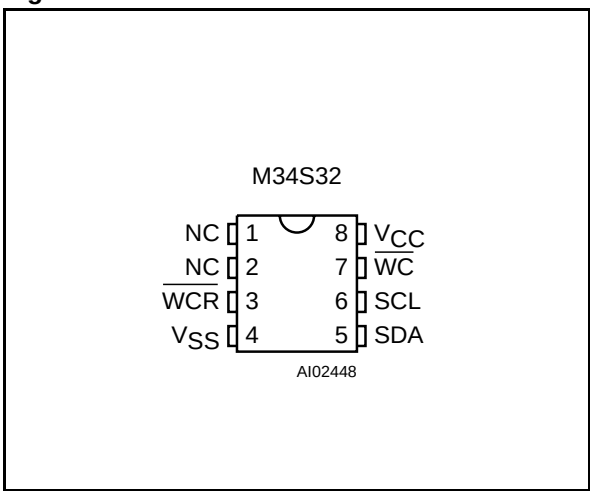


Figure 4. SO Pin Connections

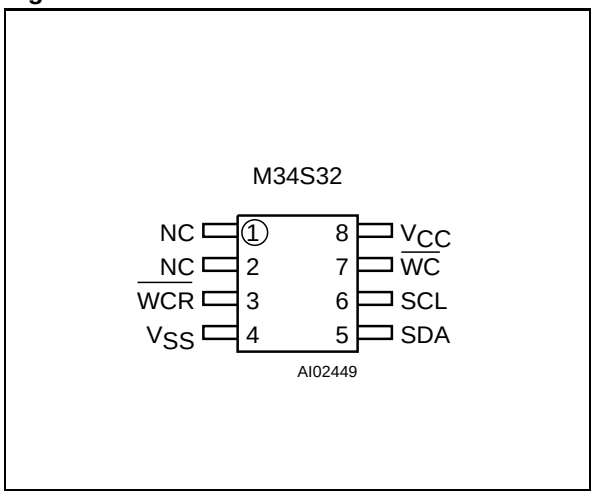


Table 2. Absolute Maximum Ratings(1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package)	40 sec	215	°C
		(PSDIP8 package)	10 sec	260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage	(Human Body model) 1. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)		4000	V
	Electrostatic Discharge Voltage	(Machine model) 2. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)		500	V

Note: 1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

The memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memory behaves as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by the Device Select Byte. This is a stream of 4 bits (the identification code 1010), then 3 bits of memory block access input, plus one read/write bit. The byte is finally terminated by an acknowledge bit.

The M34S32 contains three memory blocks: the OTP page, the EEPROM block and the ROM block. The OTP (One Time Programmable) page is a page of 32 bytes, written once by the user. The OTP page is not located within the 32 Kbits EEPROM area. Once written, the OTP page cannot be modified by further write instructions. The ROM block resides inside the 32 Kbit EEPROM area. The size of the ROM block is defined (by the user) with the help of the Control Register.

The OTP page is accessed with the Device Select Byte 1010001x, the EEPROM and ROM blocks are accessed with the Device Select Byte 1010000x. The control register is accessed with the Device Select Byte 1010100x (see Table 3).

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition.

Power On Reset: VCC lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the VCC voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when VCC drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable VCC must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to VCC to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from the SDA bus line to V_{CC} (see Figure 3).

Table 3. Device Select Byte

	Device Code				Memory Block Access			$R\overline{W}$
Device Select Bit	b7	b6	b5	b4	b3	b2	b1	b0
EEPROM and ROM access	1	0	1	0	0	0	0	$R\overline{W}$
OTP Page access	1	0	1	0	0	0	1	$R\overline{W}$
Control Register access	1	0	1	0	1	0	0	$R\overline{W}$

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	Data Bytes	Initial Sequence
Current Address Read	1	1	START, Device Select, $R\overline{W}$ = 1
Random Address Read	0	1	START, Device Select, $R\overline{W}$ = 0, Address
	1		reSTART, Device Select, $R\overline{W}$ = 1
Sequential Read	1	≥ 1	As CURRENT or RANDOM Mode
Byte Write	0	1	START, Device Select, $R\overline{W}$ = 0
Page Write	0	≤ 32	START, Device Select, $R\overline{W}$ = 0

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the whole EEPROM area from any erroneous erase/write cycle. It also protects the OTP page against the first write attempt. The Write Control signal polarity can be selected with the WCpol bit of the Control Register (see Table 13). When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as VIL (see Table 5).

When $\overline{WC}$ and WCpol are activating the Write Protection, Device Select and Address bytes are acknowledged; Data bytes are not acknowledged (see Figure 11).

Write Control ($\overline{WCR}$). In order to prevent spurious writes to the Control Register, the user can also make the Control Register Read Only (Write is inhibited). This is achieved by use of the $\overline{WCR}$ pin and the CRWD bit (see Table 14) :

– - if CRWD bit = 0, the Control register can be modified regardless of the state of the $\overline{WCR}$ pin.
– - if CRWD bit = 1, the Control register can be modified if the $\overline{WCR}$ pin is high.
– - if CRWD bit = 1 and the $\overline{WCR}$ pin is low, the Control Register is Write Protected.

DEVICE OPERATION

I²C Bus Background

The memory supports the extended addressing I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The memory is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the stand-by state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the memory samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave memory, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a Device Select Byte of 4 bits that identifies the device type, 3 memory block access bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. Communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters (1)
(T_A = 25°C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_L	$\overline{WC}$, $\overline{WCR}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_H	$\overline{WC}$, $\overline{WCR}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested in production.

Figure 5. Maximum RL Value versus Bus Capacitance (CBUS) for an I^2C Bus

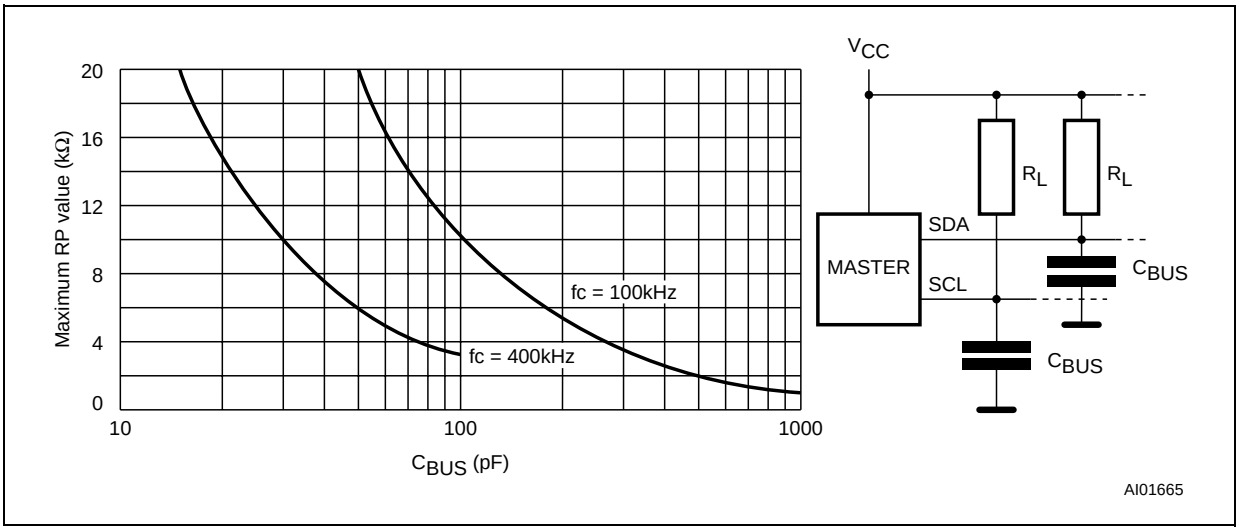


Table 6. DC Characteristics (T_A = 0 to 70°C, –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0 \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0 \le V_{OUT} \le V_{CC}$; SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5 V; f_C = 400 kHz (rise/fall time < 30 ns)		2	mA
	Supply Current (W series)	V_{CC} = 2.5 V; f_C = 400 kHz (rise/fall time < 30 ns)		1	mA
I_{CC1}	Stand-by Current	$V_{IN} = V_{SS}$ or V_{CC} ; V_{CC} = 5 V		10	µA
I_{CC2}	Stand-by Current (W series)	$V_{IN} = V_{SS}$ or V_{CC} ; V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage ($\overline{WC}$, $\overline{WCR}$)		– 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$, $\overline{WCR}$)		V_{CC} - 0.5	V_{CC} + 1	V
V_{IL}	Input Low Voltage (other pins)		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (other pins)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
	Output Low Voltage (W series)	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Table 7. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}
Input and Output Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}

Figure 6. AC Testing Input/Output Waveforms

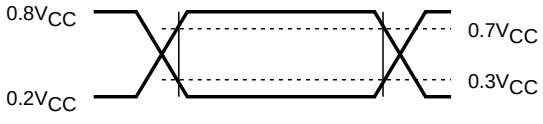


Table 8. AC Characteristics (T_A = 0 to 70°C, –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V)

Symbol	Alt.	Parameter	M34S32				Unit
			V_{CC} = 4.5V to 5.5V		V_{CC} = 2.5V to 5.5V		
			Min.	Max.	Min.	Max.	
t_{CH1CH2}	t_R	Clock Rise Time		300		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		1300		ns
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1300		1300		ns
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	ns
t_{QLQx}	t_{DH}	Data Out Hold Time	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400	kHz
t_W	t_{WR}	Write Time		10		10	ms

Note: 1. Sampled only, not 100% tested in production.
2. For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away from SCL=1 in order to avoid unwanted START and/or STOP conditions.

EEPROM Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. Bits b15 to b0 form the address of any byte of the memory. Bits b15 to b12 are don't care on the M34S32 series.

Table 9. Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8
X	X	X	X				

4. b15 to b12 are Don't Care.

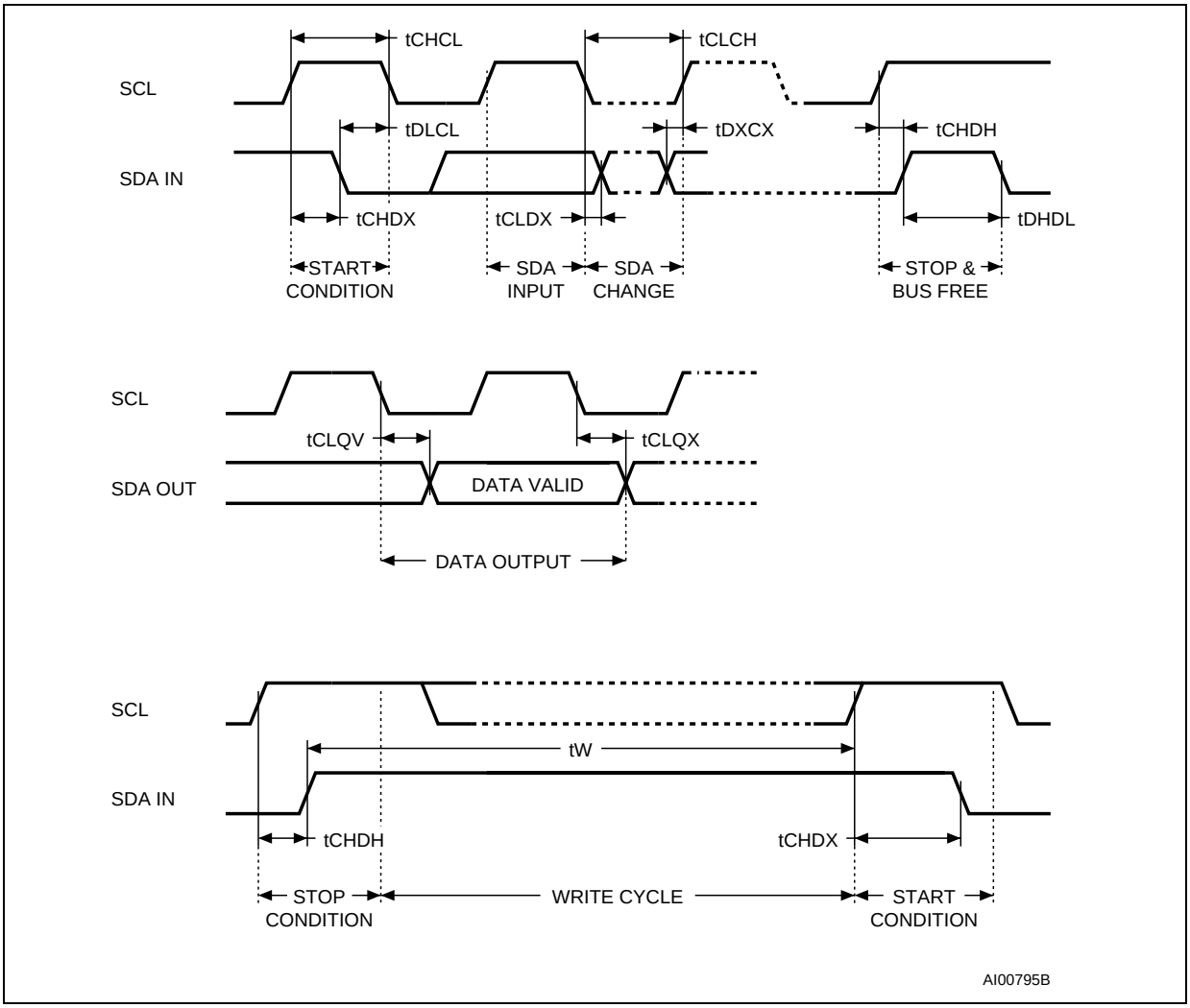
Table 10. Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Write Operations

Following a START condition the master sends a Device Select Byte with the R$\overline{W}$ bit reset to 0. The memory acknowledges this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the memory location. Writing in the memory may be inhibited with $\overline{WC}$ pin and WCpol bit (see Table 13 and Figure 11).

Figure 7. AC Waveforms

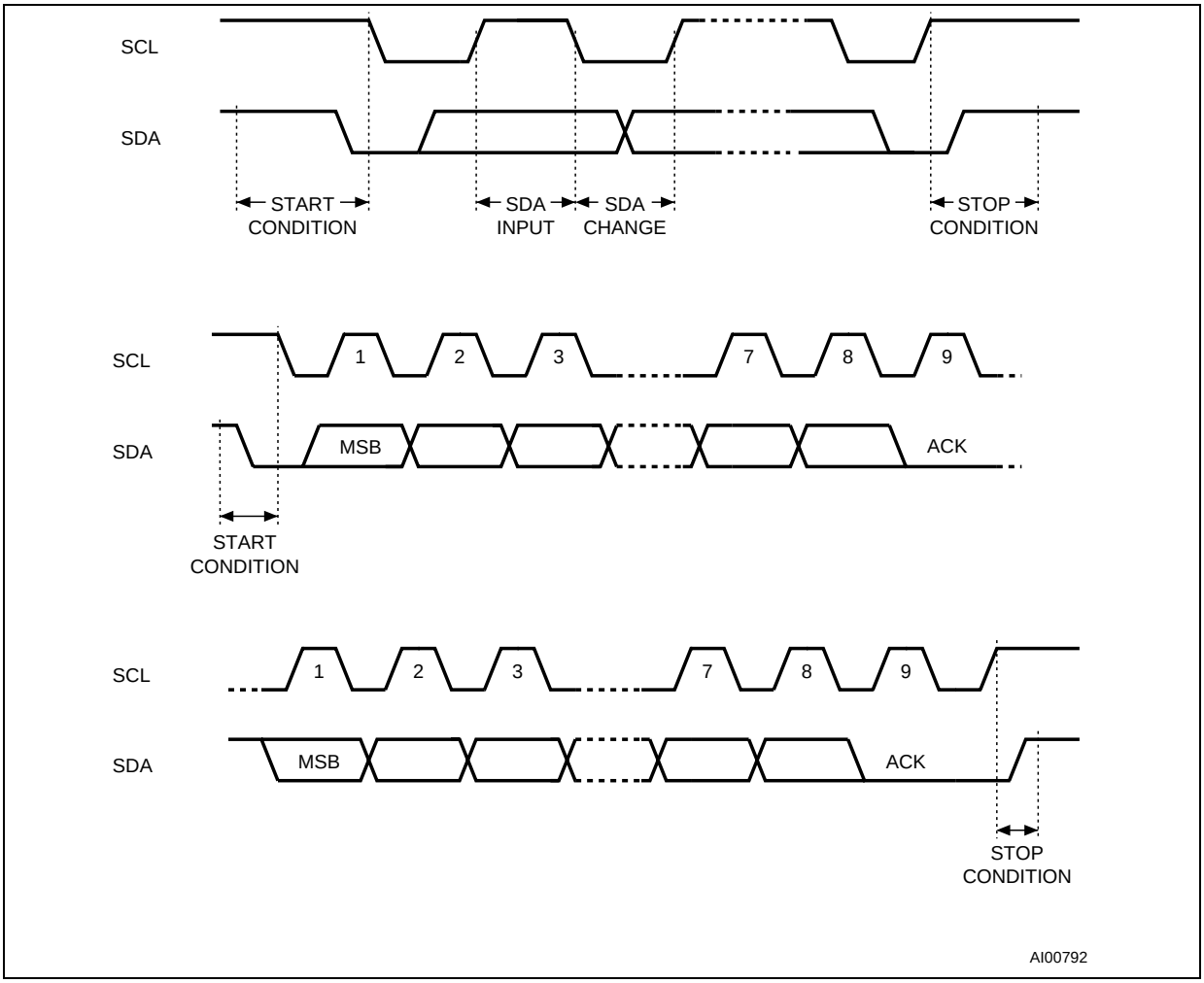


Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b12 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the memory. After each byte is transferred, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter "roll-over" which could result in data being overwritten.

Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the Memory will not respond to any request.

Figure 8. I²C Bus Protocol



Write to the Control Register

The control register is accessed using a specific Device Select Byte (as described in Table 3, and as shown in Table 11 and Table 12).

Table 11. Content of the Control Register

b7	b6	b5	b4	b3	b2	b1	b0
CRWD	WCpol	X	B2	B1	B0	X	X

Table 12. Default values

b7	b6	b5	b4	b3	b2	b1	b0
0	0	X	0	0	0	X	X

The meanings of the bits in Table 11 can be summarised as follows:

WCpol. This bit controls the polarity of the WC input (to switch pin 7 between being a WC or $\overline{WC}$ input). The default (initial) state of this bit is 0.

Table 13. Operation of the WCpol Bit

	pin 7 = high	**pin 7 = low**
WCpol = 0	Whole EEPROM and OTP page are write protected	Write instructions are allowed in the EEPROM area, and the OTP page can be written once
WCpol = 1	Write instructions are allowed in the EEPROM area, and the OTP page can be written once	Whole EEPROM and OTP page are write protected

CRWD. This is the Control Register Write Disable bit. When it is 0, pin 3 is a Don't Care input, and the control register is always writable. This is the default (initial) condition of this bit.

Table 14. Operation of the CRWD Bit

	pin 3 = high	**pin 3 = low**
CRWD = 0	Control register is writable	
CRWD = 1	Control register is writable	Control register is write protected (read only)

B2,B1,B0. These bits control the size of the ROM block. Their initial, default state is 0, 0, 0.

Table 15. Operation of the B2, B1 and B0 Bits

B2,B1,B0		**ROM block size and location**
0,0,0	0	All bits are EEPROM
0,0,1	1/64	ROM block=00h to 01FFh (512)
0,1,0	1/32	ROM block=00h to 03FFh (1K)
0,1,1	1/16	ROM block=00h to 07FFh (2K)
1,0,0	1/8	ROM block=00h to 0FFFh (4K)
1,0,1	1/4	ROM block=00h to 1FFFh (8K)
1,1,0	1/2	ROM block=00h to 3FFFh (16K)
1,1,1	1	All bits are ROM

In all cases, except when (B2,B1,B0)=(0,0,0), the selected area of EEPROM becomes read only (Write Protected) regardless of the status of the other bits and pins. However, the Control Register itself remains alterable in accordance with the status of $\overline{WC}$, WCpol, $\overline{WCR}$ and CRWD.

Write to the OTP Page

The OTP page is accessed by addressing the device using the specific, Device Select Byte (as described in Table 3).

The correct sequence for this instruction can be sketched out as follows:

```
Start
OTP Page Select(= 1010 0010)
Ack
Address (MSB) (= xxxx 0000)
Ack
Address (LSB) (= 0000 0000)
Ack
Data          (= byte to be written)
Ack
........
Data          (= byte to be written)
Ack
Stop
```

If one bit of the OTP Page Select differs from the above values, the OTP Page Select will NOT be acknowledged and the WRITE instruction will be ignored.

If one bit of the Address bytes (excluding the three most significant bits which are Don't Care) differs from the above values, the Address will be acknowledged, data will not be acknowledged and the WRITE instruction will be ignored.

The Page Write instruction must start with the first byte that is located in the OTP page (address 0h), otherwise the instruction will be ignored.

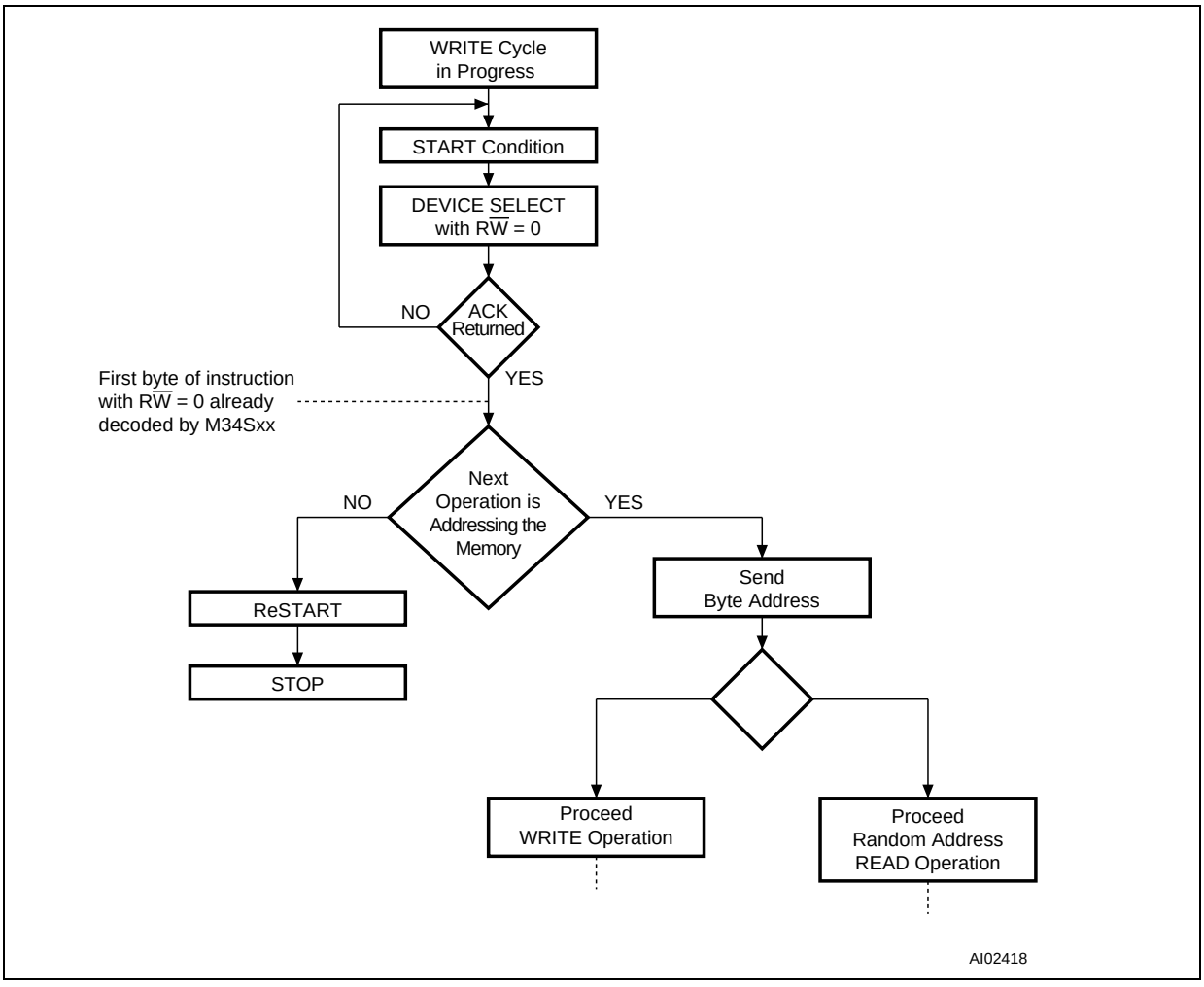
The first Write to the OTP page (whether it be a 1-byte write, a 32-byte page write, or some size in between) will disable any further write in the OTP page.

Let us suppose that byte N of the OTP page has just been addressed (for example because of a Write in the OTP page or a Random read in the OTP page). If the next instruction uses the Current Read Mode of the device, the first byte read in EEPROM will be in page 0, at address N+1 (or page 1, byte 0 if the last OTP byte addressed was at location 31).

Example of a correct sequence, leading to a 3-byte write in the OTP page:

```
Start
1010 0010     (OTP page select code)
Ack
1111 0000     (upper address, MSB)
Ack
0000 0000     (lower address, LSB)
Ack
0100 1101     (write 3 bytes of data)
Ack           (in the OTP page)
1100 1010
Ack
0101 0011
Ack
Stop
```

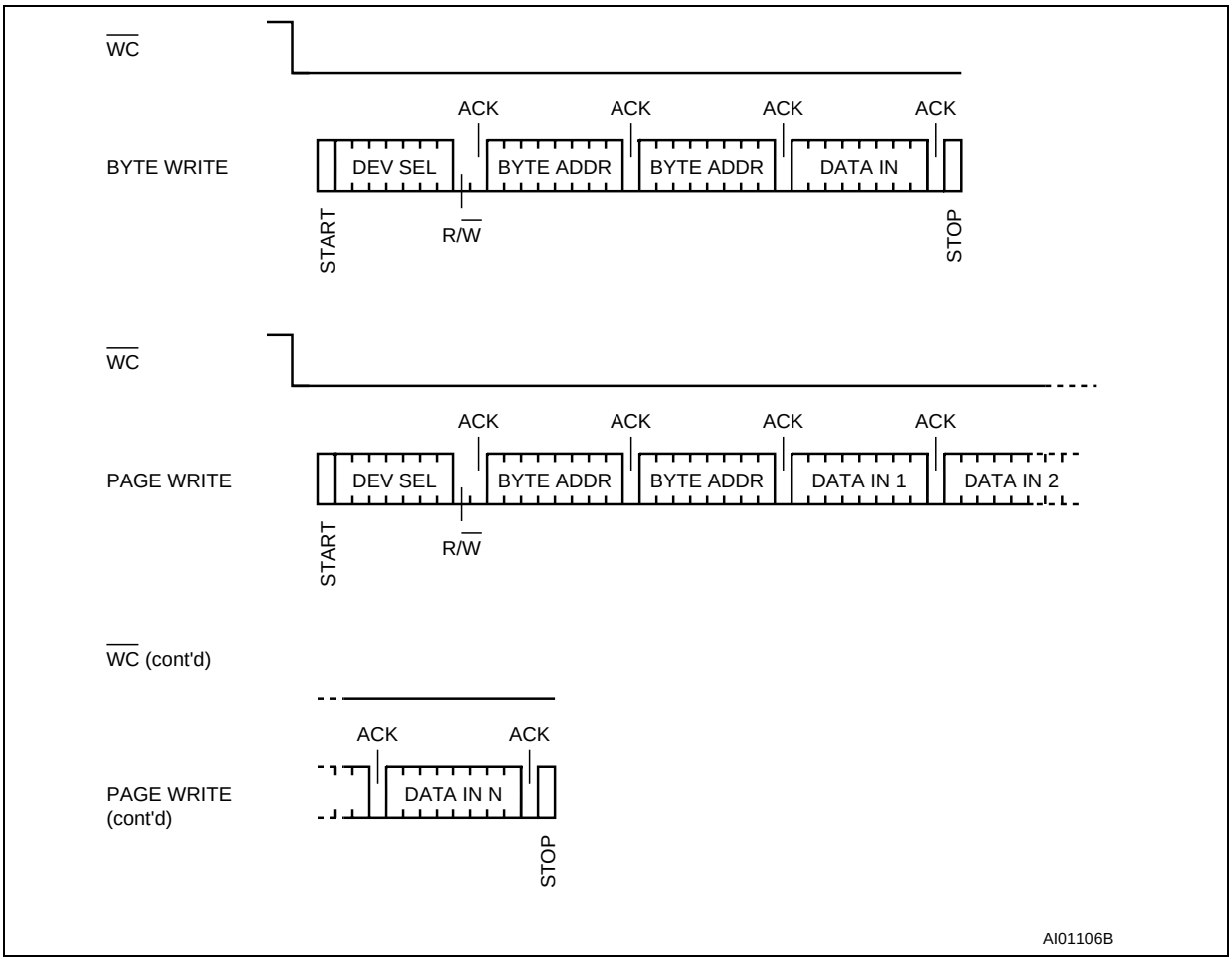
Figure 9. Write Cycle Polling using ACK



Example of an incorrect sequence, disabling the Write in the OTP page:

```
Start
1010 0010     (OTP page select code)
Ack
xxxx 0000     (MSB address)
Ack
0000 0100     (incorrect LSB address)
Ack           (acknowledged, but...)
0100 1101     (the attempts at)
(no ack)      (writing data to the)
1100 1010     (OTP page are)
(no ack)      (not acknowledged)
0101 0011
(no ack)
Stop
```

Figure 10. Write Modes Sequence with $\overline{WC}$ = 0 and WCpol = 0



Note: 1. The device has the same behavior when $\overline{WC}$ = 1 and WCpol = 1.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the memory disables itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

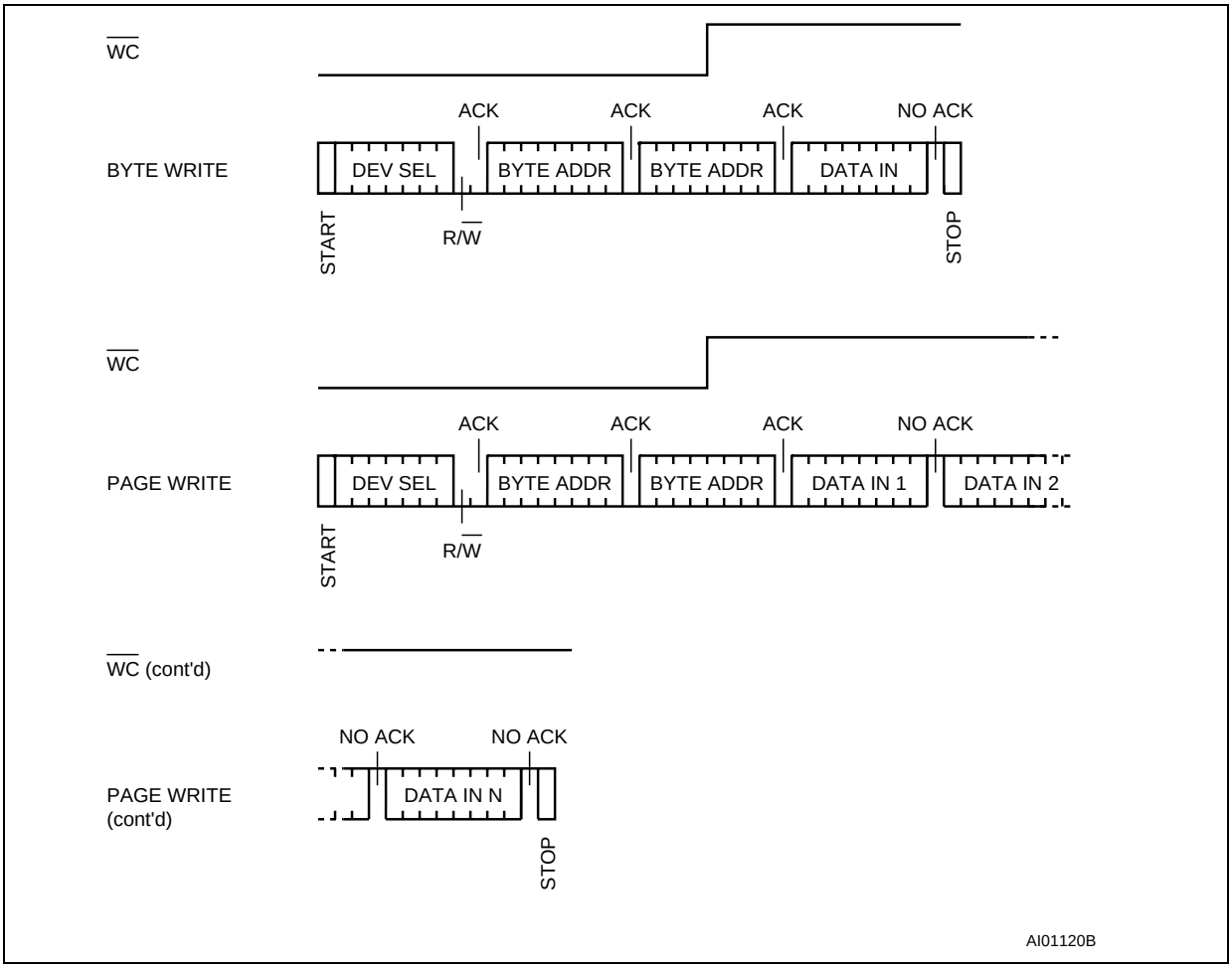
– Initial condition: a Write is in progress (see Figure 7).

– Step 1: the Master issues a START condition followed by a Device Select Byte. (1st byte of the new instruction)

– Step 2: if the memory is internally writing, no ACK will be returned. The Master goes back to Step1. If the memory has terminated the internal writing, it will issue an ACK.

The memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 11. Write Modes Sequence with $\overline{WC}$ = 1 and WCpol = 0



Note: 1. The device has the same behavior when $\overline{WC}$ = 0 and WCpol = 1.

Read Operations

On delivery, the memory content is set at all “1”s (or FFh).

Current Address Read. The memory has an internal address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select Byte with the R$\overline{W}$ bit set to 1. The memory acknowledges this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

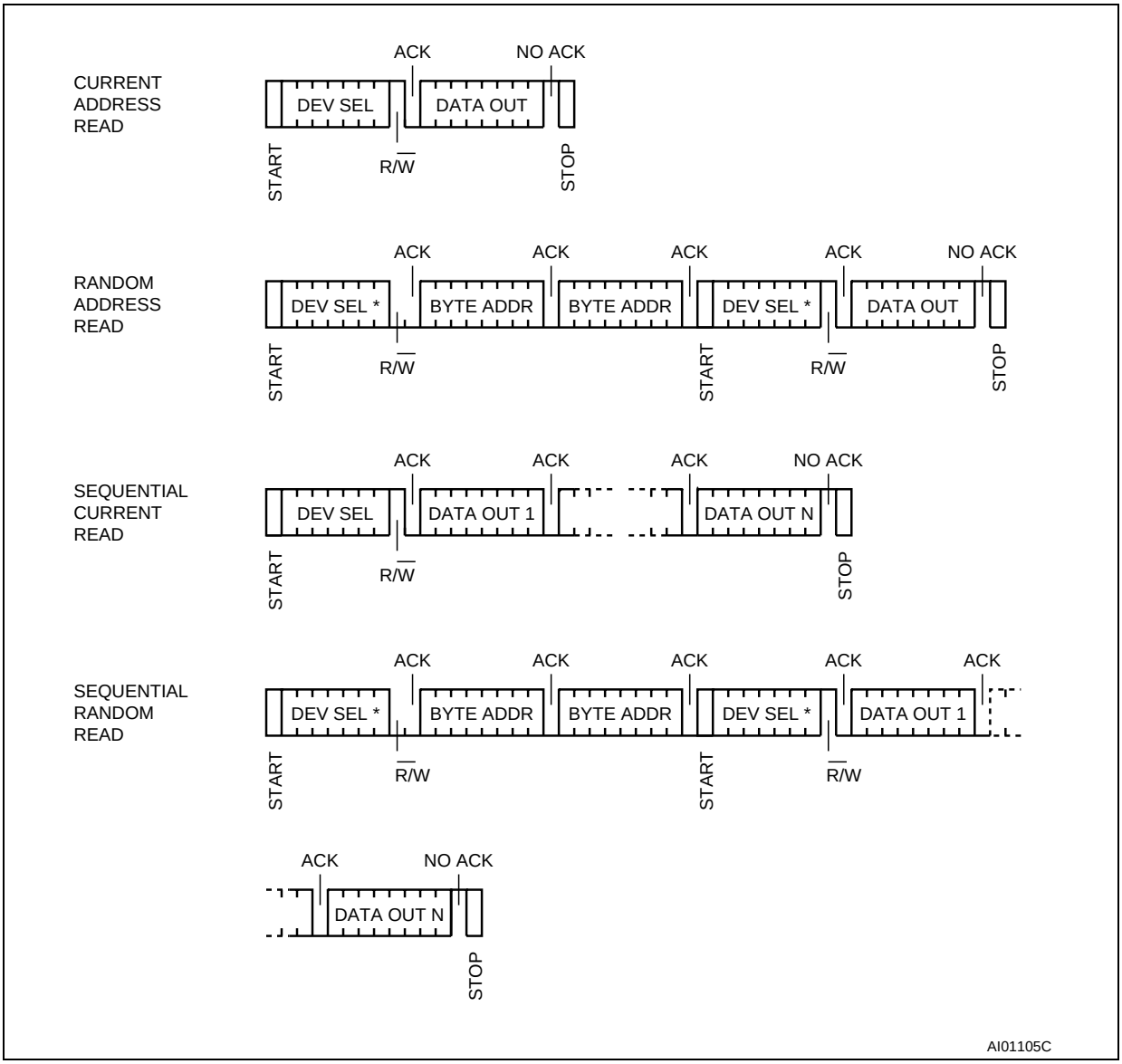
A Current Address Read in the OTP page is performed by sending the appropriate Device Select Byte, as described in Table 3.

Let us suppose, again, that byte N of the OTP page has just been addressed (for example because of a Write in the OTP page or a Random read in the OTP page). If the next instruction uses the Current Address Read Mode of the device, the first byte read in EEPROM will be in page 0, at address N+1 (or page 1, byte 0 if the last OTP byte addressed was at location 31).

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R$\overline{W}$ bit set to 1. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Specific features of the Random Address read in the OTP page. This instruction must consist of the two sequences shown on page 14 (Sequence A followed by Sequence B).

Figure 12. Read Mode Sequences



Note: 1. The seven most significant bits of the DEV SEL code of a Random Read (1st byte and 4th byte) must be identical.

```
Sequence A:
  Start
  OTP Page Select(= 1010 0010)
  Ack
  Address MSB   (= xxxx 0000)
  Ack
  Address LSB   (= 000x xxxx)
  Ack
Sequence B:
  Start
  OTP Page Select(= 1010 0011)
  Ack
  Data
  Ack
  ........
  Data
  (no Ack)
  Stop
```

If one, or more bits of the Sequence A differ from the above values, the bytes that follow it will be acknowledged (or not) according to the same rules as for the WRITE IN OTP, and the RANDOM ADDRESS READ IN OTP will be ignored.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition.

The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will “roll-over” and the memory will continue to output data.

A Sequential Read in the OTP page is performed by sending the appropriate Device Select Byte, as described in Table 3. If a sequential read reaches the last location in the OTP page (address 1Fh), subsequent Sequential Reads will wrap round to the start, to address 00h.

Acknowledge in Read Mode. In all read modes the memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to a stand-by state.

APPLICATION HINTS ON HOW TO USE THE CONTROL REGISTER TOGETHER WITH THE / WCR PIN

The application board can be designed in such a way that $\overline{WCR}$ pin is connected to V_{SS} (directly or through a pull-down resistor). It should be noted that the $\overline{WCR}$ pin features an internal pull-down resistor allowing this input to be left unconnected. With such a P.C.B. (Printed Circuit Board), the device can be initialised according to following set-up sequence :

1. Write the data that is to be Write protected:
   - Write data in the area starting from address 00h up to the desired address.
2. Write in the Control Register (single byte write using the following bits):
   - Set B2, B1 and B0 values according to the ROM block size (as defined in Table 15)
   - Set WCpol according to the application needs.
   - Set CRWD bit to 1

Once the CRWD bit is set to 1, the control register becomes Write Protected. The only way to write again to the Control Register is to set the $\overline{WCR}$ pin high. This is possible by applying V_{CC} to $\overline{WCR}$ if it was previously floating or connected to V_{SS} through an external pull-down resistor. If $\overline{WCR}$ is shorted to V_{SS}, the device needs to be de-soldered from the PCB.

OTHER NOTES

The $\overline{WCR}$ pin has an internal pull-down resistor. Connecting this pin to GND does not affect the power consumption, thus giving the M34S32 its lowest power consumption when it is in Protected mode.

The OTP page may be programmed before or after the hardware protected mode has been set (by setting the CRWD bit). This allows the application MCU to program the OTP page either on the assembly line or during the operating life of the application.

The $\overline{WC}$ pin (but not the $\overline{WCR}$ pin) may be driven dynamically by the MCU to increase the immunity to data corruption of the unprotected EEPROM area. This pin may alternatively be pulled to V_{CC} or GND (depending on which is appropriate, according to the setting of the WCpol bit).

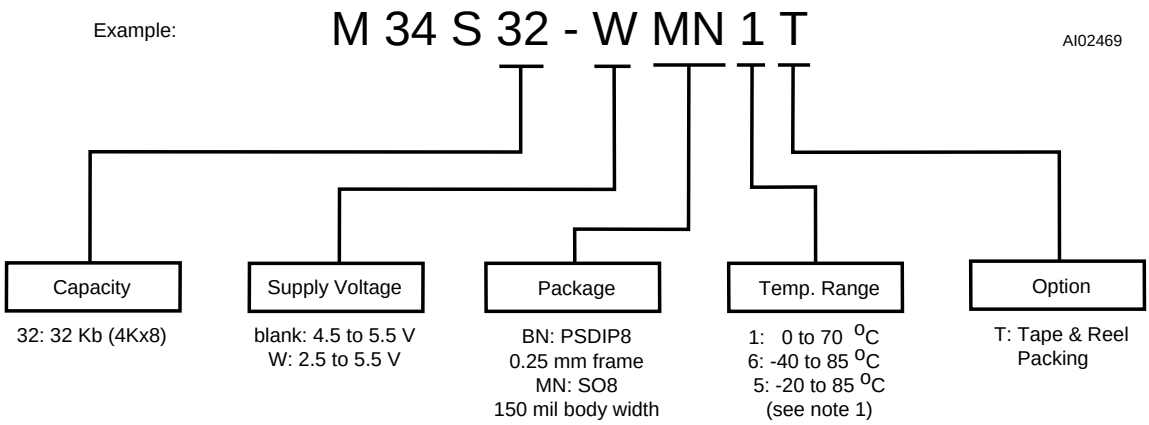
ORDERING INFORMATION SCHEME

Devices are shipped from the factory with the memory content set at all “1”s (FFh).

For a list of available options, refer to the current *Memory Shortform Catalogue*.

For further information on any aspect of this device, please contact the ST Sales Office nearest to you.

In general, the fields of the product number are made up as follows:

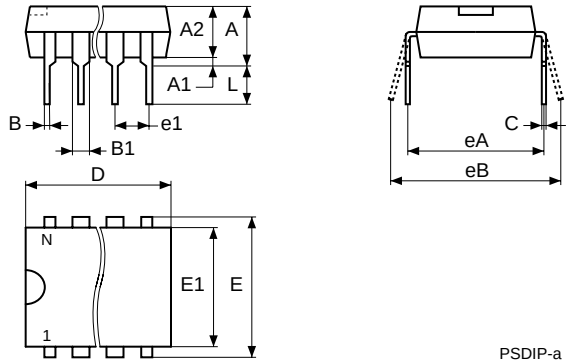


Note: 1. Temperature range 1 is available on request only.

Table 16. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 13. PSDIP8

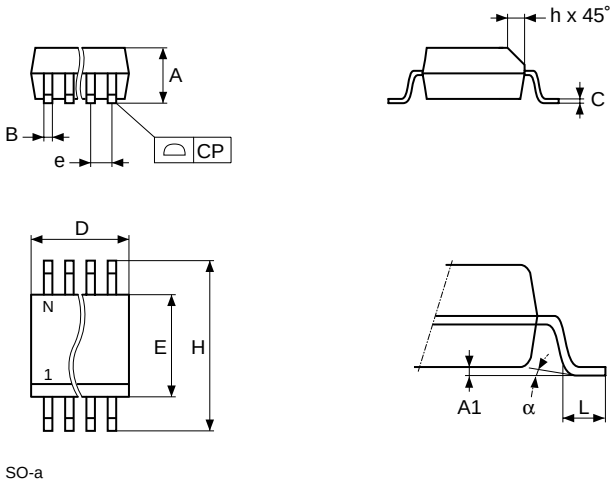


Note: 1. Note: Drawing is not to scale.

Table 17. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 14. SO8a



SO-a

Note: 1. Note: Drawing is not to scale.