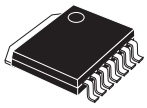
ST3L01

TRIPLE VOLTAGE REGULATOR

- DUAL INPUT VOLTAGE (12V AND 5V)
- TRIPLE OUTPUT VOLTAGE (2.6V, 3.3V, 8V)
- 2.6V GUARANTEED I_{OUT} UP TO 1.2A
- 3.3V GUARANTEED I_{OUT} UP TO 1.0A
- 8V GUARANTEED I_{OUT} UP TO 200mA
- THERMAL AND SHORT CIRCUIT PROTECTION
- GUARANTEED OPERATING TEMPERATURE RANGE (0°C to 125°C)

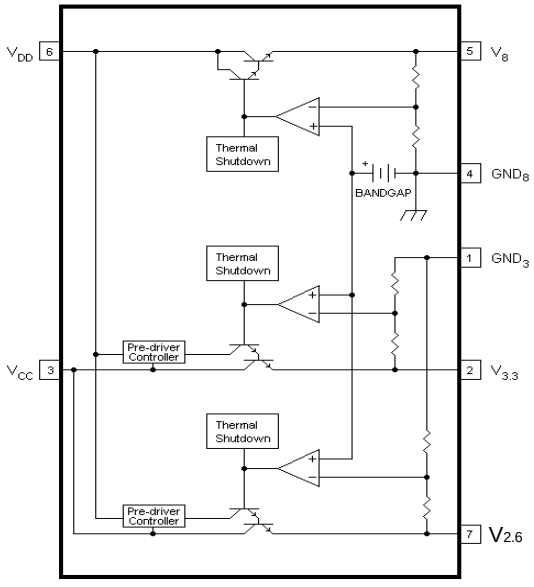


SPAK-7L
(PowerFlex™)

DESCRIPTION

This device contains three voltage regulators, all fixed output voltage, in one 7 pin surface mount package. The first is a 2.6 V regulator to power the integrated controller/µP. The second is a 3.3V regulator to power the read channel chip, and memory chips requiring 3.3V The last is an 8V regulator to power the preamp chip. The bandgap reference, the 8V ground, and the substrate are all tied to a common ground pin, while the 2.6V and 3.3V ground is tied to a separate ground pin.This grounding scheme allows for improved noise isolation between the 8V regulator and the 2.6V and 3.3V regulators.The 2.6V and 3.3V regulators shall be respectively capable of 1.0A and 1.2A. The 8V regulator shall be capable of 200mA.
It is housed in the SPAK (PowerFlex™)

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
V_{DD}	ISupply Voltage	18	V
V_{ESD}	ESD Tolerance (Human Body Model)	4	KV
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_J	Operating Junction Temperature Range	0 to +150	°C

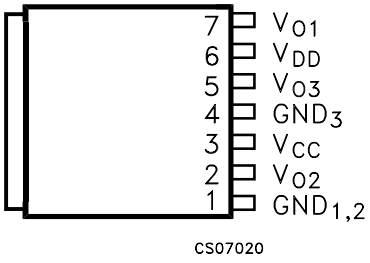
GENERAL OPERATING CONDITION

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} Supply Voltage	4.75 to 5.25	V
ΔV_{CC}	V_{CC} Ripple	±0.15	V
t_r	Rise Time (10% to 90%) referred to V_{CC}	1	V
t_f	Fall Time (90% to 10%) referred to V_{CC}	1	V
V_{DD}	V_{DD} Supply Voltage	10.8 to 13.2	V
ΔV_{DD}	V_{DD} Ripple	±0.3	V
t_r	Rise Time (10% to 90%) referred to V_{DD}	1	V
t_f	Fall Time (90% to 10%) referred to V_{DD}	1	V
T_{AI}	Operating Ambient Temperature Range	0 to 70	µs

THERMAL DATA

Symbol	Parameter	SPAK-7L	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	2	°C/W

CONNECTION DIAGRAM (top view)



SPAK-7L

PIN DESCRIPTION

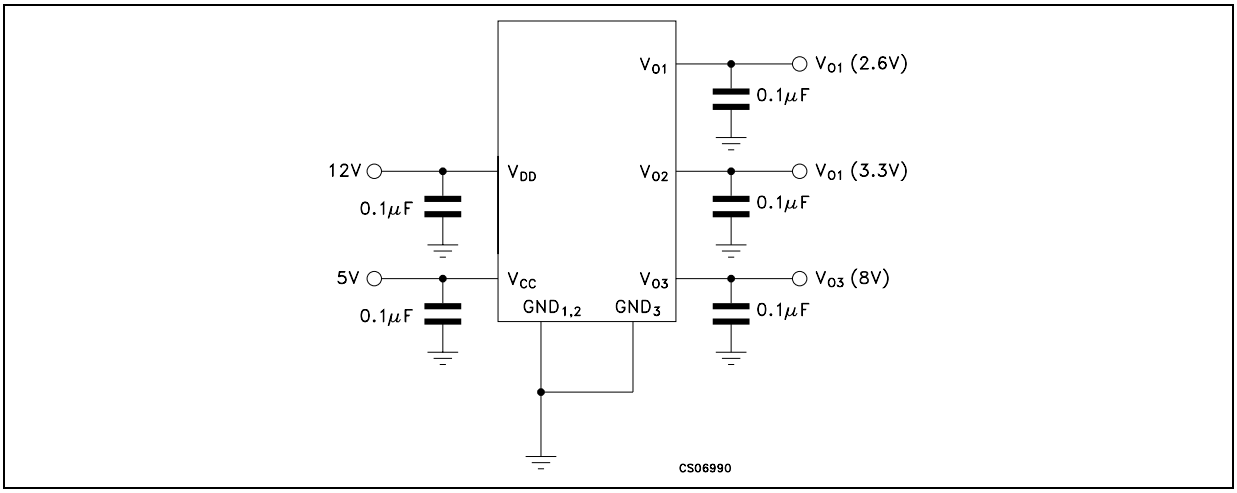
Pin N°	Symbol	Name and Function
1	$GND_{1,2}$	V_{O1} and V_{O2} regulators GND pin
2	V_{O2}	Second Output Pin: Bypass with a 0.1µF capacitor to GND
3	V_{CC}	Input Pin: Bypass with a 0.1µF capacitor to GND
4	GND_3	V_{O3} regulators GND pin
5	V_{O3}	Third Output Pin: Bypass with a 0.1µF capacitor to GND
6	V_{DD}	Input Pin: Bypass with a 0.1µF capacitor to GND
7	V_{O1}	First Output Pin: Bypass with a 0.1µF capacitor to GND

ORDERING INFORMATION

TYPE	SPAK (Power Flex™) 7 leads (*)
ST3L01	ST3L01K7

(*) Available in Tape & Reel with the suffix "R"

TYPICAL APPLICATION CIRCUIT



Note: To improve noise figure of the 8V VREG connect this capacitor to the GND_{8V} pin. C_{CC}, C_{DD}, C_{O1}, C_{O2} and C_{O3} capacitors must be located not more than 0.5" from the output pins of the device. Form more details about Capacitors read the "Application Hints"

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{DD}=12V, C_{CC}=1µF (Tantalum), C_{DD}=0.1µF (X7R), C_{O1}=C_{O2}=C_{O3}=0.11µF (X7R) T_j=0 to 125°C unless otherwise specified. Typical values are referred at T_j=25°C, I_{FL1} =1.2A, I_{FL2} =1.0A, I_{FL3} =0.2A,

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage 1	I_{O1} = 10mA T_j = 25°C	2.575	2.6	2.626	V
		I_{O1} = 0 to I_{FL1} V_{CC} = 4.75 to 5.25V T_j = 0 to 125°C	2.55	2.6	2.65	
		V_{DD} = 0 to 10.8V I_{O1} = 0.5A	2.2		2.65	
V_{O2}	Output Voltage 2	I_{O2} = 10mA T_j = 25°C	3.23	3.3	3.37	V
		I_{O2} = 0 to I_{FL2} V_{CC} = 4.75 to 5.25V T_j = 0 to 125°C	3.2	3.3	3.4	
		V_{DD} = 0 to 10.8V I_{O2} = 0.5A	2.92		3.4	
V_{O3}	Output Voltage 3	I_{O3} = 10mA T_j = 25°C	7.84	8	8.16	V
		I_{O3} = 0 to I_{FL3} V_{DD} = 10.8 to 13.2V T_j = 0 to 125°C	7.76	8	8.24	
ΔV_O	Line Regulation 1	I_O = 10mA V_{CC} =±5% V_{DD} =±10%		<0.2		$\%V_O$
ΔV_O	Load Regulation 1	I_O = 0.01 to I_{FL} (Note 1)		<0.4		$\%V_O$
V_{D1}	Dropout Voltage 1	I_{O1} = I_{FL1} (Note 2)		1.3	1.9	V
V_{D2}	Dropout Voltage 2	I_{O2} = I_{FL2} (Note 2)		1.13	1.4	V
V_{D3}	Dropout Voltage 3	I_{O3} = I_{FL3} (Note 2)		1.6	2.2	V
t_{TR}	Transient Response	(Note 3, 7)		<1		µs
I_{OL1}	Output 1 Current Limit	ΔV_O = 125mV	1.5	2.1	2.5	A
I_{OL2}	Output 2 Current Limit	ΔV_O = 165mV	1.1	1.7	2.5	A
I_{OL3}	Output 3 Current Limit	ΔV_{OUT} = 400mV	0.25	0.4	0.5	A
I_{O1}	Output 1 Minimum Load Current	(Note 4, 7)			0	mA
I_{O2}	Output 2 Minimum Load Current	(Note 4, 7)			0	mA
I_{O3}	Output 3 Minimum Load Current	(Note 4, 7)			0	mA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_O	Output Capacitor	(Note 5, 7)	0.1			µF
C_{CC}	Input Capacitor	(Note 5)	1.0			µF
C_{DD}	Input Capacitor	(Note 5)	0.1			µF
Reg_{Therm}	Therma Regulation	$I_{OUT} = I_{FL}$, t_{PULSE} = 30ms (Note 7)		0.1	0.3	%/W
SVR1	Supply Voltage Rejection (V_{CC} to Output 1)	B = 100Hz to 100KHz $I_{O1} = I_{FL1}/10$ V_{CC} = 4.75 to 5.25V (Note 7)	30	>40		dB
SVR2	Supply Voltage Rejection (V_{CC} to Output 2)	B = 100Hz to 100KHz $I_{O2} = I_{FL2}/10$ V_{CC} = 4.75 to 5.25V (Note 7)	30	>40		dB
SVR3	Supply Voltage Rejection (V_{DD} to Output 3)	B = 100Hz to 100KHz $I_{O3} = I_{FL3}/10$ V_{DD} = 10.8 to 13.2V (Note 7)	40	>50		dB
I_{VCC}	V_{CC} Quiescent Current	$I_{O1} = I_{O2} = I_{O3} = 0$		7	10	mA
I_{VDD}	V_{DD} Quiescent Current	$I_{O1} = I_{O2} = I_{O3} = 0$		13	20	mA
eN	Output Noise	B = 10Hz to 10KHz (Note 7)		0.003		$\%V_{OUT}$
ΔV_O	Temperature Stability	I_O = 10mA (Note 6, 7)		0.5		$\%V_{OUT}$
ΔV_O	Long Term Stability	T_j = 125°C, 1000Hrs (Note 7)		0.3		$\%V_{OUT}$

Note 1: Low duty cycle pulse testing with Kelvin connections are required in order to maintain accurate data

Note 2: Dropout Voltage is defined as the minimum differential voltage between V_I and V_O required to mantain regulation at V_O. It is measured when the output voltage drops 100mV below its nominal value.

Note 3: Transient response is defined with a step change in load from 10mA to $I_{FL}/2$ as the time from the load step until the output voltage reaches it's minimum value.

Note 4: Minimum load current is defined as the minimum current required at the output in order to maintain regulation for the output voltage.

Note 5: The regulator shall withstand 100000 reverse bias discharges of the maximum output capacitance, with no degradation, when the input voltage is switched to ground in 1 µs.

Note 6: Temperature stability is the change in output from nominal over the operating temperature range.

Note 7: Guaranteed by design, not tested in production.

APPLICATION HINTS

EXTERNAL CAPACITORS

The ST3L01 requires external capacitors for stability. We suggest to solder both capacitors as close as possible to the relative pins.

INPUT CAPACITORS

An input capacitor, whose value is at least 0.1µF, is required on the V_{DD} input; the amount of the input capacitance can be increased without limit. Any good quality tantalum or ceramic low ESR capacitor may be used at the V_{DD} input.

Any input capacitor, whose value is at least 1_mF is instead required on the V_{CC} input; the amount of this input capacitance can be increased without limit. Tantalum or aluminum electrolitic capacitor can be used at the V_{CC} input; ceramic, low ESR capacitor are not recommended.

Both capacitors must be located at a distance of not modre than 0.5" from the input pins of the device and returned to a clean analog ground.

OUTPUT CAPACITOR

The ST3L01 is designed specifically to work with Ceramic and Tantalum capacitors.

The test results of the ST3L01 stability using multilayer ceramic capacitors show that a minimum value of 0.1µF is needed for the three regulators. This value can be increased for even better transient response and noise performance.

Surface-mountable solid tantalum capacitors offer a good combination of small physical size for the capacitance value and ESR in the range need by the ST3L01. The test results show good stability for both outputs with values of at least 0.1µF. Also this capacitor value can be increased without limit for even better performance such a transient response and noise.

IMPORTANT; The output capacitor must maintain its ESR in the stable region over the full operating temperature to assure stability. Also , capacitor tolerance and variation with temperature must be considered to assure that the minimum amount of capacitance is provided at all times. For this reason, when a caramic multilayer capacitor is used, the better choise for temperature coefficent is the X7R type, which holds the capacitance within ±15% . The output capacitor should be located not more than 0.5" from the output pins of the device and returned to a clean analog ground.

TYPICAL CHARACTERISTICS (C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R))

Figure 1 : Output Voltage vs Temperature

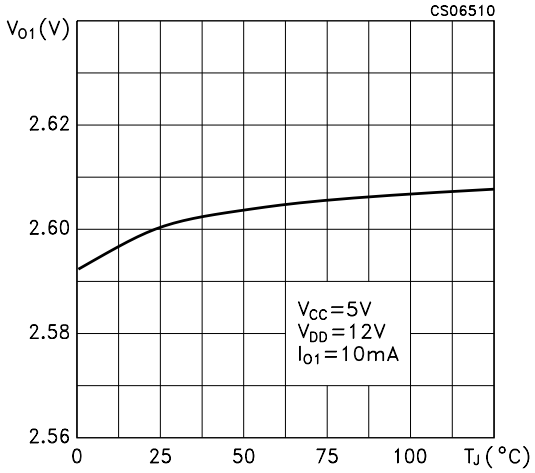


Figure 2 : Output Voltage vs Temperature

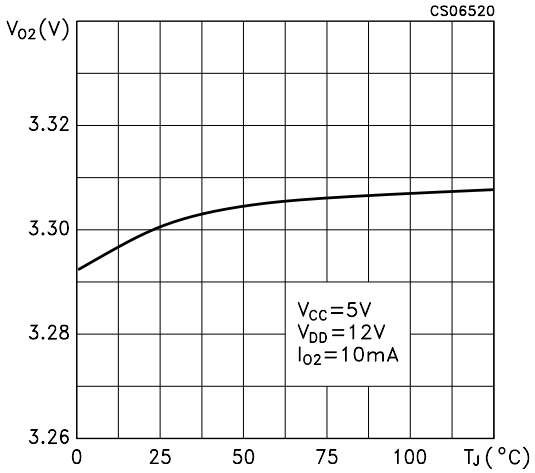


Figure 3 : Output Voltage vs Temperature

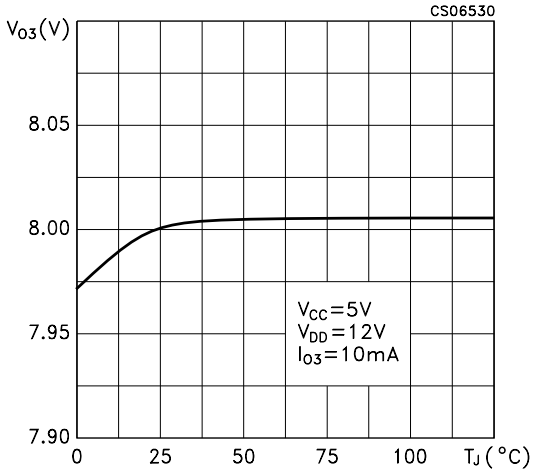


Figure 4 : Load Regulation vs Temperature

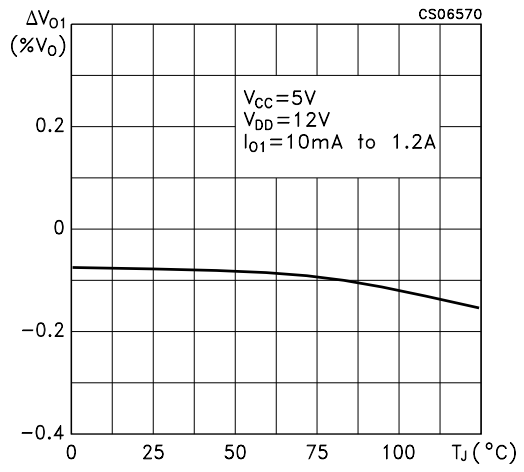


Figure 5 : Load Regulation vs Temperature

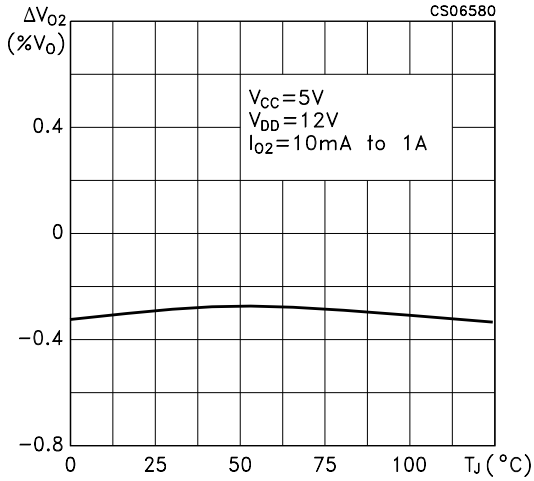


Figure 6 : Load Regulation vs Temperature

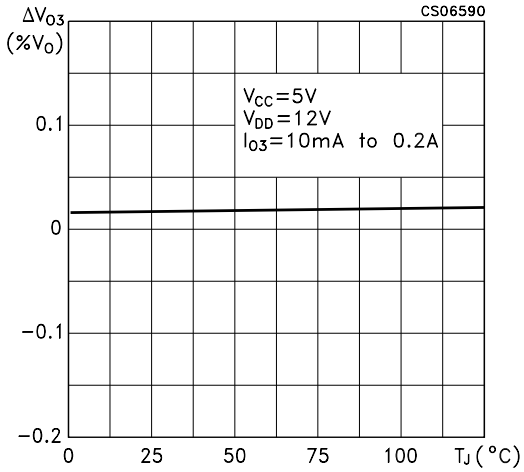


Figure 7 : Dropout Voltage vs Temperature

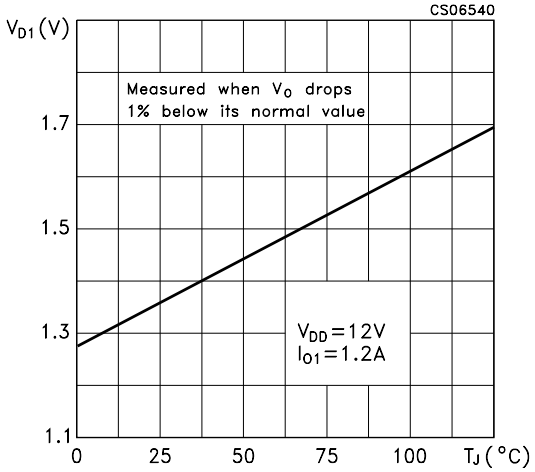


Figure 8 : Dropout Voltage vs Temperature

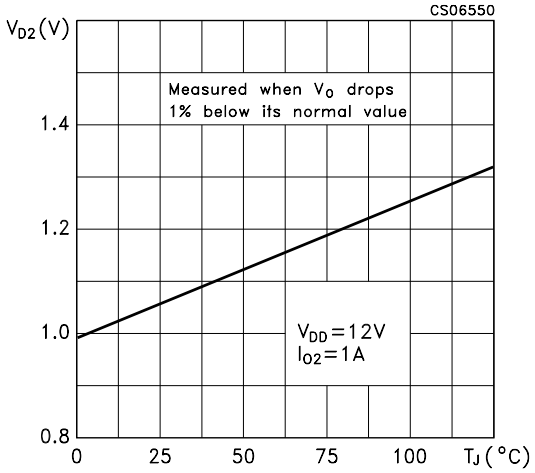


Figure 9 : Dropout Voltage vs Temperature

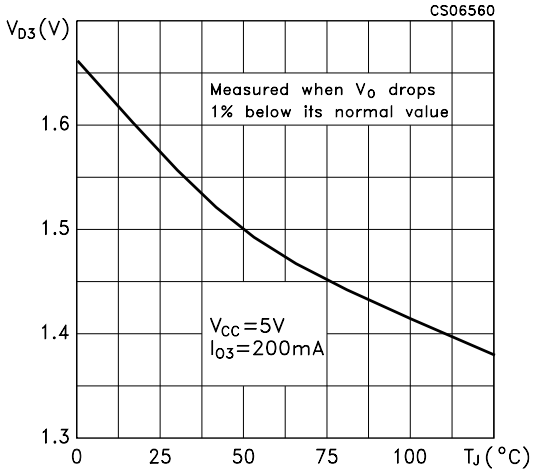


Figure 10 : Dropout Voltage vs Output Current

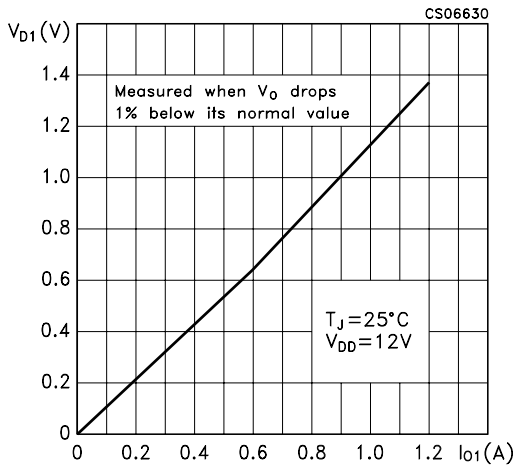


Figure 11 : Dropout Voltage vs Output Current

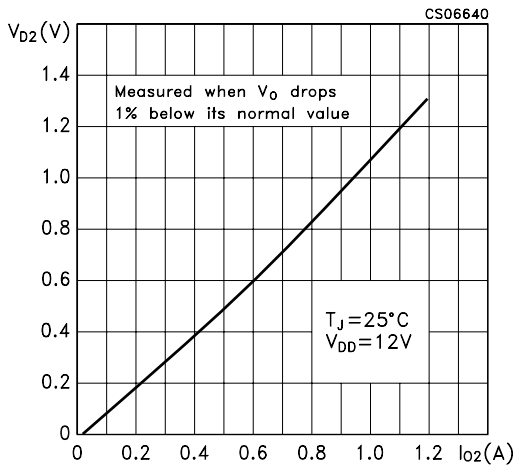


Figure 12 : Dropout Voltage vs Output Current

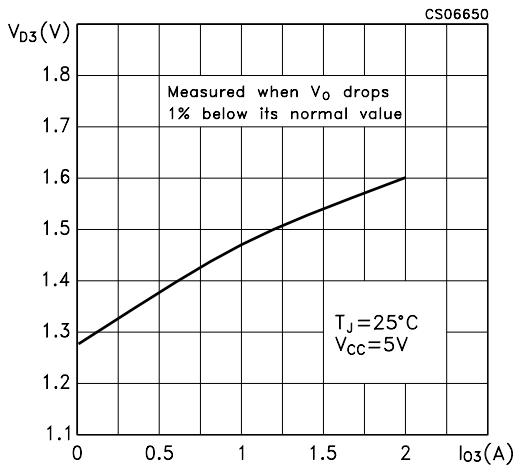


Figure 13 : Current Limit vs Temperature

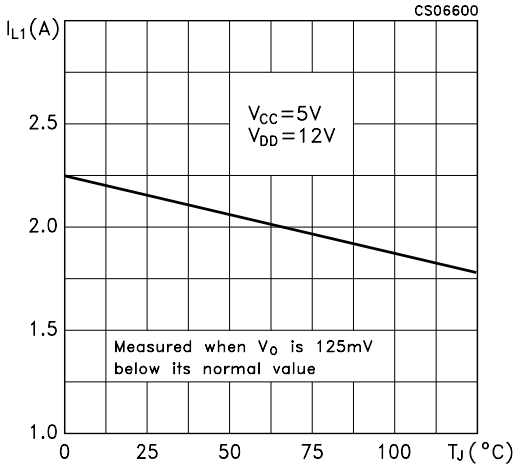


Figure 14 : Current Limit vs Temperature

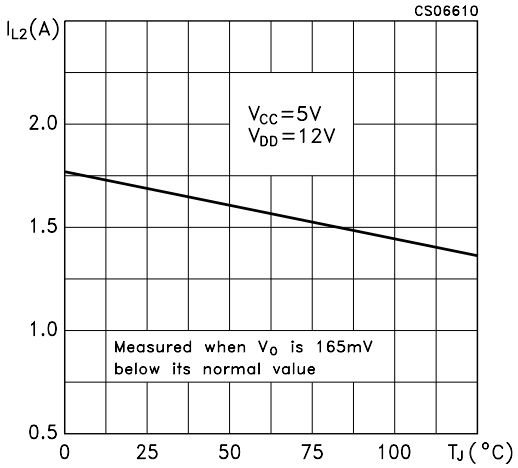


Figure 15 : Current Limit vs Temperature

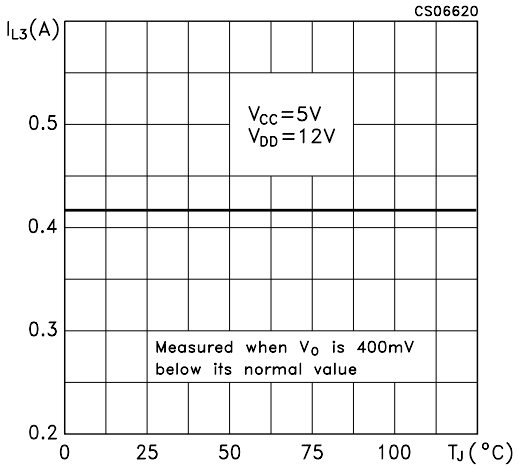


Figure 16 : Output Voltage vs Output Current

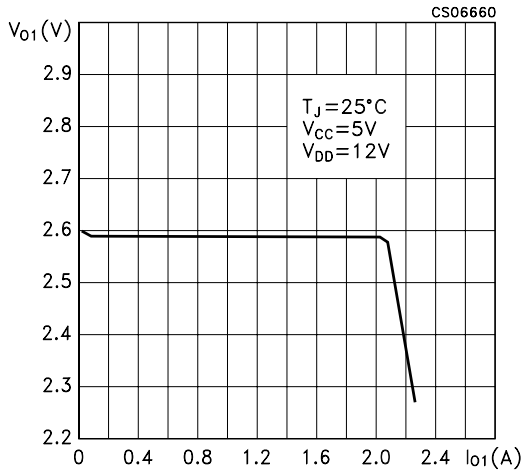


Figure 17 : Output Voltage vs Output Current

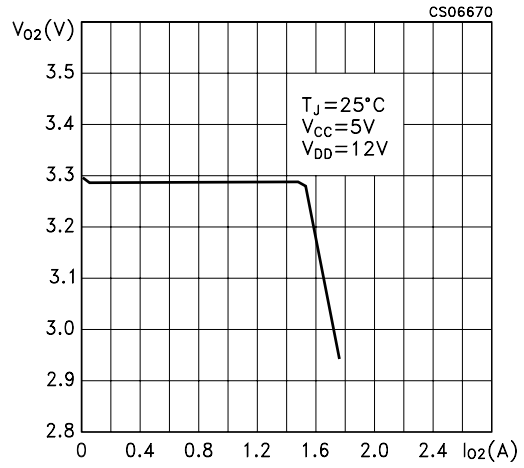


Figure 18 : Output Voltage vs Output Current

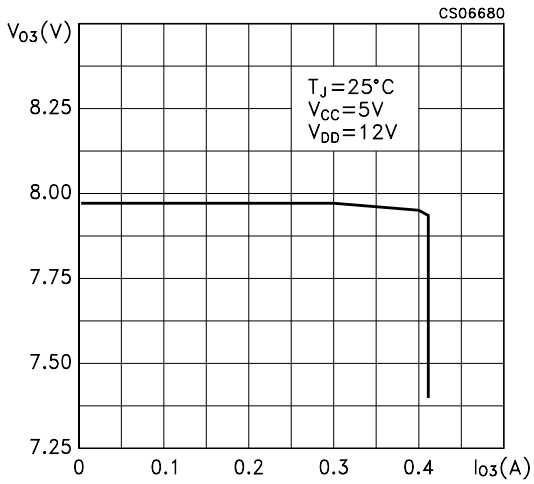


Figure 19 : Quiescent Current vs Temperature

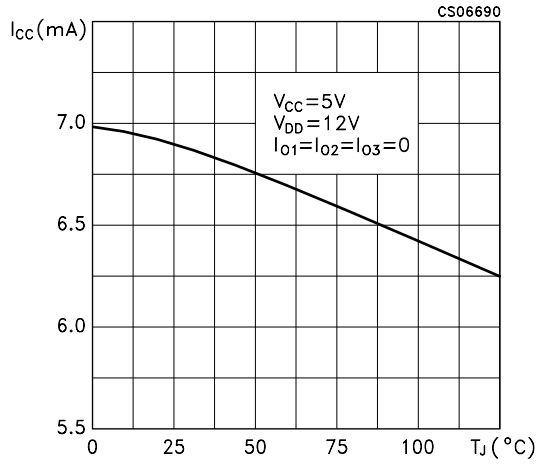


Figure 20 : Quiescent Current vs Temperature

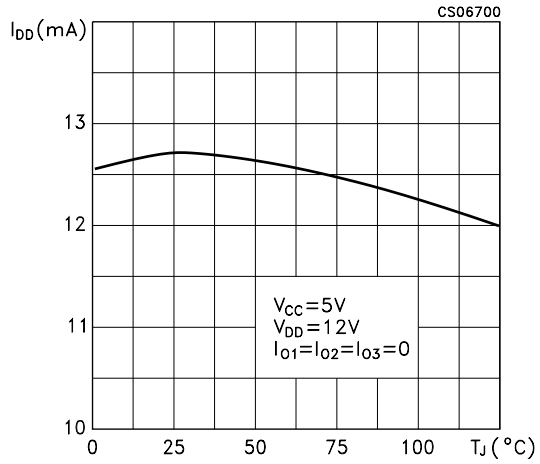


Figure 21 : Supply Voltage Rejection vs Frequency

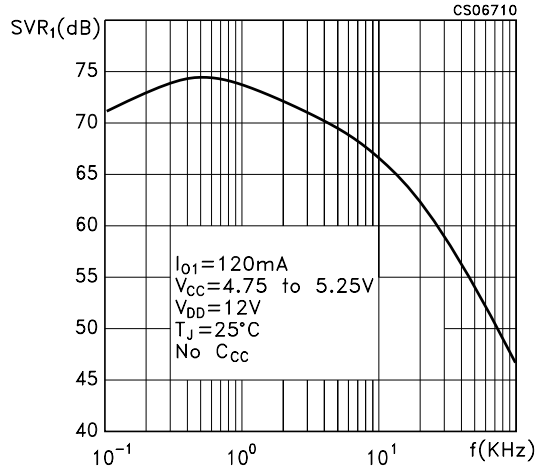


Figure 22 : Supply Voltage Rejection vs Frequency

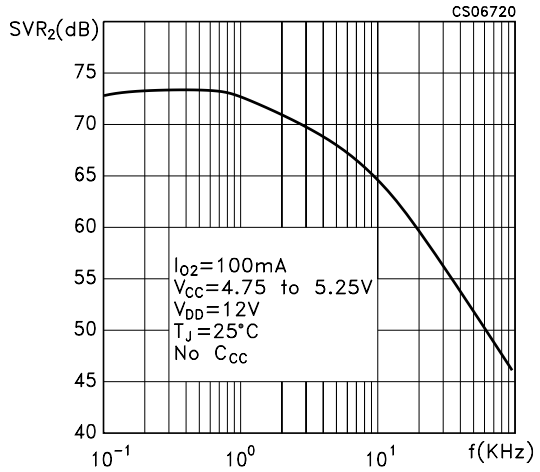


Figure 23 : Supply Voltage Rejection vs Frequency

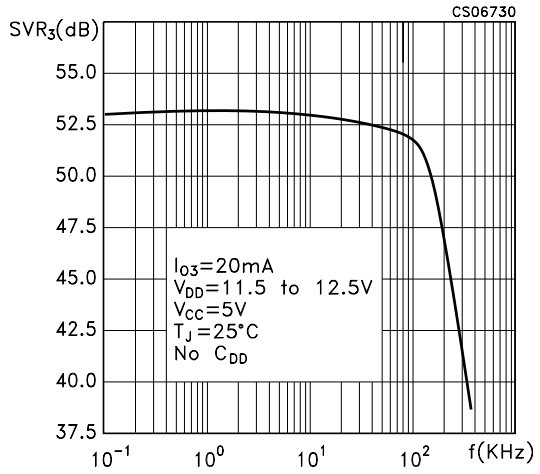


Figure 24 : Supply Voltage Rejection vs Output Current

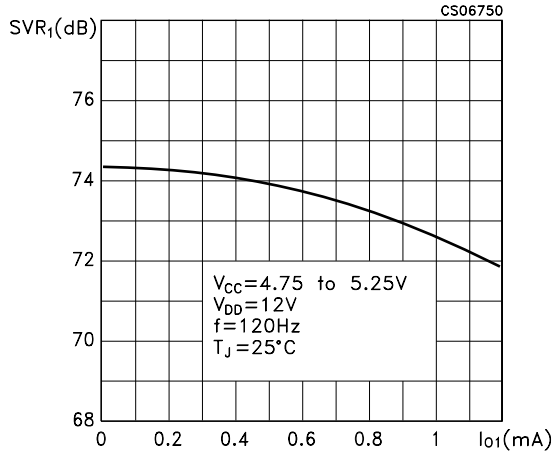


Figure 25 : Supply Voltage Rejection vs Output Current

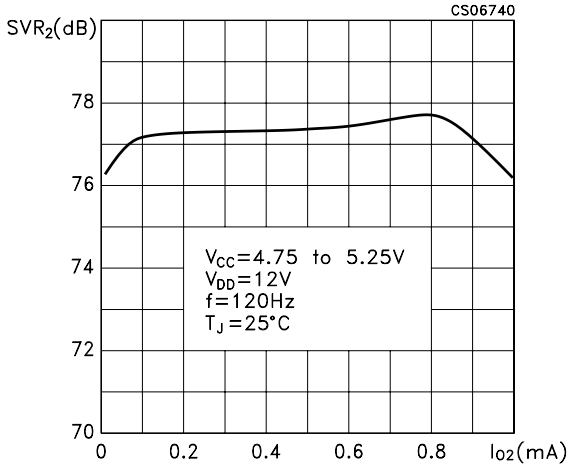


Figure 26 : Supply Voltage Rejection vs Output Current

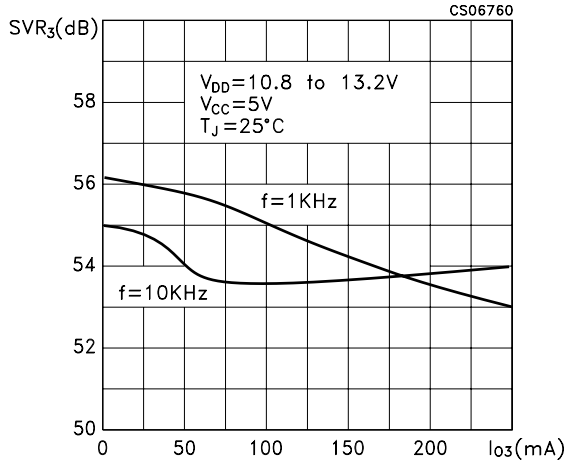


Figure 27 : Supply Voltage Rejection vs Temperature

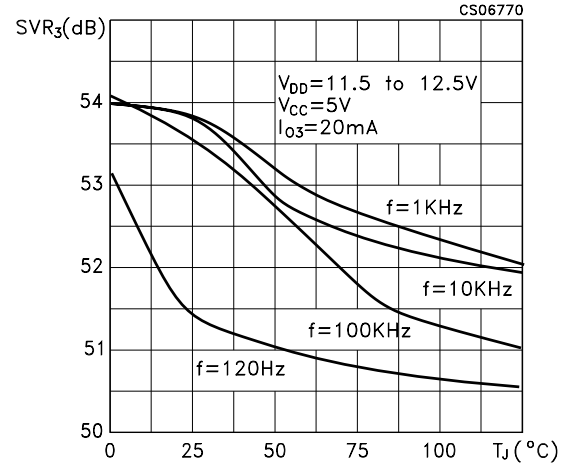
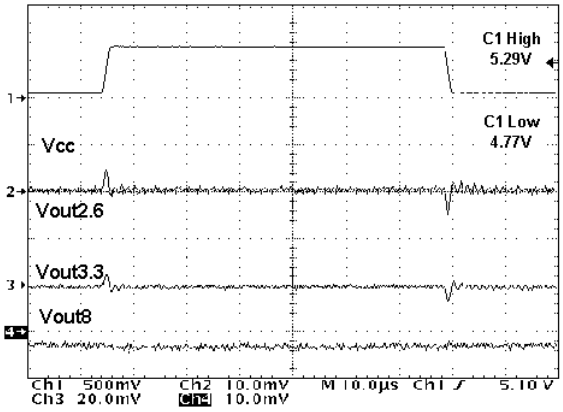
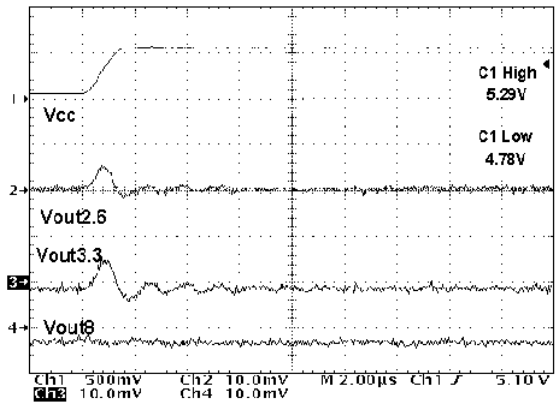


Figure 28 : Line Transient



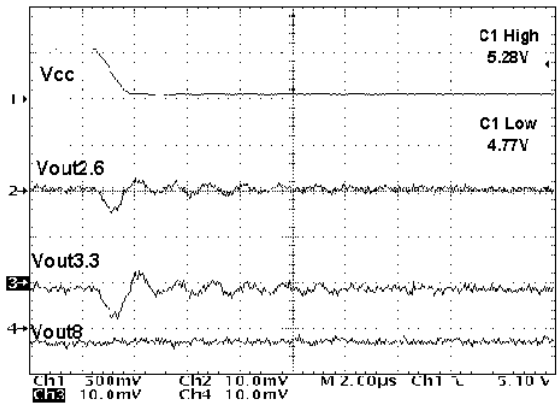
V_{CC}=4.75 to 5.25V, V_{DD}=12V, I_{O1}=I_{O2}=10mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 29 : Line Transient



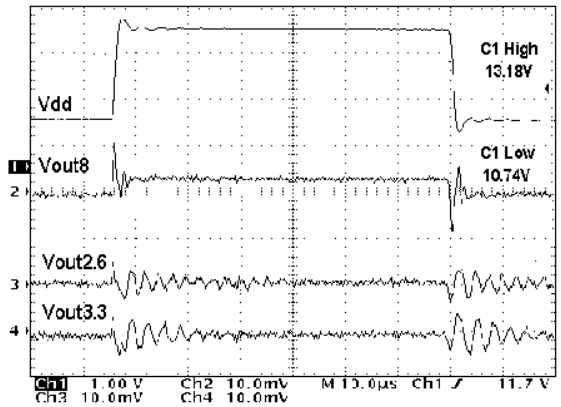
V_{CC}=4.75 to 5.25V, V_{DD}=12V, I_{O1}=I_{O2}=10mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 30 : Line Transient



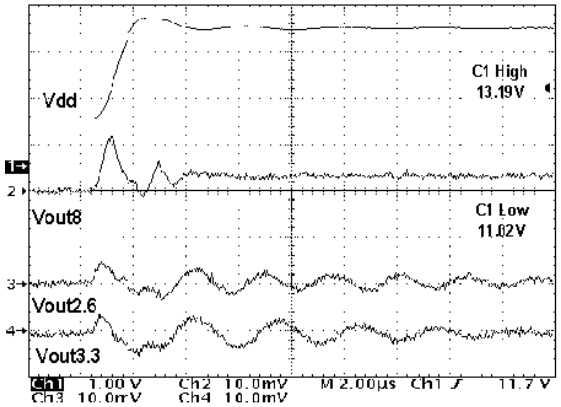
V_{CC}=4.75 to 5.25V, V_{DD}=12V, I_{O1}=I_{O2}=10mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 31 : Line Transient



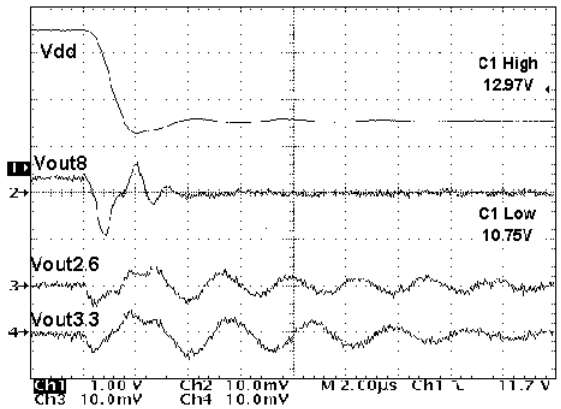
V_{CC}=5V, V_{DD}=10.7 to 13.2V, I_{O3}=10mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 32 : Line Transient



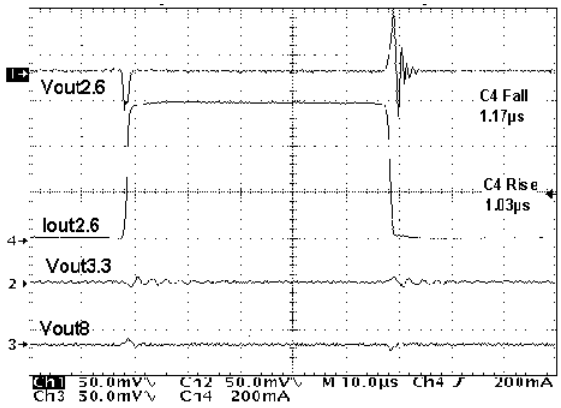
V_{CC}=5V, V_{DD}=10.7 to 13.2V, I_{O3}=10mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 33 : Line Transient



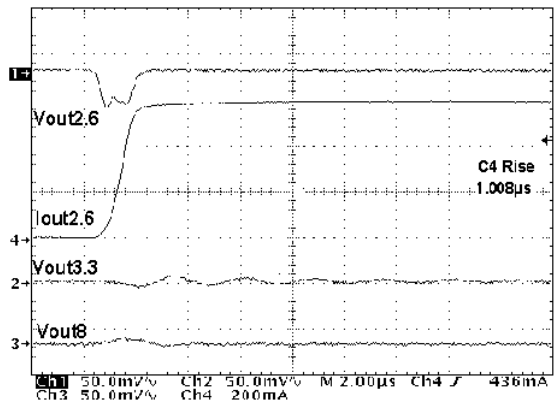
V_{CC}=5V, V_{DD}=10.7 to 13.2V, I_{O3}=10mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 34 : Load Transient



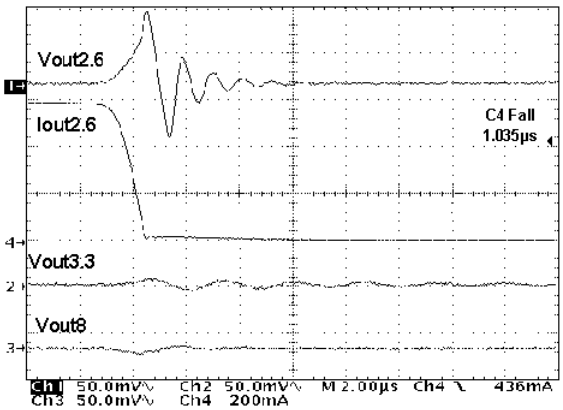
V_{CC}=5V, V_{DD}=12V, I_{O1}=10 to 600mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

Figure 35 : Load Transient



V_{CC}=5V, V_{DD}=12V, I_{O1}=10 to 600mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

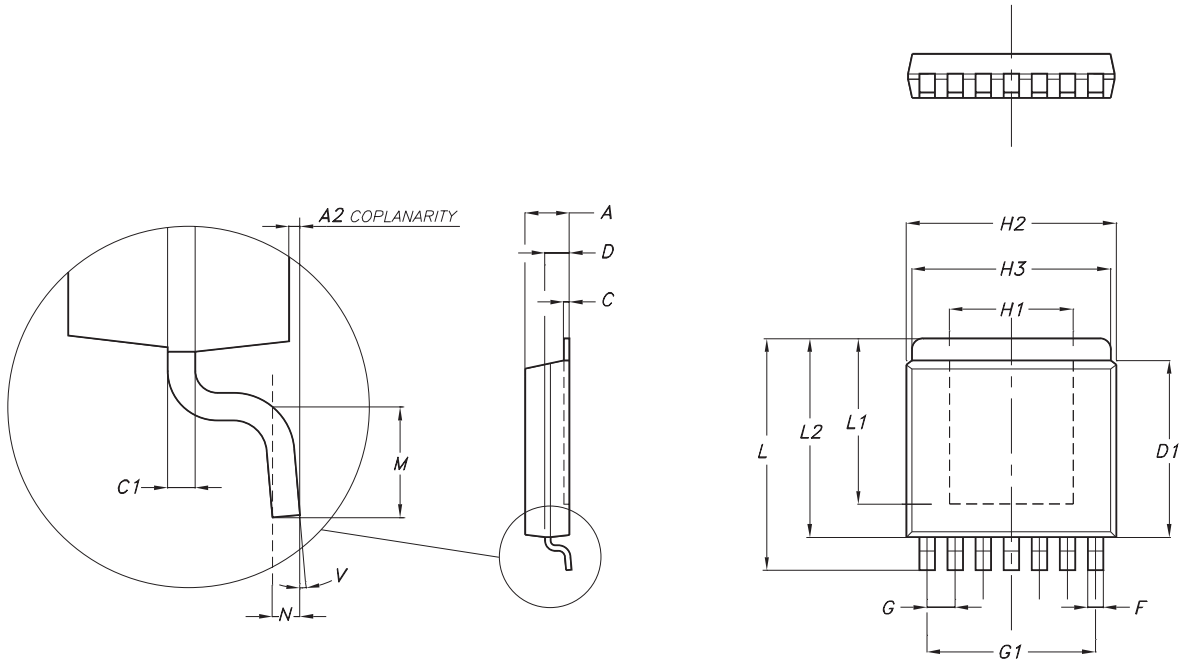
Figure 36 : Load Transient



V_{CC}=5V, V_{DD}=12V, I_{O1}=10 to 600mA, C_{CC}=1µF (tant), C_{DD}=100nF (X7R), All C_O=100nF (X7R)

SPAK-7L MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.78		2.03	0.070		0.080
A2	0.03		0.13	0.001		0.005
C		0.25			0.010	
C1		0.25			0.010	
D	1.02		1.27	0.040		0.050
D1	7.87		8.13	0.310		0.320
F	0.63		0.79	0.025		0.031
G		1.27			0.050	
G1		7.62			0.3	
H1		5.59			0.220	
H2	9.27		9.52	0.365		0.375
H3	8.89		9.14	0.350		0.360
L	10.41		10.67	0.410		0.420
L1		7.49			0.295	
L2	8.89		9.14	0.350		0.360
M	0.79		1.04	0.031		0.041
N		0.25			0.010	
V	3°		6°	3°		6°



PO13F2/A