ST70136

CPE ADSL ANALOG FRONT END

- WIDE TRANSMIT AND RECEIVE DYNAMIC RANGE TO REDUCE EXTERNAL FILTERING REQUIREMENTS
- RECEIVE PROGRAMMABLE GAIN: 0 TO 31dB GAIN IN 1dB STEPS
- RECEIVE PROGRAMMABLE ATTENUATOR 0,-4dB, -8dB, -12dB
- 12-BIT A/D CONVERTER IN RECEIVE PATH
- TRANSMIT PROGRAMMABLE GAIN: 0 TO -15dB IN 1dB STEPS
- 14-BIT D/A CONVERTER IN TRANSMIT PATH
- LOW POWER MODE: 10mW IN LISTENING MODE, 250µW IN POWER DOWN
- TONE DETECTOR: ACTIVITY DETECTION FOR WAKE-UP FUNCTION
- 64-PIN TQFP PACKAGE
- 64-PIN LFBGA PACKAGE
- 0.50µm, 5V BICMOS TECHNOLOGY
- 3.3V DIGITAL INTERFACE
- 5V ANALOG INTERFACE

INTRODUCTION

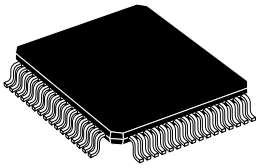
The ST70136 ADSL Analog Front End (AFE) chip implements the analog transceiver functions required in a Customer Premise ADSL modem. It connects the digital modem chip with the loop driver and hybrid balance circuits.

The AFE has been designed with high dynamic range in order to greatly reduce the external filtering requirements at the front end.

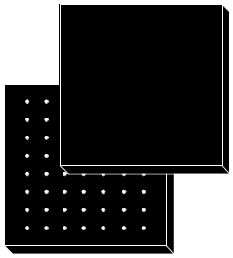
The AFE chip and its companion digital chip along with a loop driver, implement the complete G.992.2 and G.992.1 DMT modem solution.

The AFE receive path contains a programmable gain amplifier (RxPGA), a low pass anti-aliasing filter, and a 12-bit A/D converter. The RxPGA is digitally programmable from 0 to 31dB in 1dB steps.

The AFE transmit path consists of a 14-bit D/A converter, followed by a programmable gain amplifier (TxPGA). The transmit gain is programmable from 0 to -15dB in 1dB steps.

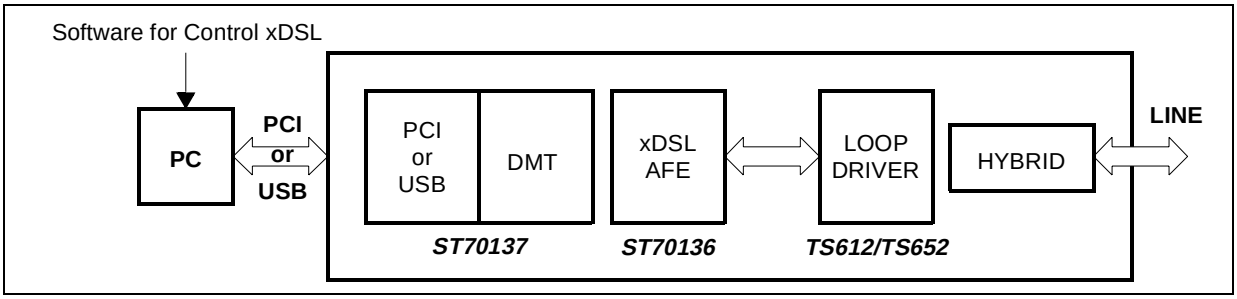


TQFP64 Full Plastic
(10 x 10 x 1.40 mm)
ORDER CODE: ST70136G

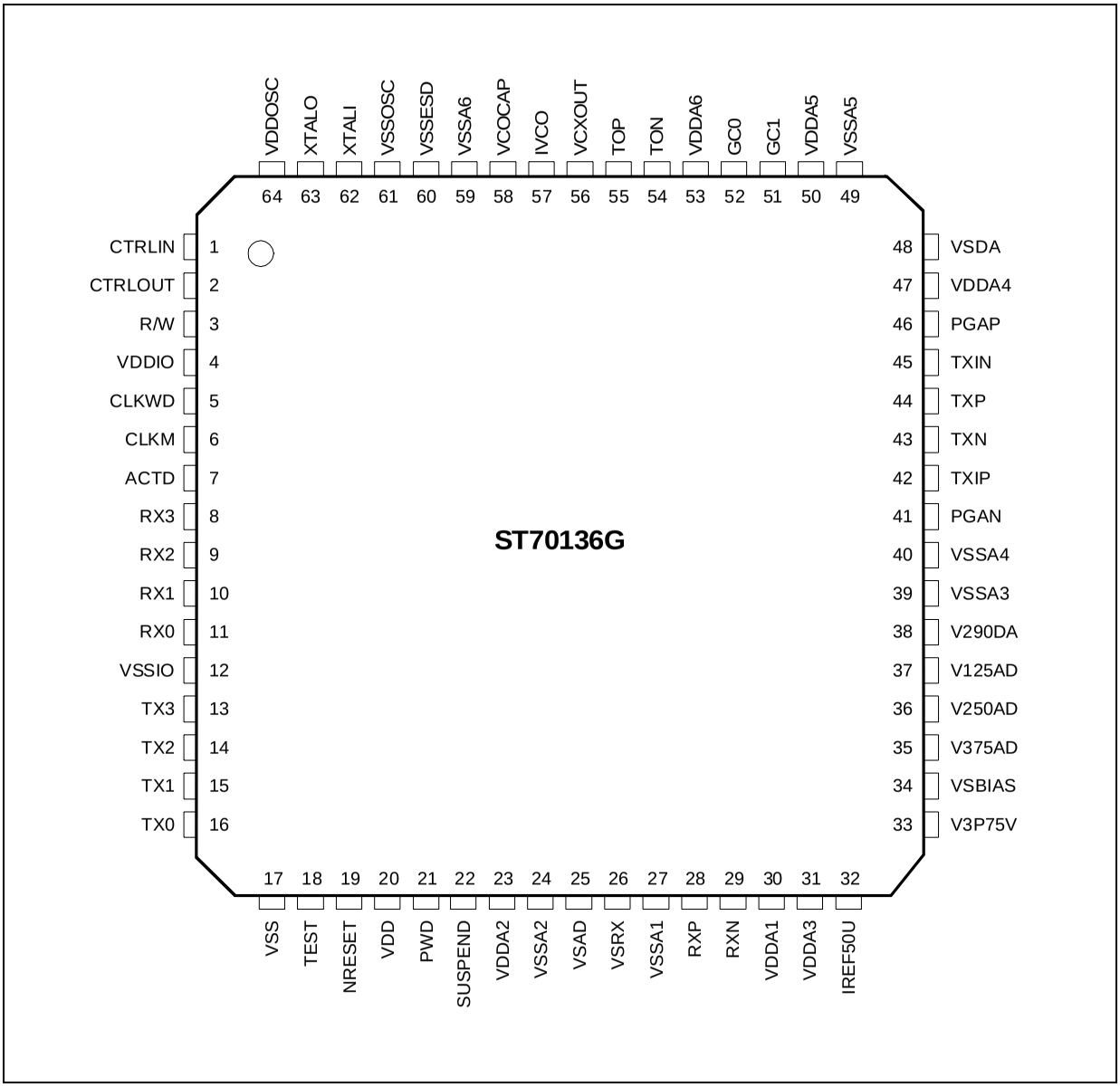


LFBGA64
(8 x 8 x 1.7 mm)
ORDER CODE: ST70136B

Figure 1 : Overall Application Block Diagram



ST70136 Pinout



1 - PIN LIST

The following list gives the different PIN Types:

AI	Analog Input	DO	Digital Output
AIO	Analog Input/Output	VDDA	Analog Power Supply
AO	Analog Ouptut	VDDD	Digital Power Supply
DI	Digital Input	VSSA	Analog Ground
DIO	Digital Input/Output	VSSD	Digital Ground

Table 1 : Pin Assignment

Pins		Name	Type	Description
TQFP	LFBGA			
1	B2	CTRLIN	DI	Digital input for control interface
2	C3	CTRLOUT	DO	Digital output for control interface
3	C2	R/NW*	DI	Selection of read or write mode for control interface
4	B1	VDDIO	VDDD	I/O buffer supply voltage
5	A1	CLKWD	DO	8.832MHz output clock. Used to synchronize RX/TX word data exchange, and master clock of register control interface
6	C1	CLKM	DO	35.328MHz Master Clock. Xtal buffer
7	D2	ACTD	O	Tone Detector Activation
8	D1	RX3	DO	Received data output
9	E2	RX2	DO	Received data output
10	E1	RX1	DO	Received data output
11	F2	RX0	DO	Received data output
12	G2	VSSIO	VDDD	I/O buffer ground voltage
13	F1	TX3	DI	Transmit data input
14	G1	TX2	DI	Transmit data input
15	H2	TX1	DI	Transmit data input
16	H1	TX0	DI	Transmit data input
17	E3	VSS	VSSD	Core digital ground
18	G3	TEST	DI	Test mode is activated with TEST=1. Must be tied to ground in normal mode
19	E4	NRESET*	DI	Reset input. All digital circuitry is well defined after a negative pulse on this input
20	H3	VDD	VSSD	Core digital supply (3.3V)
21	F3	PWD	DI	Power Down pin
22	G4	SUSPEND	DI	Suspend Mode pin
23	F4	VDDA2	VDDA	ADC supply voltage (5V)
24	H4	VSSA2	VSSA	ADC ground voltage
25	G5	VSAD	VSSA	Substrate voltage for RX-AD path (Must be connected to VSSAx)
26	E5	VSRX	VSSA	Substrate voltage for RXPGA path (Must be connected to VSSAx)
27	H5	VSSA1	VSSA	RXPGA ground voltage
28	H6	RXP	AI	Positive Analog Receive input

Table 1 : Pin Assignment (continued)

Pins		Name	Type	Description
TQFP	LFBGA			
29	H7	RXN	AI	Negative Analog Receive input
30	G6	VDDA1	VDDA	RXPGA voltage supply (5v)
31	F5	VDDA3	VDDA	Bias and References voltage supply (5v)
32	H8	IREF50U	AI	External resistor for bias current 50kΩ
33	G8	V3P75V	AO	3.75v output from bandgap; 0.22µF decoupling
34	G7	VSBIAS	VSSA	Substrate voltage for biasing & reference cell (Must be connected to VSSAx)
35	F7	V375AD	AO	3.75 volt reference voltage. Need decoupling 0.1µF
36	F8	V250AD	AO	2.50 volt reference voltage. Need decoupling 0.1µF
37	F6	V125AD	AO	1.25 volt reference voltage. Need decoupling 0.1µF
38	E7	V290DA	AO	2.90 volt reference voltage. Need decoupling 0.1µF
39	E8	VSSA3	VSSA	Biasing and References ground voltage
40	E6	VSSA4	VSSA	Tx path ground voltage
41	D6	PGAN	AO	Negative TXPGA output
42	D8	TXIP	AI	Positive analog input for Tx external filtering
43	D7	TXN	AO	Negative analog transmit output
44	C7	TXP	AO	Positive analog transmit output
45	C8	TXIN	AI	Negative analog input for Tx external filtering
46	B7	PGAP	AO	Positive TXPGA output
47	B8	VDDA4	VDDA	Tx analog supply voltage (5V)
48	A8	VSDA	VSSA	Substrate voltage for DAC path (Must be connected to VSSAx)
49	A7	VSSA5	VSSA	DAC path ground voltage
50	C6	VDDA5	VDDA	DAC analog supply voltage (5v)
51	A6	GC1	DO	MSB for external gain control
52	B6	GC0	DO	LSB for external gain control
53	D5	VDDA6	VDDA	VCXO & Tone detector Input analog supply voltage (5v)
54	C5	TON	AI	Negative tone detector input
55	B5	TOP	AI	Positive tone detector input
56	D4	VCXOUT	AIO	VCXO output current
57	A5	IVCO	AIO	VCXO input current
58	C4	VCOCAP	AO	VCXO output filtering
59	A4	VSSA6	VSSA	VCXO & Tone detector analog ground voltage
60	B4	VSSESD	VSSD	Ground voltage reference for ESD
61	D3	VSSOSC	VSSD	Ground voltage for Xtal oscillator
62	A3	XTALI	DI	Xtal oscillator input
63	B3	XTALO	DO	Xtal oscillator output
64	A2	VDDOSC	VDDD	Supply voltage for Xtal cell (3.3v)

** A "N" means active low. Example: R/NW means write active low.*

2 - PIN DESCRIPTION

2.1 - Analog Power Supplies

These pins are the positive analog power supply voltage for the DAC and the ADC section. It is not internally connected to digital supply. In any case the voltage on these pins must be higher or equal to the voltage of the Digital power supply.

2.2 - Digital Power Supplies

These pins are the power supply pins that are used by the internal digital circuitry. All DVDD pins must be connected together to a +3.3 V supply.

2.3 - Analog Ground and Substrate

These pins are the ground return of the analog DAC and ADC blocks. The analog VDDA should be decoupled with respect to the analog ground. Decoupling capacitors should be as close as possible to the supplies pins. All grounds must be tied together.

2.4 - Digital Ground

These pins are the ground return of the digital circuitry. The digital power supplies must should be decoupled with respect to the digital ground. Decoupling capacitors should be as close as possible to the supplies pins. All grounds must be tied together.

2.5 - Powerdown - PWD

When pin PWD =”1”, the chip is set in low power mode.

2.6 - Suspend

The SUSPEND pin is used to control the output of CLKM. When SUSPEND is low CLKM output is enabled otherwise CLKM is disabled.

2.7 - Reset

The reset function is implied when the NRESET pin is at a low voltage input level. In this condition, the reset function can be easily used for power up reset conditions. Reset is asynchronous, tenths of ns are enough to put the IC in reset. After reset, all registers are set to their default value.

2.8 - Reference Voltages

2.8.1 - V125AD, V250AD, V375AD

These pins are used to externally decouple the internal reference voltages used for the ADC (1.25V, 2.5V, 3.75V).

2.8.2 - V3P75V

This pin is the 3.75V Bandgap output and should be externally decoupled with an external capacitor of 0.22uF.

2.8.3 - IREF50U

This pin is used for setting the bias current and must be externally connected to a resistor of 2.5V / 50μA equals 50kΩ.

2.8.4 - V290DA

This pin is the 2.9V transmit DAC output reference voltage and must be decoupled externally.

2.9 - Analog Transmit Output

2.9.1 - TXP

This pin is the non-inverting output of the fully differential analog amplifier.

2.9.2 - TXN

This pin is the inverting output of the fully differential analog amplifier.

2.9.3 - TXIP

This pin is the differential non-inverting input for external filtering.

2.9.4 - TXIN

This pin is the differential inverting input for external filtering.

2.9.5 - PGAP

This pin is the differential non-inverting PGA output.

2.9.6 - PGAN

This pin is the differential inverting PGA output.

2.10 - Analog Receive Input

2.10.1 - RXN

This pin is the differential inverting receive input.

2.10.2 - RXP

This pin is the differential non-inverting receive input.

2.11 - Tone Detector

The analog input differential signal must be less than 8V peak to peak. These pins are used for activity detection when in sleeping mode.

2.11.1 - TON

This pin is the differential inverting tone detector input.

2.11.2 - TOP

This pin is the differential non-inverting tone detector input.

2.11.3 - ACTD

This pin is active when tone 40 or 72 has been detected in sleeping mode (see control register)

2.12 - CRYSTAL

These pins must be tied to an external crystal (F = 35.328MHz).

2.12.1 - XTALI

This pin is the crystal oscillator input.

2.12.2 - XTALO

This pin is the crystal oscillator output.

2.13 - VCXO

2.13.1 - IVCO

This pin is the current reference for the VCO DAC

2.13.2 - VCOCAP

This pin is used to introduce time constant. The tuning is done by connecting an external capacitor

2.13.3 - VCXOUT

This pin is the output control current generated by a 8 bit DAC.

2.14 - Control Serial Interface

Access to the control register can be done only in stable state fonctionality:

SUSPEND = "0".

2.14.1 - CTRLIN

This pin is used to program the internal registers. The data burst is composed of 16 bits sampled at CLKM when CLKWD = 1. The first bit is used as start bit (’0’), the three LSBs being used to identify the data contained in the twelve remaining bits.

The start bit b15 (b5 = 0) is transmitted first followed by bits b[14:0]. At least 1 stop bit "1" need to be provided to validate the data.

2.14.2 - CTRLOUT

This pin is the control register output. The burst data on this pin is the value of the register addressed by CTRLIN.

2.14.3 - CLKWD

This pin is the word clock used to sample the control information and equal to CLKM / 4.

2.14.4 - R/NW

This pin is used for the read and write operation for the control interface and sampled at the same time than bit b15 of CTRLIN.

2.14.5 - Digital Interface

The interface is a nibble serial interface running at 8.832MHz sampling frequency. The data are presented in 16bits format, and transferred in groups of 4 bits (nibbles). The LSBs are transferred first. Data is transmitted on the rising edge of the master clock CLKM

2.14.6 - CLKM

This pin is the master clock equal to 35.328MHz and is the sampling clock of the input / output data.

2.14.7 - TX0, TX1, TX2, TX3

These pins are the digital transmit data input.

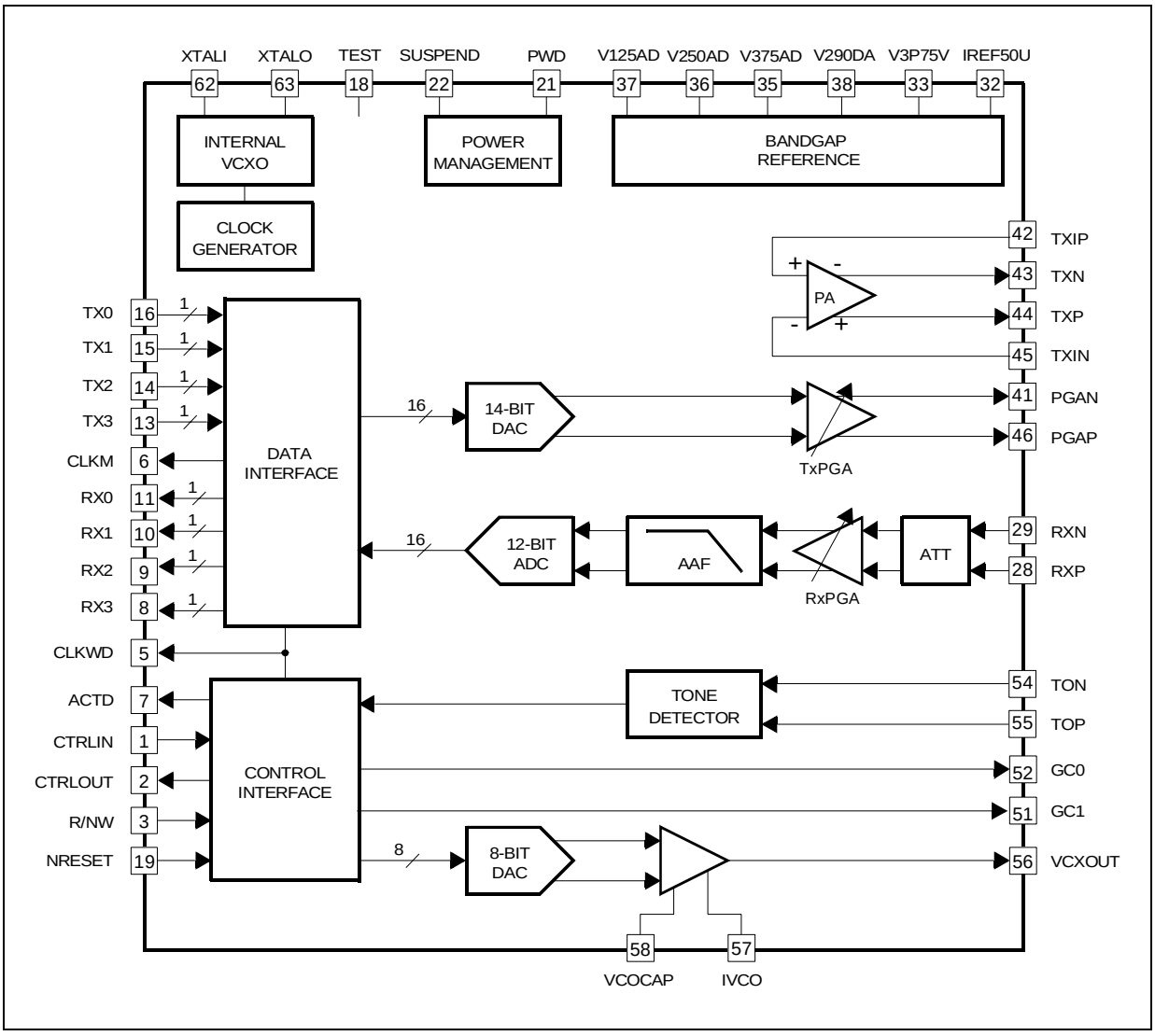
2.14.8 - RX0, RX1, RX2, RX3

These pins are the digital receive data output.

2.15 - Test

This pin is dedicated to put the ST70136 in test mode.

3 - BLOCK DIAGRAM



4 - FUNCTIONAL DESCRIPTION

4.1 - General

The ST70136 consists of the following functional blocks:

– Transmit Signal Path
– Receive Signal Path
– Bias Voltage and Current Generation
– Digital Data Interface
– Control Serial Interface
– Tone Detector
– Power Down mode management

4.2 - Transmit Path Description

The transmit path contains the 14-bit digital to analog converter (DAC) necessary to generate the transmit signal from a 16-bit digital input word.

This transmit signal is then scaled by the on chip programmable gain amplifier (TxPGA) from 0 to -15dB in 1dB steps. The scaled output signal is then driven off chip to the external filters and power amplifier (PA) which drives the DMT signal to the subscriber loop. The transmit path is fully differential.

4.3 - Receive Path Description

The receive path contains first an attenuator (which allows the selection between 4 attenuated versions of the signal) followed by a programmable gain amplifier (RxPGA), a 1st order low pass anti-aliasing filter, and a 12-bit analog to digital converter (ADC). The RxPGA gain is digitally programmable from 0 to 31dB in 1dB steps. The receive path is fully differential.

4.4 - VCXO

The ST70136 contains the circuits required to construct an internal VCXO. It is divided in a crystal driver and an auxiliary 8 bits DAC for timing recovery. The crystal driver is able to operate at 35.328MHz.

The DAC which is driven by the CTRLIN pin (the input of the Serial Control Interface), provides a current output with 8 bits resolution and can be used to tune the crystal frequency with the help of external components. A time constant between DAC input and VCXOUT can be introduced (via CTRLIN interface) and programmed with the help of an external capacitor (on VCOCAP pin).

4.5 - Bias Voltage and Current Generation

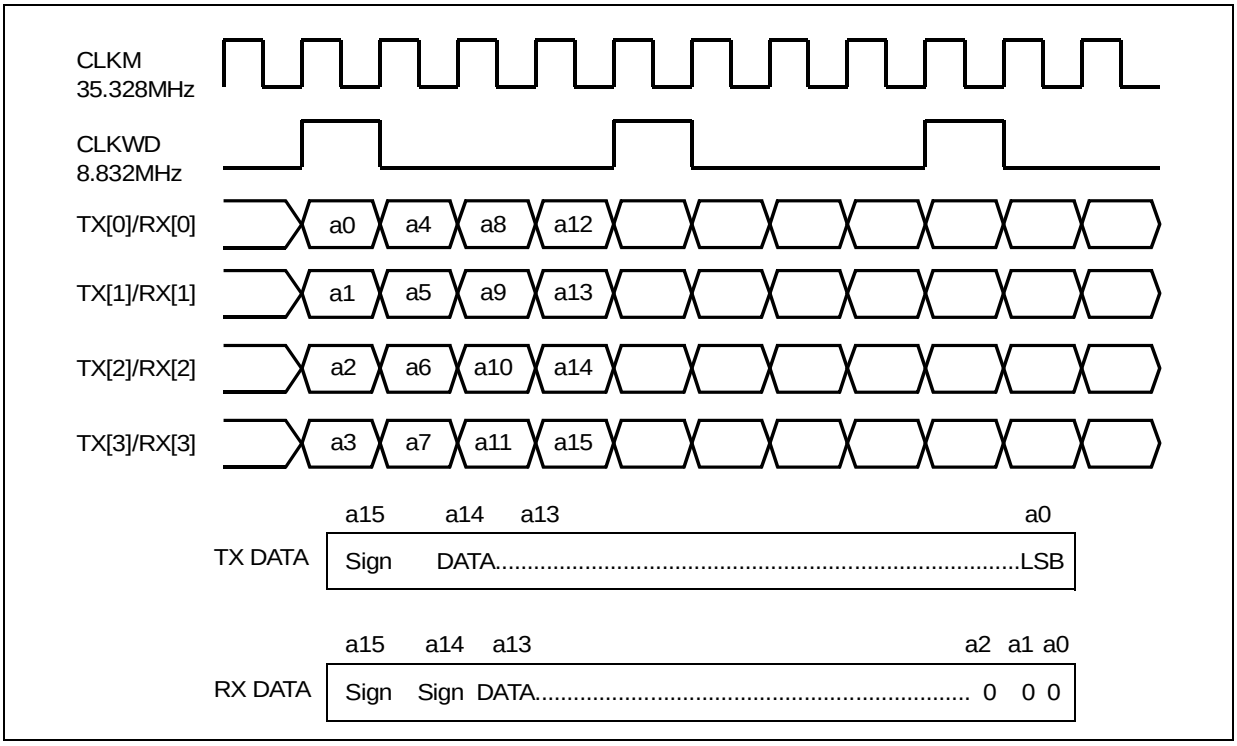
The bias circuitry contains a bandgap voltage reference from which the converters references and analog ground voltages are generated. This block also generates an accurate bias current using an external resistor.

4.6 - Digital Data Interface

To facilitate data transfer between the ST70136 and the digital data pump, a 4-bit wide serial interface for the transmit and receive path is incorporated into the AFE.

This interface consists of four transmit pins (TX[0:3]), four receive pins (RX[0:3]), and the necessary control signals (CLKM, CLKWD) to transmit and receive the required data.

Figure 2 : Digital Data Interface



4.7 - Control Serial Interface

There is a 4-pin serial digital interface (CLKWD, CTRLIN, CTRLOUT, R/W) that access one of the 8 x 12-bit registers that controls all the programmable features on the ST70136.

The registers are loaded with the asynchronous type data burst delivered to CTRLIN pin. It is composed of 16 bits from which the first bit (b15) is used as start bit ('0'), the three LSBs (b2:b0) being used to identify the register to be loaded.

The twelve remaining bits (b14:b3) are the control data. During a read operation, the CTRLOUT pin figures out the register contents addressed by CTRLIN pin.

Figure 3 : Control Register Interface Write Cycle

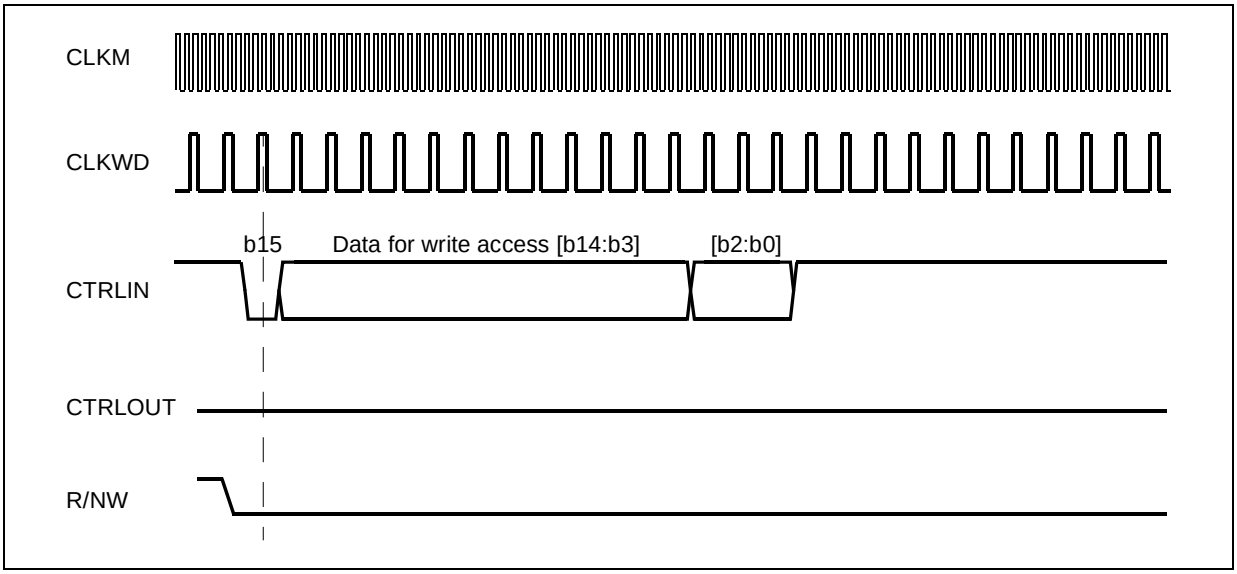
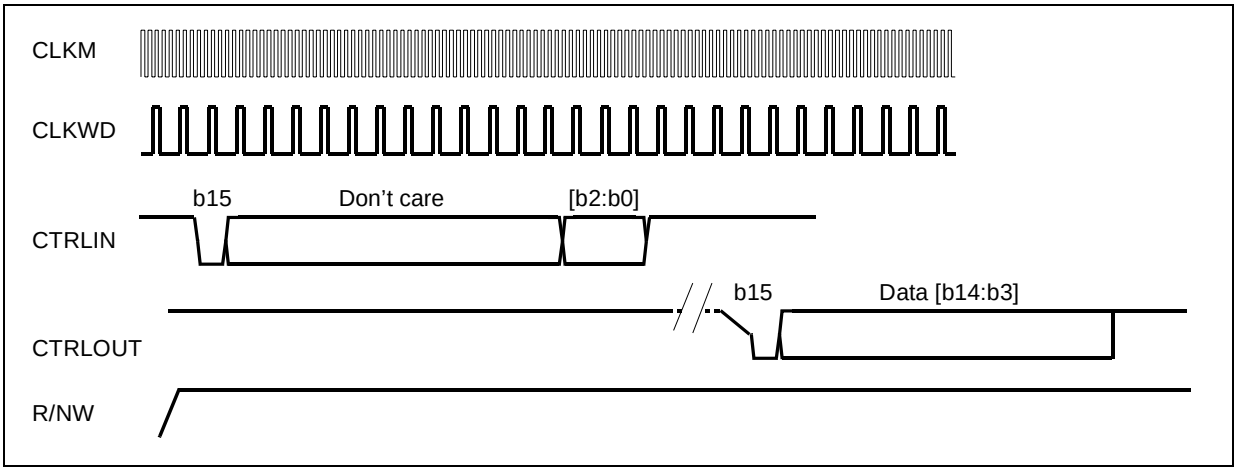


Figure 4 : Control Register Interface Read cycle



4.7.1 - AFE registers

4.7.1.1 - Rx Gain Control

This register is located at the address “000” and is used to program the gain in the receive path.

Table 2 : Rx Gain Control (address [b2:b0]=”000”)

Name	Pos.	Type	Def.	Description
GC[1:0]	14.13	R/W	00	bit14: selects External Gain Control GC1 bit13: selects External Gain control GC0
Other	12	R/W	0	Reserved
RxAGC	11..7	R/W	00000	Select internal gain for Receive amplifier 00000 : 0dB 11111 : 31dB
RxAtt	6..5	R/W	00	Receive attenuator 00 = 0dB 01 = -4dB 10 = -8dB 11 = -12dB
Other	4.3	R/W	00	Reserved

4.7.1.2 - Tx Gain Control

This register is located at the address “001” and is used to program the gain in the transmit path.

Table 3 : Tx Gain Control (address [b2:b0]=”001”)

Name	Pos.	Type	Def.	Description
TxAGC	14..11	R/W	0000	Select internal gain for Transmit amplifier 0000 : -15dB 1111 : 0dB
Other	10..3	R/W	0..0	Reserved

4.7.1.3 - Special Features Configuration

This register is located at the address “010” and is used to configure different blocks.

Table 4 : Adsl Configuration (address [b2:b0]=”010”)

Name	Pos.	Type	Def.	Description
Reserved	14.13	R/W	00	Reserved
VCO-DAC	12	R/W	1	Enable the VCO DAC 1: enabled 0: disabled
Other	11.4	R/W	0..0	Reserved
FVCXO	3	R/W	0	Filtered VCXO output 1 : filtered 0 : not filtered

4.7.1.4 - VCXO Control

Table 5 : VCXO DAC Value (address [b2:b0]=”011”)

Name	pos.	type	def.	Description
DAC value	14..7	R/W	80H	8 bits for VCO DAC. 0...0 = min. current 1...1 = max current.
Others	6..3	R/W	0000	Reserved

4.7.1.5 - Test Only Registers

They are presently located at address “100” to “101”.

4.7.1.6 - Tone Detection Threshold Setting Register

Table 6 : Tone Detection Threshold Setting Register (address [b2:b0]=”110”)

Name	Pos.	Type	Def.	Description
Threshold Level	14..5	R/W	1000000000	Set the threshold of the tone detector
Reserved	4.3	R/W	00	Reserved

4.7.1.7 - Status Register & tone detector

This register can be used in the case of read / write registers.

Table 7 : Status & Tone Detector Register (address [b2:b0]=”111”)

Name	Pos.	Type	Def.	Description
Receiver Clip indicator	14	R/W_clear [1]	0	1: Receive Clipping occurred
Transceiver Clip indicator	13	R/W_clear	0	1: Transmit Clipping occurred
Sleeping Mode	12	R/W	0	0: disable tone detector in power down 1: enable tone detector in power down
Tone Detector	11	R/W	0	Tone detector frequency setting 0: standard ADSL (tone 40) 1: ADSL over ISDN (tone 72)
Debug Mode	10	R/W	0	When in normal mode “0” the CTRLOUT pin is in HIZ and don’t care for R/W and the control access register are always writing operation whatever on R/W pin. When in debug mode “1” the CTRLOUT and R/W pins are operating as defined in pin description chapter.
Software Reset	9	R/W	0	When set all registers are set to their default value
Reserved	8..3	R/W	0..0	Reserved

Note: 1. R/W_clear: bit is resetted to 0 by writing 0.

4.8 - Tone Detector

The tone detector is dedicated for remote activation. It operates during SUSPEND mode with PWD = 0 only. When the tone detector level received Vin over tone 40 or 72 is greater than 15µV peak to peak, the ACTD pin is set to wake up the modem.

ACTD pin is resetted when the AFE is back in full operating mode (SUSPEND = 0, PWD = 0). The maximum signal sensitivity at the Tone detector inputs is 50mV peak to peak.

4.9 - Mode Management

4.9.1 - General

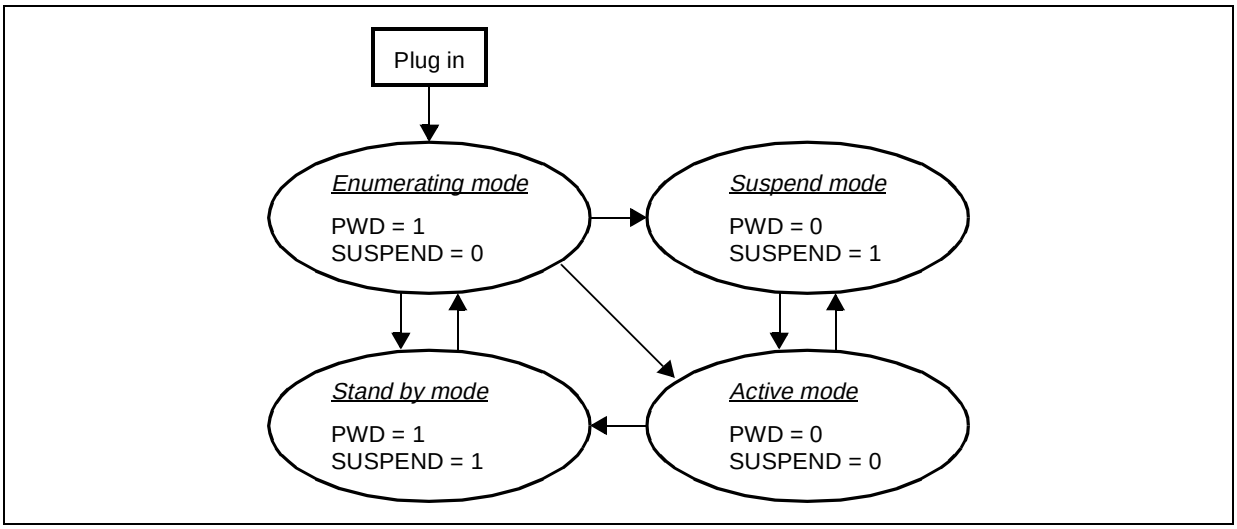
The ST70136 can be used in a various range of ATU-R equipments, but a specific mode management address USB application in its different modes.

In following table, "CPE" is an USB ADSL modem application done with a ST70136 AFE and a ST70137 DMT. The CPE is connected to an USB port of an equipment.

Table 8 : ST70136 / USB Operating Mode Configurations

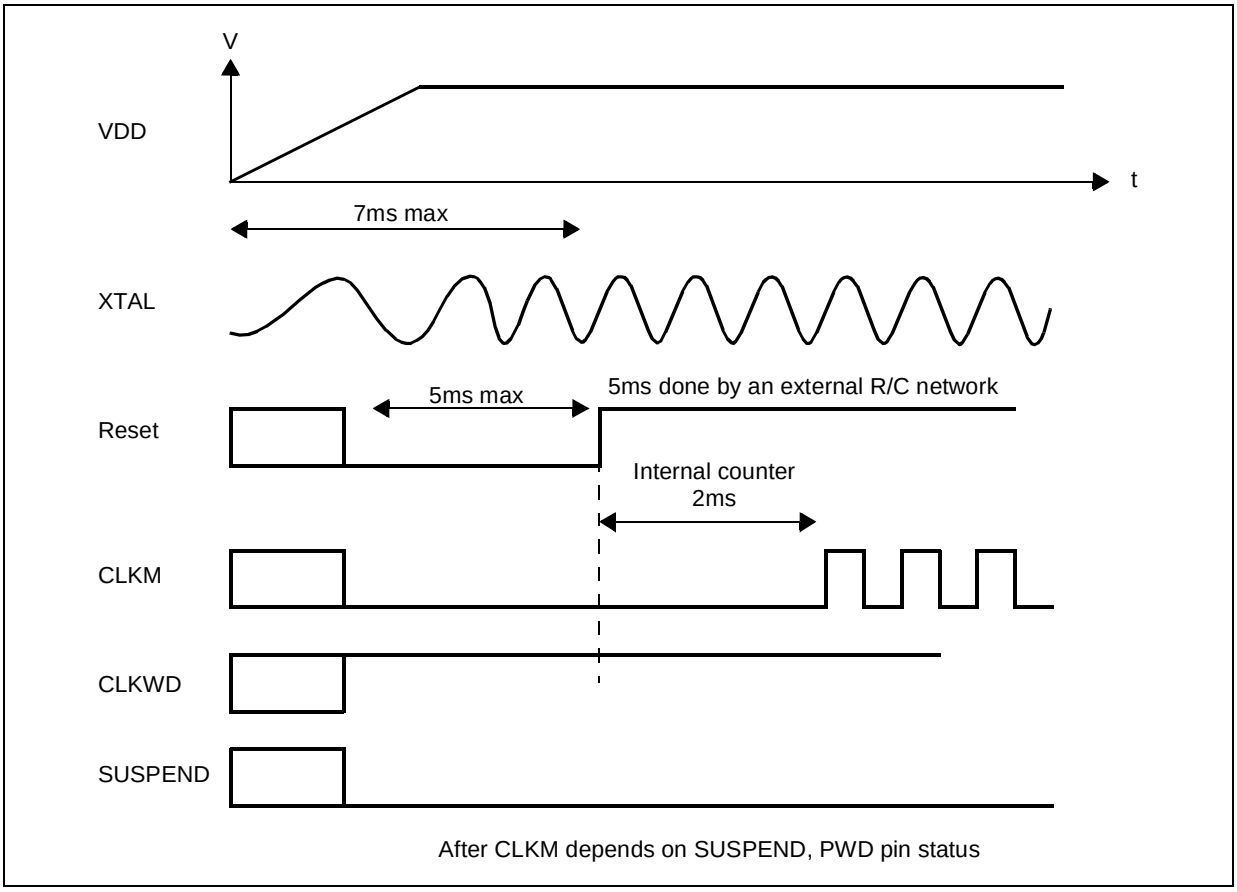
SUSPEND	PWD	USB Mode Description
0	0	**Active mode** The CPE application is in operative mode, its current consumption is less than 500 mA. ST70136 is power-up, the Tone detector is OFF and CLKM output is enabled.
0	1	**Enumerating mode** The CPE application is in the configuration process, plug in, its current consumption is less than 100 mA. ST70136 analog part is in power done mode, the digital part is enabled and CLKM output is enabled.
1	0	**Suspend mode after enumerating mode** After enumerating, the CPE application is in suspend mode, in this mode the CPE must be able to wake up the equipment when a tone is received, its current consumption is less than 2.5 mA. ST70136 analog and digital parts are in power down mode, the Tone detector is activated and CLKM output is disabled.
1	1	**Stand by mode** The CPE is not configured and in stand by mode, it could be wake up only by the equipment, its current consumption is less than 500µA. ST70136 is fully in stand by mode and CLKM is disabled.

Figure 5 : USB Power Management Operating Modes



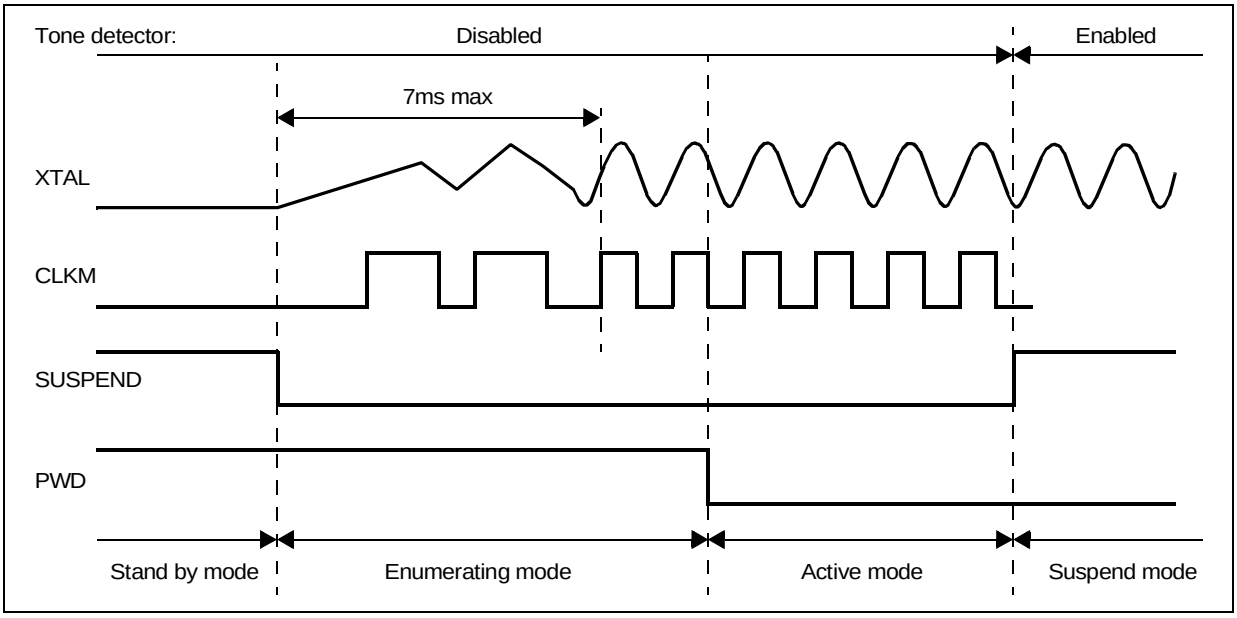
4.9.2 - Reset Timing

Figure 6 : Reset Timing



4.9.3 - Mode Management Timing

Figure 7 : Mode Management



5 - SPECIFICATIONS

5.1 - Absolute Maximum Ratings

Supply Voltage(AVDD,DVDD)	-0.3V to 6V
Input Voltage	-0.3V to AVDD,DVDD + 0.3V
Input current per pin	-10mA to + 10mA
Output current per pin	-20mA to + 20mA
Storage Temperature	-65°C to 150°C
ESD Protection	2000V

General DC Specification

Parameter	Minimum	Typical	Maximum	Unit
AVDD	4.75	5	5.25	V
DVDD	3	3.3	3.6	V
- Active				
Analog		75	85	mA
Digital		10	30	mA
Oscillator		2	5	mA
- Listening				
Analog		10	11	µA
Digital		1.1	1.7	mA
Oscillator		0.6	1	mA
- Stand by				
Analog		10	11	µA
Digital		10	25	µA
Oscillator		5	25	µA

5.2 - Characteristics for Digital Signals

T_A = 0 to 70°C unless otherwise specified.

	Parameter	Type	Conditions	Minimum	Typical	Maximum	Unit
Iil	Low level input current	DI	Vi = 0v	-1		1	µA
Iih	High level input current	DI	Vi = VDD	-1		1	µA
Ioz	Tri-state output leakage	DIO	Vo = 0v or VDD	-1		1	µA
Vih	Input high voltage	DI, DIO		0.8 x VDD			V
Vil	Input low voltage	DI, DIO				0.2 x VDD	V
Voh	high level output voltage	DO	Ioh = 2mA			0.4	V
Vol	low level output voltage	DO	Iol = 2mA	0.85 x VDD			V
Col	Output load capacitance	DO				20	pF

5.3 - Receive Path Specifications

TA = 0 to 70°C unless otherwise specified. The following specifications are guaranteed only when the Digital Control Interface is not active.

Table 9 : Receive Path Specifications

Typical specifications apply for VCC = 5.0V, temperature = 27°C, nominal process and bias current. Maximum and minimum performance is with VCC ±5%, 0°C < $T_{ambient}$ < 70°C, and worst case process and bias current.					
Description	**Min.**	**Typ.**	**Max.**	**Unit**	**Comments**
Output word rate		8.832		MHz	Data Sampling frequency
Output word resolution 16 bits			16	bits	
Reference Input signal [a]	-0.8	-0.4	0	dBfs	Fref=138KHz, PGA gain=0dB, Vin = 0dBr (2.4Vpd)
Common mode voltage	2.4	2.5	2.6	V	Measured on each single input
Differential Input impedance	12	20	28	kΩ	Between RXN and RXP
Input noise [b]			15	$\frac{nV}{\sqrt{Hz}}$	@gain=+31dB, frequency>138KHz
Gain, 0 ≤ D ≤ 31 [c] Step size 1dB	D-0.5	D	D+0.5	dB	Receive Programmable gain. D is the binary value of the control word. (see Section 4.7.1.1 - Rx Gain Control on page 10
Step size	0.8	1	1.2	dB	
Attenuator 0 >= Att >= -3 [d] Step size 4dB	4*Att-0.5	4*Att	4*Att+0.5	dB	Receive attenuator ATT is the binary value of the control word. (see Section 4.7.1.1 - Rx Gain Control on page 10
Att step size	3.5	4	4.5	dB	
AAF cutoff frequency	1	1.4	2	MHz	-3dB corner vs low frequency
Output SDR 2 tones [e]	66			dBc	For RxPGA gain=31dB, measured at output of ADC.

Notes: a. The corresponding typical value correspond to a 2.4Vpd at RXN/RXP differentiel inputs. The 2.4Vpd correspond to what will be called 0dBr for the other specifications in the present table. Variations include process, temperature and power variations.

b. The input noise must be measured in the frequency domain from 138KHz to 1.1MHz, with an sinusoidal input signal at -60dBr amplitude. Frequency of the input signal is 552KHz.

c. D is the gain relatively to the 0dBr previously defined. Variations include process, temperature and power variations.

d. Monotonicity is guaranted for RxPGA, Attenuator, but separatly.

e. Ratio between max peak amplitude of one of the 2 single tones to any spurious measured in the down-stream band [138KHz-1.1MHz] ; each tone amplitude is at -6-31=-37dBr. The couples are (f1,f2) = (200KHz, 300KHz), (400KHz, 500KHz), (600KHz, 700KHz).

5.4 - Transmit Path Specifications

TA = 0 to 70°C unless otherwise specified. The following specifications are guaranteed only when the Digital Control Interface is not active.

Table 10 : Transmit Path Specifications

Typical specifications apply for VCC = 5.0V, temperature = 27°C, nominal process and bias current. Maximum and minimum performance is with VCC ±5%, 0°C < $T_{ambient}$ < 70°C, and worst case process and bias current.					
Description	**Min.**	**Typ.**	**Max.**	**Unit**	**Comments**
Input word rate		8.832		MHz	
Input word resolution			16	bits	
PGAP/PGAN OUTPUT					
Common mode voltage	2.4	2.5	2.6	V	Measured on each output
Load resistance	500			Ω	Single ended
Load capacitance			10	pF	Single ended
Output Impedance		1	5	Ω	Single ended
Reference Output signal [a]	-5%	2.4	+5%	Vp	Differential output @0dB gain for TxPGA
Output noise			45	$\frac{nV}{\sqrt{Hz}}$	See also mask diagram below ("Final PGAP/N noise mask")
Cutoff frequency		4		MHz	@-3dB
Gain,$0 \leq D \leq 15$ [b] step size 1dB	-D-0.5	-D	-D+0.5	dB	Programmable attenuator.
Step size	0.8	1	1.2	dB	
TXP/TXN OUTPUT					
Common mode voltage	2.4	2.5	2.6	V	Measured on each output
Load resistance	500			Ω	Single ended
Load capacitance			10	pF	Single ended
Output Impedance		1	5	Ω	Single ended
Output SDR 2 tones ADSL/POTS [c] 2 tones ADSL/ISDN [d]	 79 71			dB	For TxPGA gain = 0dB

Notes: a. This will represents the 0dBr for the other specifications in the present table. The level is mesured for the frequency of 30KHz which will correspond to the reference frequency. Variations include process, temperature and power variations.

b. This gain is given relatively to the 0dBr previously defined. Variations include process, temperature and power variations.

c. Ratio between max peak amplitude of one of the 2 single tones to any spurious. Measure performed for a dual tone signal (each tone with an amplitude equal to -6dBr), in range 30KHz to 1MHz (couple (f1,f2) are (70KHz, 80KHz), (120KHz, 130KHz)).

d. Ration between max peak amplitude of one of the 2 single tones to any spurious. Measure performed for a (250KHz, 260KHz) dual tone signal (each tone with an amplitude equal to -6dBr), in range 30KHz to 1MHz.

Figure 8 : Tone Detector Schematic

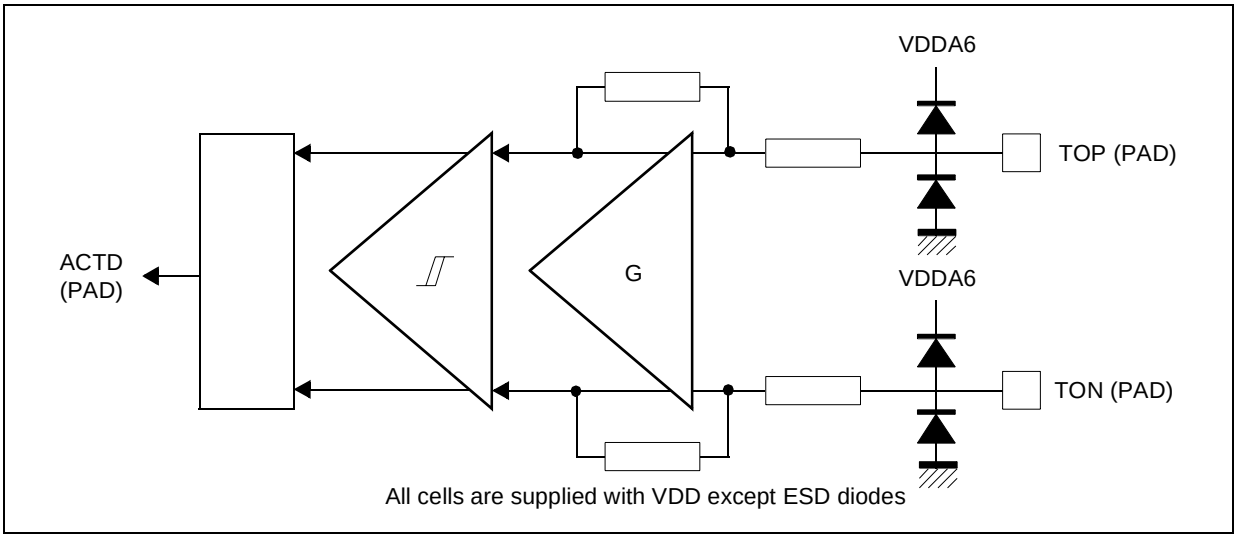


Table 11 : Tone DetectorSpecifications

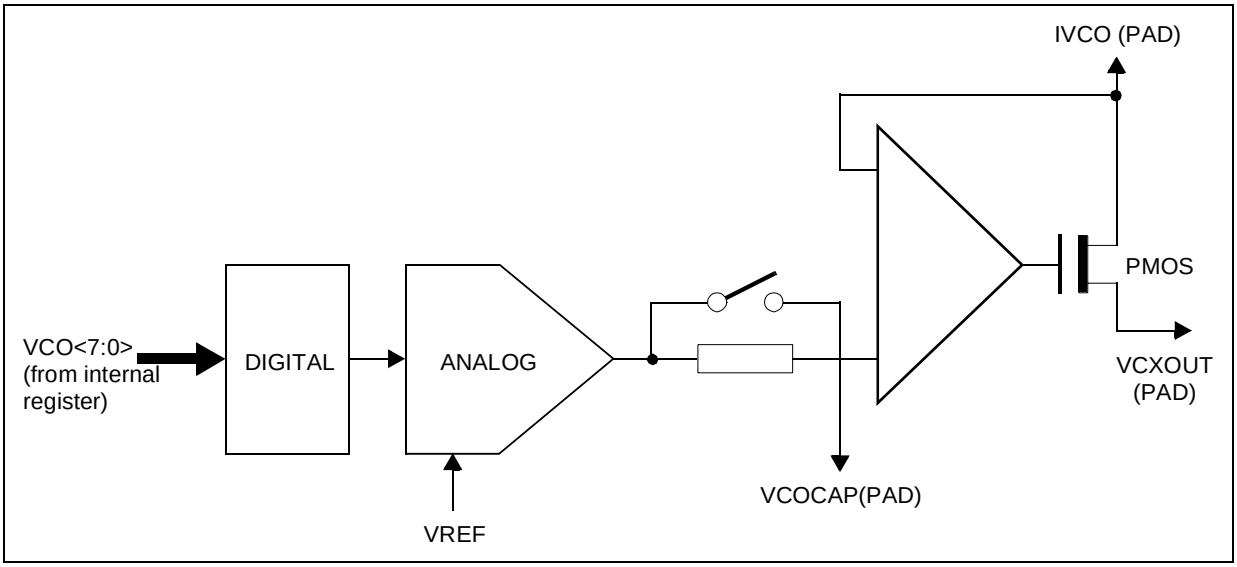
Description	Minimum	Typical	Maximum	Unit	Comments
Zin listening mode	3.5	5	6.5	kΩ	Diffferential
Zin normal mode	350	500	650	kΩ	Diffferential
Minimum differential input signal	15			µVp	Peak to peak
Maximum diffential input signal			VDD		In listening mode
VCM input		VDD/2			In listening mode

5.5 - VCXO

Unless otherwise noted, typical specifications apply for AVdd = 5.0V, DVdd = 3.3V, temperature = 27°C.

A voltage controlled crystal oscillator is integrated in ST70136. Its nominal frequency is 35.328MHz. The quartz crystal is connected between XTALI and XTALO pins.

Figure 9 : DAC VCXO Schematic



TA = 0 to 70°C unless otherwise specified.

Table 12 : DAC 8B Specifications

Typical specifications apply for VCC = 5.0V, temperature = 27°C, nominal process and bias current. Maximum and minimum performance is with VCC ±5%, 0°C < $T_{ambient}$ < 70°C, and worst case process and bias current.						
Description		**Minimum**	**Typical**	**Maximum**	**Unit**	**Comments**
Number of bit			8			
Sampling rate				1	KHz	
DNL	a	-0.5		0.5	LSB	
INL	a	-2		2	LSB	
max code (FFh)	a	2.42	2.52	2.62	V	
mid code (80h)	a	3.57	3.63	3.69	V	
min code (00h)	a	4.74	4.77	4.80	V	
Offset IVCO vs VCOCAP	b	-10		10	mV	
Offset variation with current		-20		20	mV	Iout variation from 10µA to 400µA, @ code max, VCXOUT = 2.4V
VCOCAP Zout	c	320	500	680	kΩ	
VCOCAP Zout	d	350	500	650	Ω	
VCOCAP load			10		µF	

Notes: a. Measured at VCOCAP output, filter disabled.

b. Filter disabled, current through IVCO = 10µA, VCXOUT = 2V.

c. Filter enabled.

d. Filter disabled.

5.6 - Crystal

Table 13 : Crystal Parameters

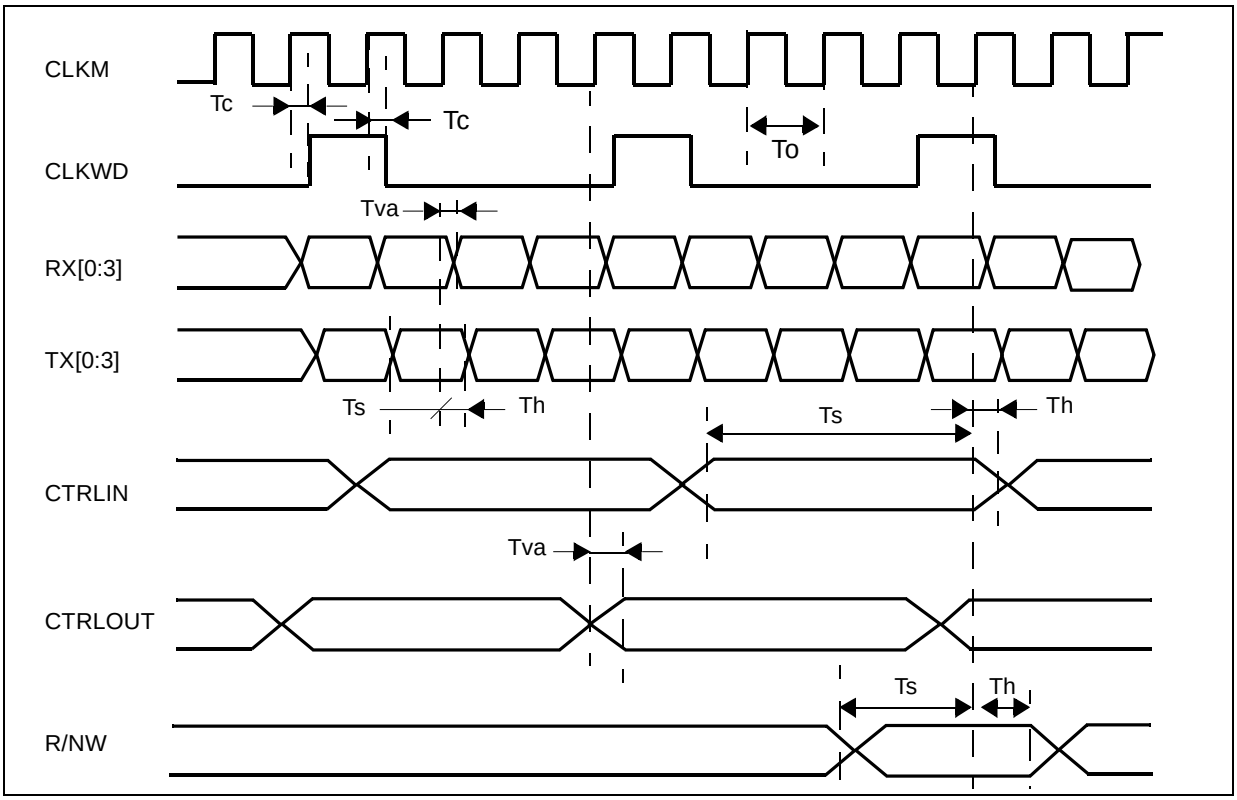
Parameter	Symbol	Minimum	Typical	Maximum	Unit
Start up time	T_{SU}			7	ms
Clock Frequency	CLKM		35.328		MHz
Frequency adjustment range	X_{ADJ}	-100		100	ppm

Note: Recommended Crystal: MELCOM 35.328MHz / UM1/ 30 / 30 / 0+70 / 15pF / FUND.

5.7 - Data and Control Timing Interface

T_A = 0 to 70°C unless otherwise specified.

Figure 10 : Data and Control Timing Interface



Symbol	Description	Minimum	Typical	Maximum	Unit
Tva	Data valid time	0		4	ns
Ts	Data setup time	13			ns
Th	Data hold time	2			ns
Tc	Word clock delay	0		4	ns
Fo	CLKM Frequency		35.328		MHz
	CLKM clock duty cycle	40		60	%
To	CLKM period		28.3		ns

Figure 11 : Application Schematic ST70136

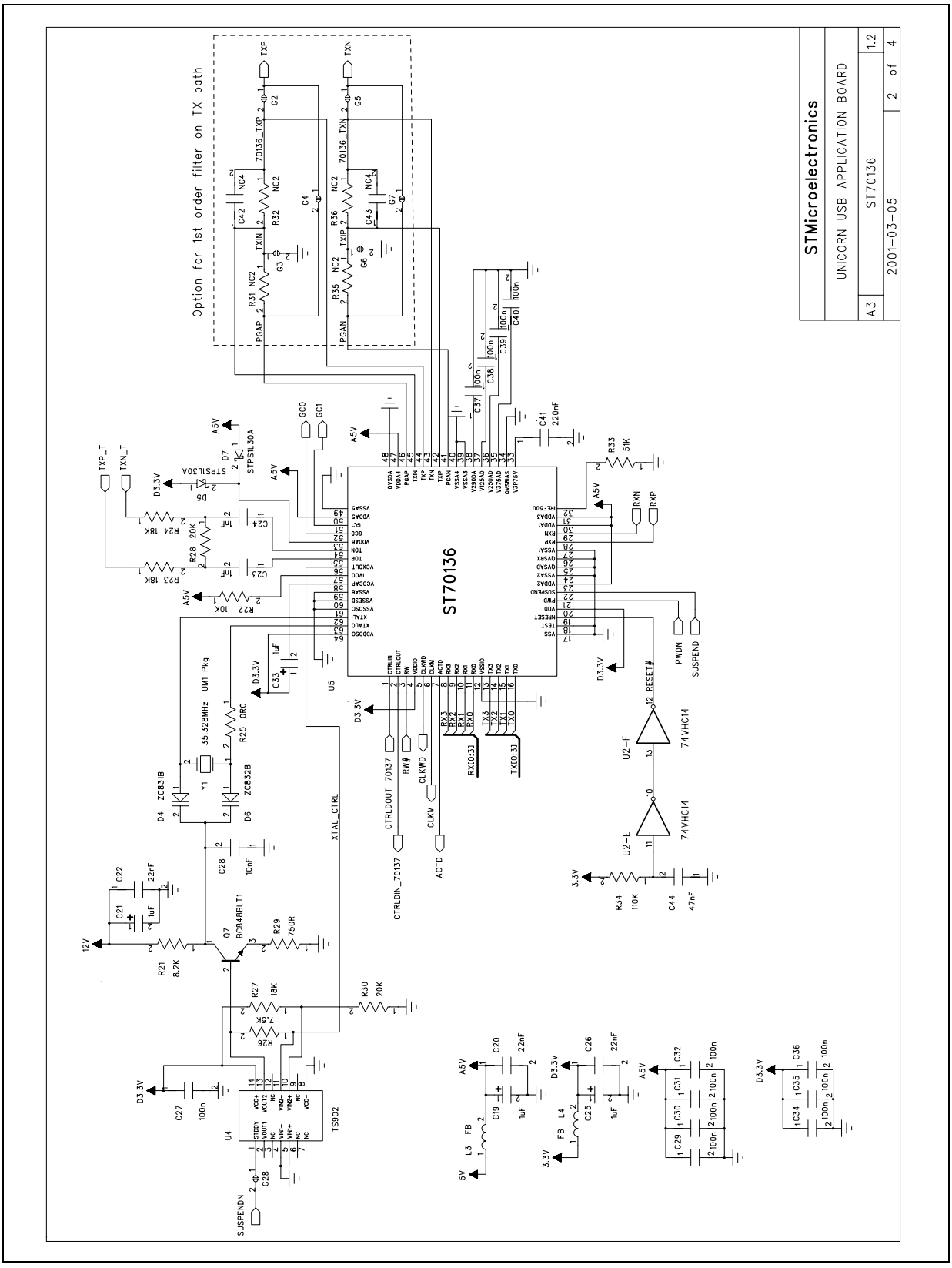
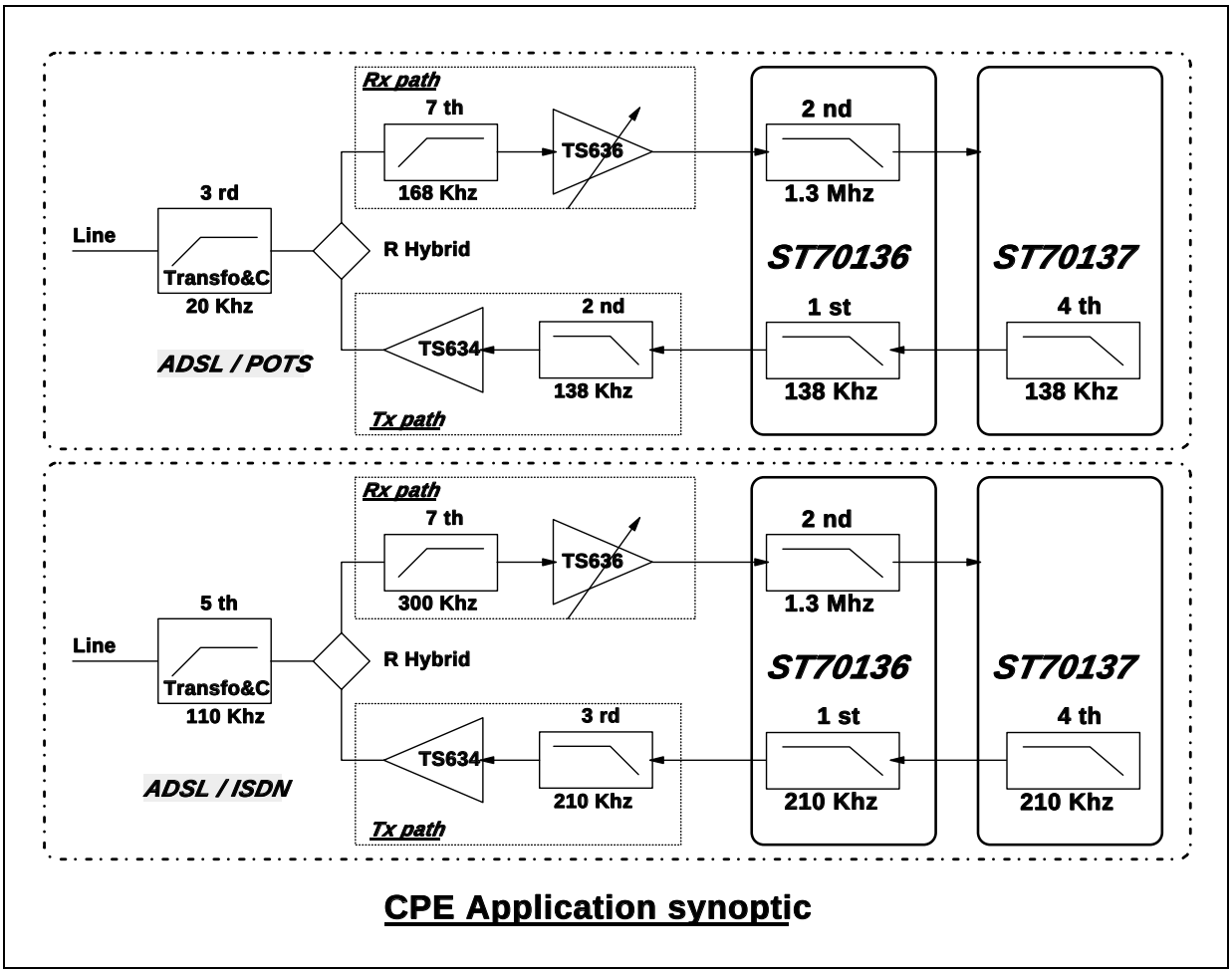
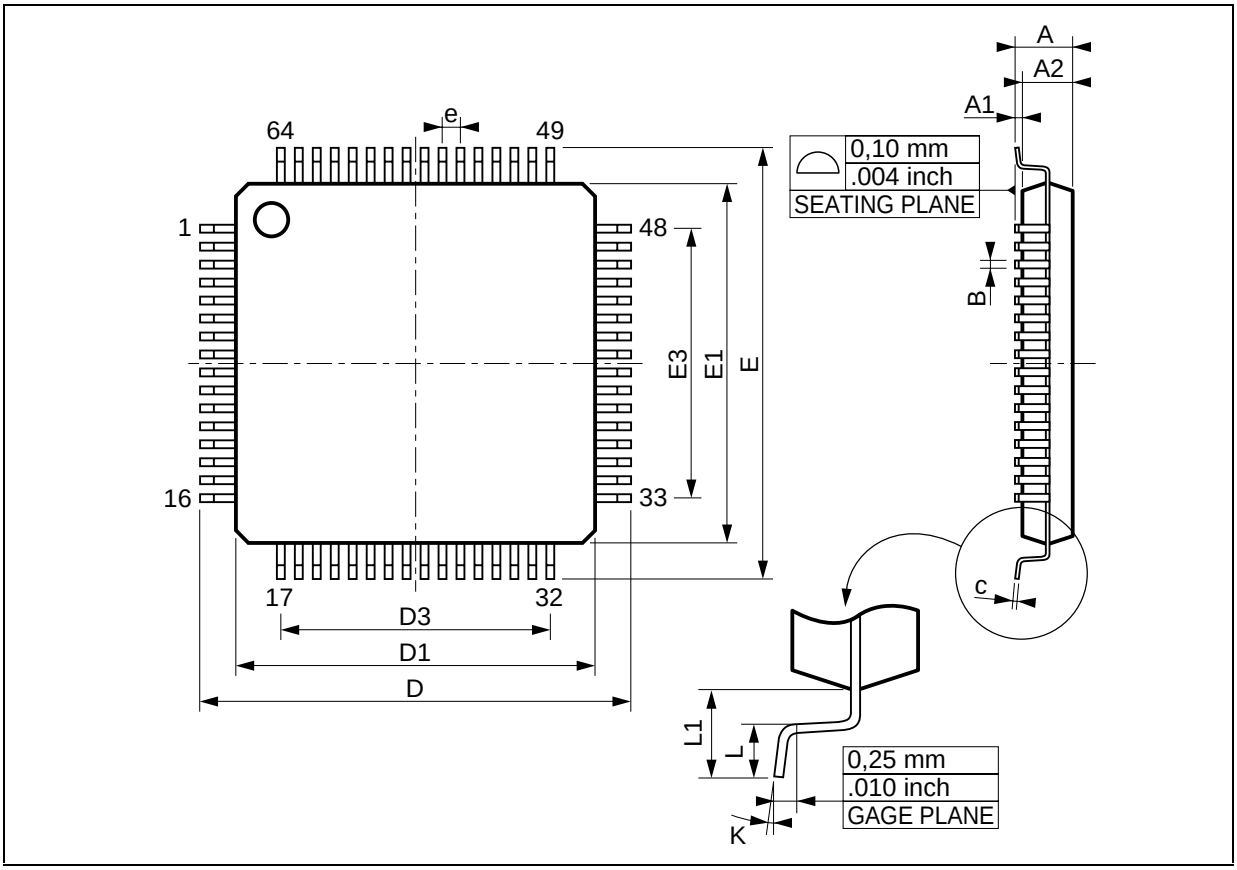


Figure 12 : CPE Application Synoptic



6 - PACKAGE MECHANICAL DATA

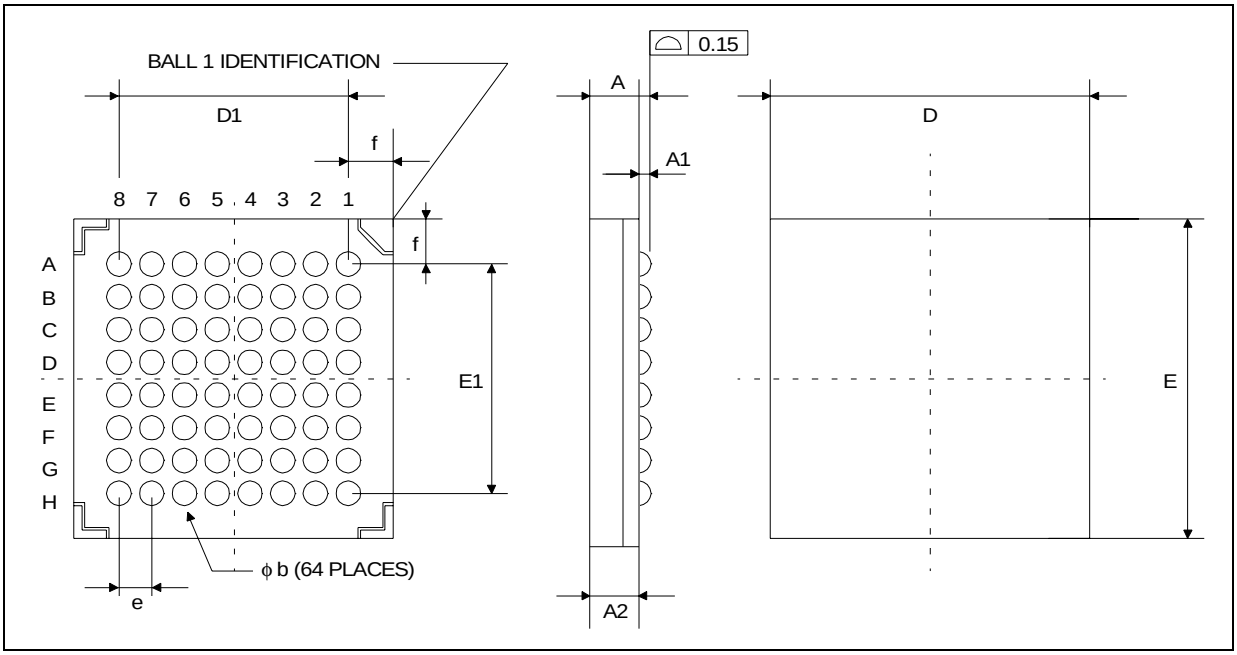
Figure 13 : Package TQFP64 Full Plastic (10 x 10 x 1.40 mm)



Dimensions	Millimeters			Inches (approx)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00	1		0.394	
E3		7.50			0.295	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (Minimum), 7° (Maximum)					

7 - PACKAGE MECHANICAL DATA

Figure 14 : Package LFBGA64 (8 x 8 x 1.7 mm)



Dimensions	Millimeters			Inches (approx)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			1.700			0.067
A1	0.350	0.400	0.450	0.014	0.016	0.018
A2		1.100			0.043	
b		0.500			0.20	
D		8.000			0.315	
D1		5.600			0.220	
e		0.800			0.031	
E		8.000			0.315	
E1		5.600			0.220	
f		1.200			0.047	