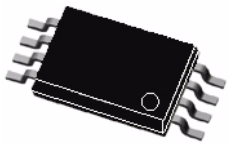
STC5DNF30V

Dual N-channel 30V - 0.032Ω - 4.5A - TSSOP8
2.7V-Driver STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STC5DNF30V	30V	< 0.035Ω (@4.5V) < 0.040Ω (@2.7V)	4.5A

- Standard outline for easy automated surface mount assembly
- Ultra low threshold gate drive (2.7V)

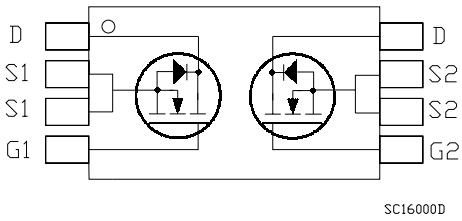


TSSOP8

Description

This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility. No electrical connections are shared between mosfets.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STC5DNF30V	C5DNF30V	TSSOP8	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate- source voltage	± 8	V
I_D (1)	Drain current (continuous) at T_C = 25°C	4.5	A
I_D (1)	Drain current (continuous) at T_C = 100°C	2.8	A
I_{DM}(2)	Drain current (pulsed)	18	A
P_{TOT} (1)	Total dissipation at t_c = 25°C	1.3	W

1. When mounted on FR-4 board with 1inch² pad, 2 Oz of Cu and t<10sec.
2. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-pcb(1)	Thermal resistance junction-pcb max	120	°C/W
Rthj-pcb(2)	Thermal resistance junction-pcb max	97.5	°C/W
T_j	Operating junction temperature	-55 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. When mounted on minimum recommended footprint.
2. When mounted on FR-4 board with 1inch² pad, 2 Oz of Cu and t<10sec.

2 Electrical characteristics

(T_J =25°C unless otherwise specified)

Table 3. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating,T_C=125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 8V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 4.5V, I_D = 2.3A V_{GS} = 2.7V, I_D = 2.3A		0.032 0.036	0.035 0.040	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} =25V , I_D = 2.3A		9.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		460 200 50		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 16V, I_D = 4.5A, V_{GS} = 4.5V (see Figure 14)		8.5 1.8 2.4	11.5	ns ns ns

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 10V, I_D = 2.3A, R_G= 4.7Ω V_{GS} = 4.5V (see Figure 13)		7 33 27 10		ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 16V, I_D = 2.3A, R_G = 4.7Ω, V_{GS} = 4.5V (see Figure 17)		26 11 21		ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				4.5 18	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.5A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.5A, di/dt =100A/µs, V_{DD} = 10V, T_j = 150°C (see Figure 15)		26 13 1		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

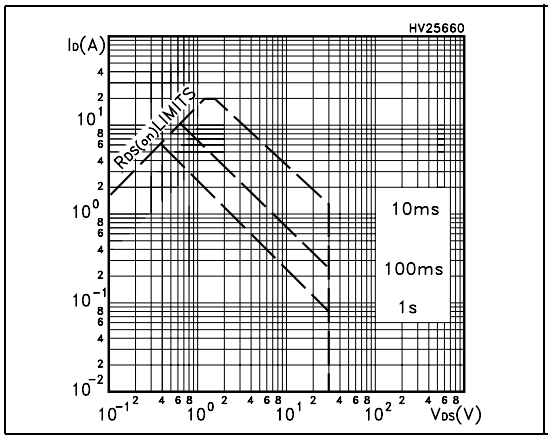


Figure 2. Thermal impedance

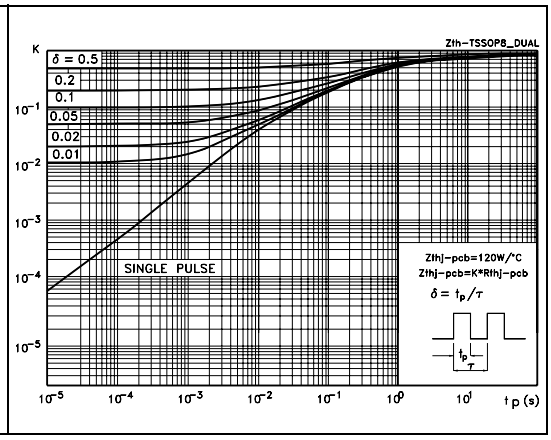


Figure 3. Output characteristics

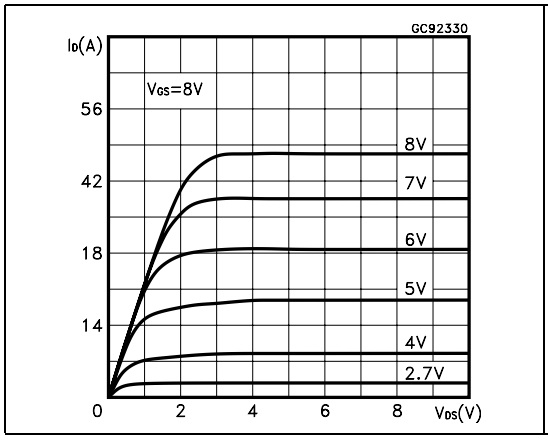


Figure 4. Transfer characteristics

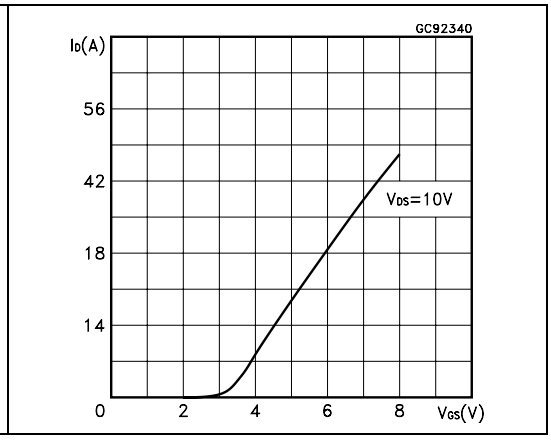


Figure 5. Transconductance

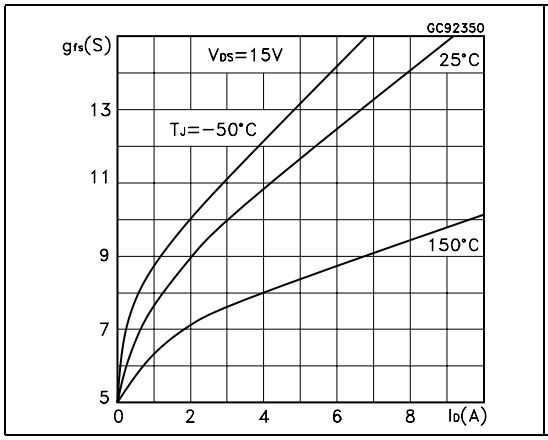


Figure 6. Static drain-source on resistance

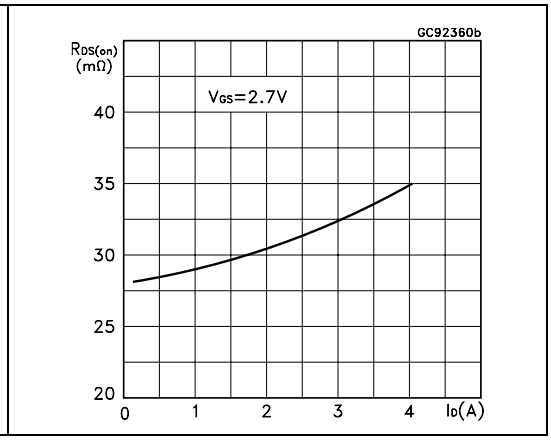


Figure 7. Gate charge vs gate-source voltage

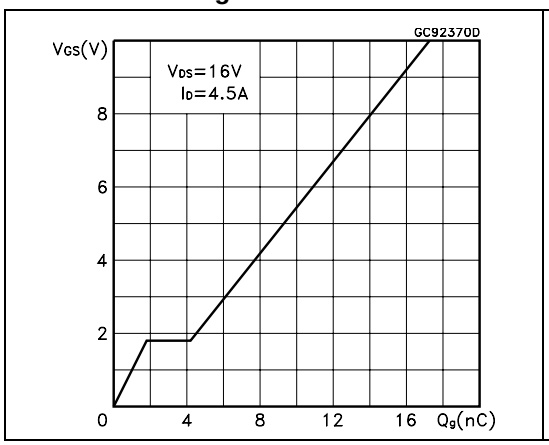


Figure 8. Capacitance variations

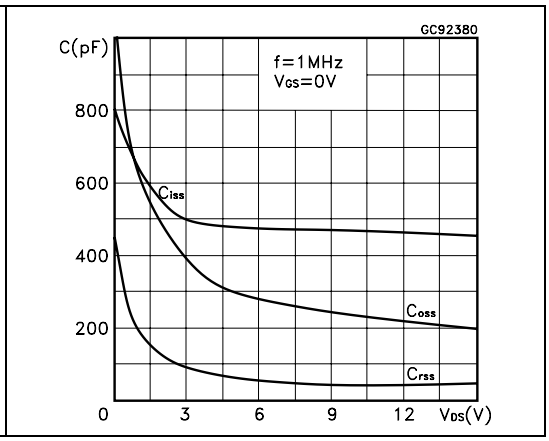


Figure 9. Normalized gate thereshold voltage vs temperature

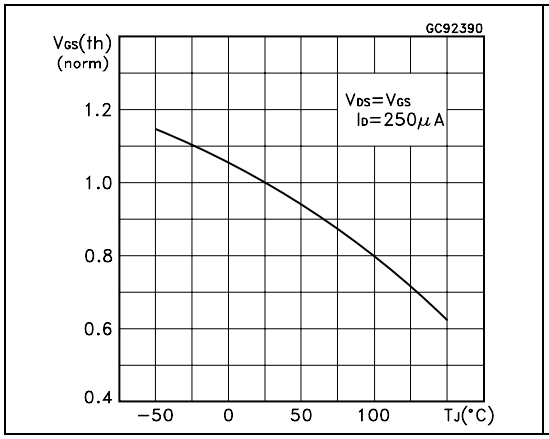


Figure 10. Normalized on resistance vs temperature

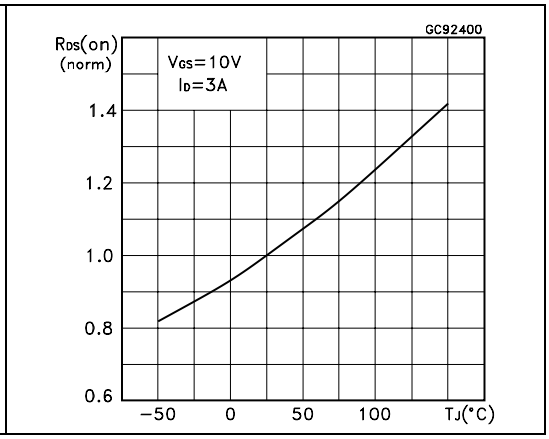


Figure 11. Source-drain diode forward characteristics

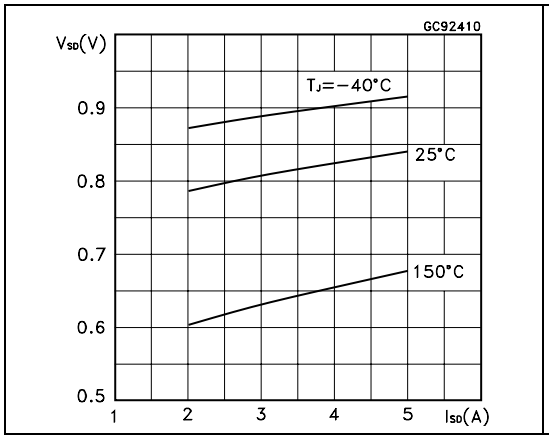
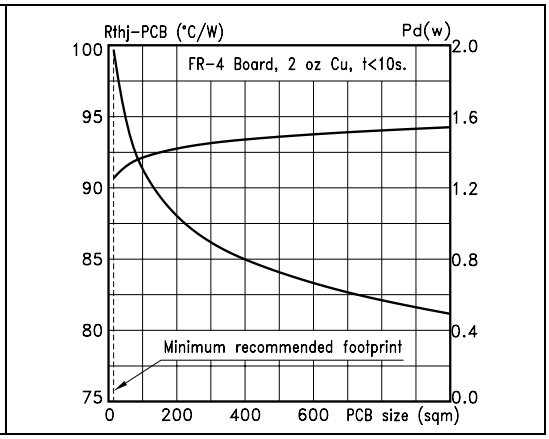


Figure 12. Thermal resistance and max power



3 Test circuits

Figure 13. Switching times test circuit for resistive load

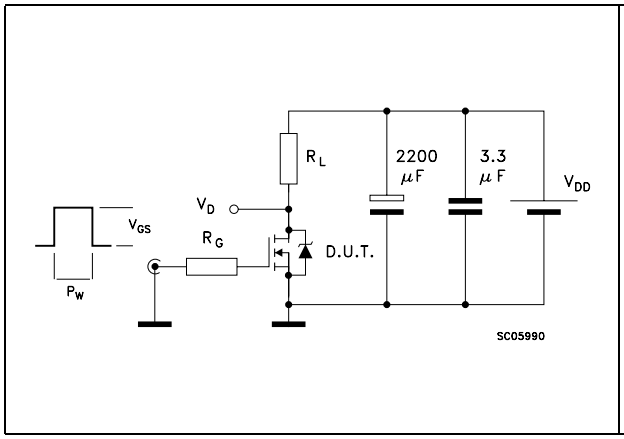


Figure 14. Gate charge test circuit

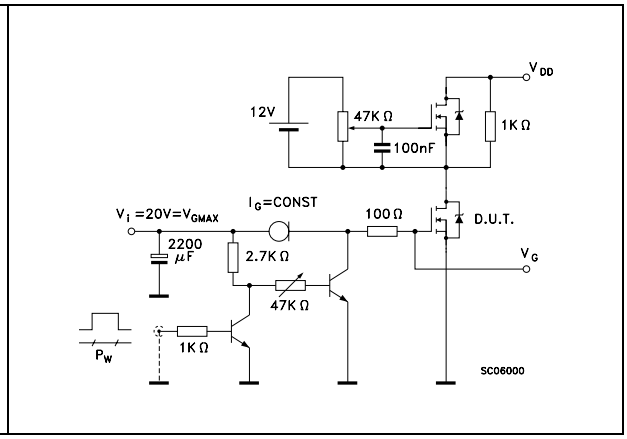


Figure 15. Test circuit for inductive load switching and diode recovery times

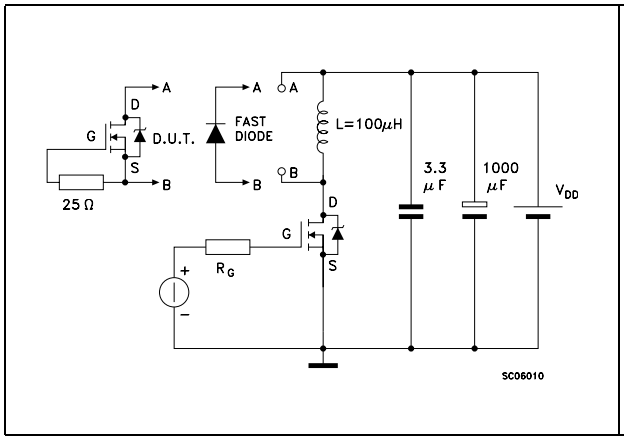


Figure 16. Unclamped inductive load test circuit

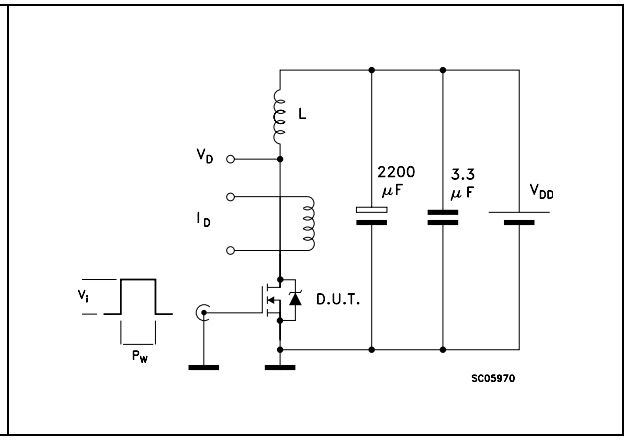
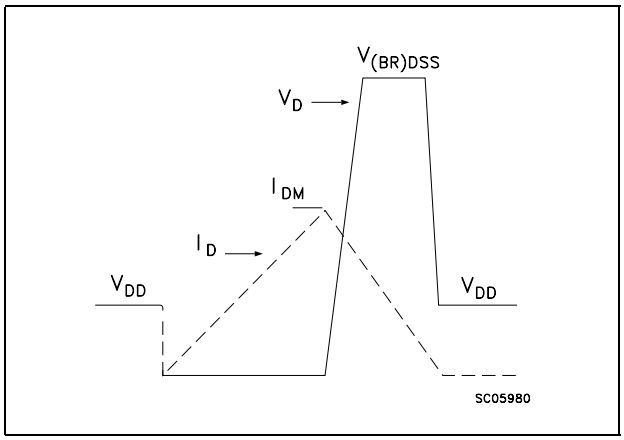


Figure 17. Unclamped inductive waveform

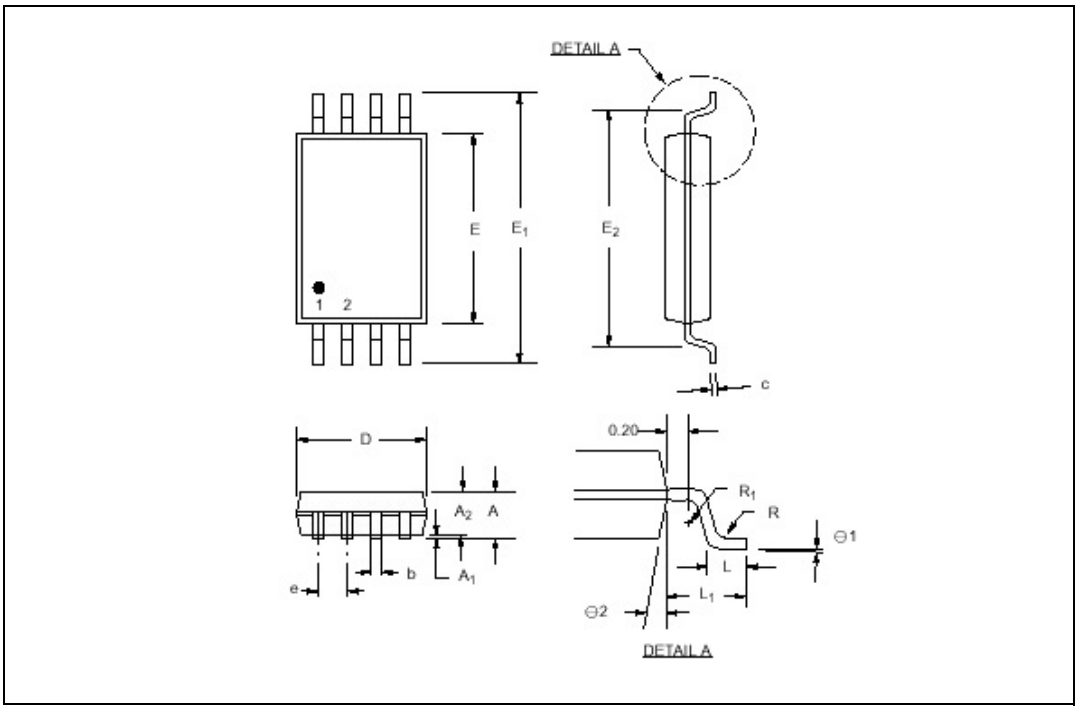


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TSSOP8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.05		1.20	0.041		0.047
A1	0.05		0.15	0.002		0.006
A2	0.80		1.05	0.032		0.041
b	0.19		0.30	0.008		0.012
c		0.127			0.005	
D	2.90		3.10	0.114		0.122
E	4.30		4.50	0.170		0.177
E1	6.20		6.60	0.240		0.260
E2	5.14		5.24	0.202		0.206
e		0.65			0.025	
L	0.45		0.75	0.018		0.030
L1	0.90		1.10	0.0355		0.0433
R	0.09			0.004		
R1	0.09			0.004		
θ1	0°		8°	0°		8°
θ2	12°					



5 Revision history

Table 7.

Date	Revision	Changes
11-Apr-2006	1	First release

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