STD110NH02L

N-CHANNEL 24V - 0.0044 Ω - 80A DPAK STripFET™ III POWER MOSFET

| TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD110NH02L	24 V	< 0.005 Ω	80 A(2)

- TYPICAL R_{DS}(on) = 0.0044 Ω @ 10 V
- TYPICAL R_{DS}(on) = 0.0056 Ω @ 5 V
- $R_{DS(ON)}$ * Qg INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

DPAK
TO-252
(Suffix "T4")

DESCRIPTION
The STD110NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable fot the most demanding DC-DC converter application where high efficiency is to be achieved.
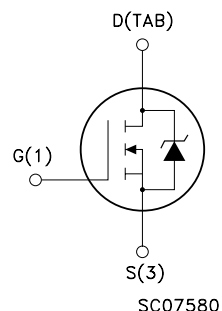
APPLICATIONS
- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTES
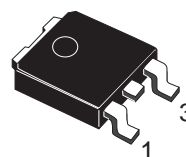
INTERNAL SCHEMATIC DIAGRAM

SC07580

Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD110NH02LT4	D110NH02L	TO-252	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{spike(1)}$	Drain-source Voltage Rating	30	V
V_{DS}	Drain-source Voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate- source Voltage	± 20	V
I_D(2)	Drain Current (continuous) at T_C = 25°C	80	A
I_D(2)	Drain Current (continuous) at T_C = 100°C	80	A
I_{DM}(3)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_C = 25°C	125	W
	Derating Factor	0.83	W/°C
E_{AS} (1)	Single Pulse Avalanche Energy	900	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.20	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)
OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 25 mA, V_{GS} = 0	24			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 20 V V_{DS} = 20V T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON [5]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 40 A V_{GS} = 5 V I_D = 20 A		0.0044 0.0050	0.0050 0.0095	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} [5]	Forward Transconductance	V_{DS} = 10 V I_D = 40 A		52		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 15V f = 1 MHz V_{GS} = 0		4450 1126 141		pF pF pF
R_G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.6		Ω

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 10 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		14 224		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 10 V I_D= 80 A V_{GS}= 10 V		69 13 9	93	nC nC nC
Q_{oss}(6)	Output Charge	V_{DS}= 16 V V_{GS}= 0 V		27		nC
Q_{gls}(7)	Third-quadrant Gate Charge	V_{DS}< 0 V V_{GS}= 10 V		64		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 10 V I_D = 40 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 3)		69 40	54	ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 40 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 80 A di/dt = 100A/μs V_{DD} = 15 V T_j = 150°C (see test circuit, Figure 5)		47 58 2.5		ns nC A

(1) Garanted when external Rg=4.7 Ω and t_f < t_{fmax}.
(2) Value limited by wire bonding
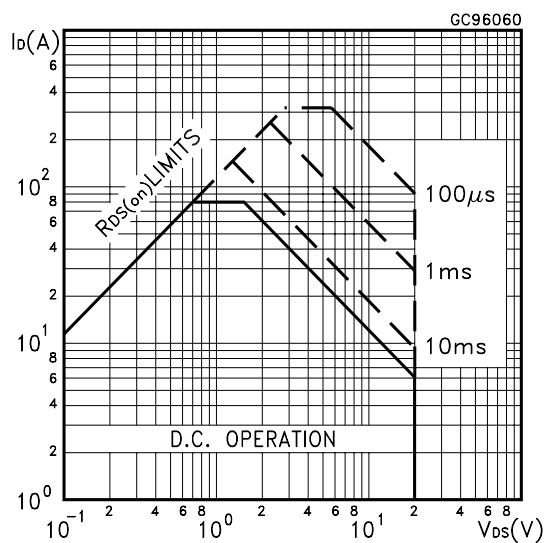(3) Pulse width limited by safe operating area.
(4) Starting T_j = 25 °C, I_D = 40A, V_{DD} = 10V   .
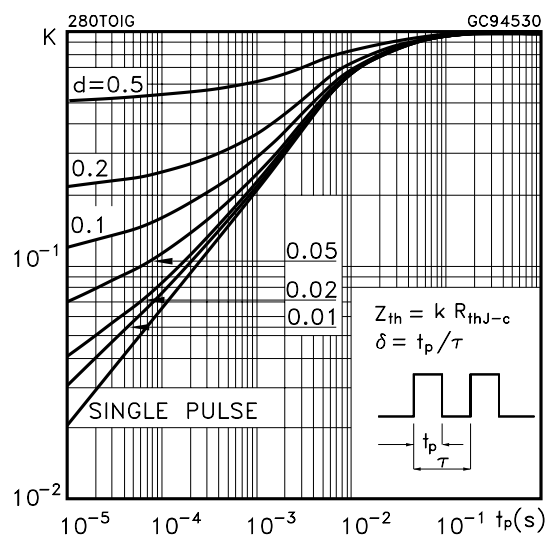
(5) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
(6) Q_{oss} = C_{oss}*Δ V_{in} , C_{oss} = C_{gd} + C_{ds} . See Appendix A
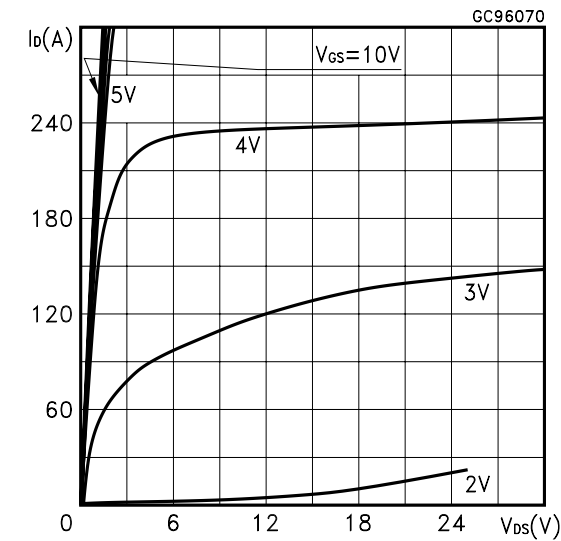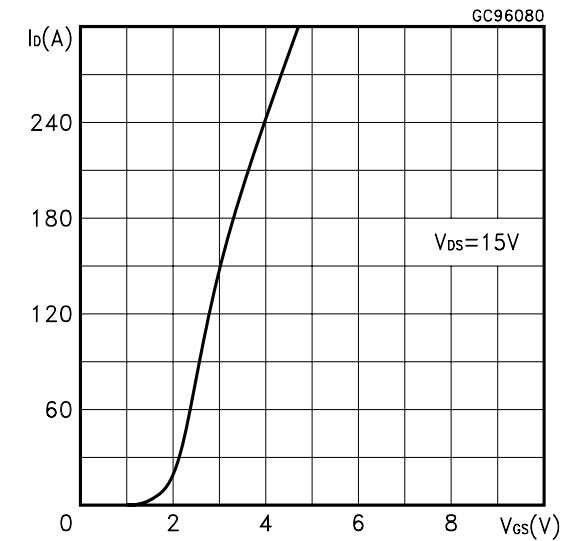(7) Gate charge for synchronous operation
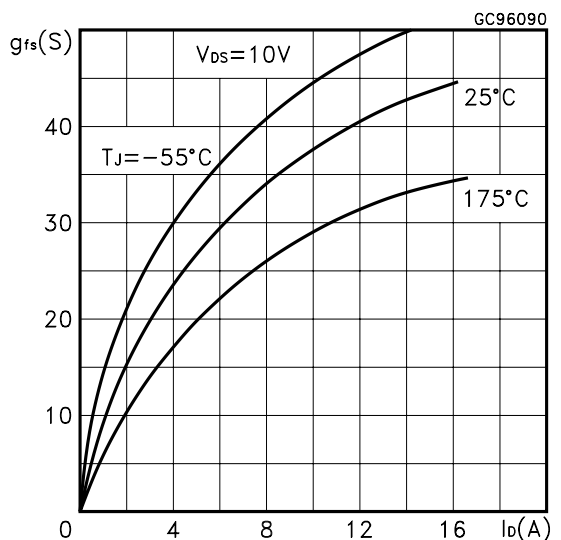
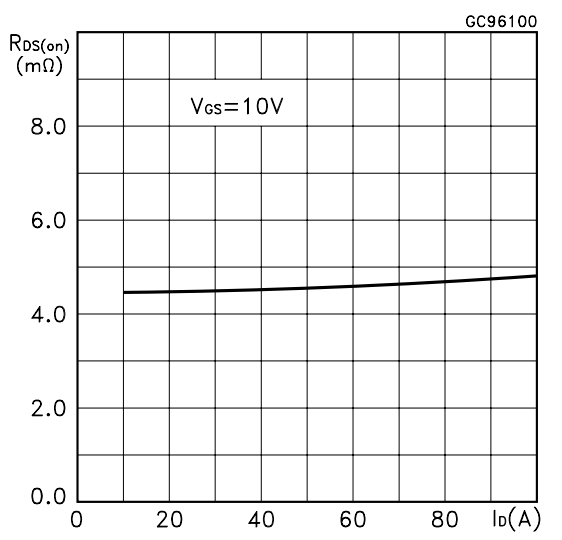Safe Operating Area

Thermal Impedance

Output Characteristics

GC96070

$I_D(A)$

$V_{GS}=10V$

5V

240

4V

180

3V

120

60

2V

0   6   12   18   24 $V_{DS}(V)$

Transfer Characteristics

GC96080

$I_D(A)$

240

180

$V_{DS}=15V$

120

60

0   2   4   6   8 $V_{GS}(V)$

Transconductance

GC96090

$g_{fs}(S)$

$V_{DS}=10V$

25°C

40

$T_J=-55°C$

175°C

30

20

10

0   4   8   12   16 $I_D(A)$

Static Drain-source On Resistance

GC96100

$R_{DS(on)}$ (mΩ)

$V_{GS}=10V$

8.0

6.0

4.0

2.0

0.0

0   20   40   60   80 $I_D(A)$

Gate Charge vs Gate-source Voltage

GC96110

$V_{GS}(V)$

$V_{DS}=10V$
$I_D=80A$

12

9

6

3

0   20   40   60   80 $Q_g(nC)$
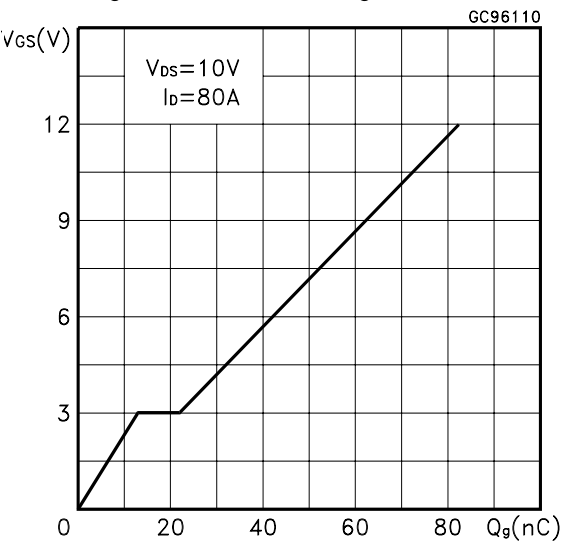
Capacitance Variations

GC96120

$C(pF)$

$f=1MHz$
$V_{GS}=0V$

8000

6000

C_{iss}

4000

2000

C_{oss}

C_{rss}

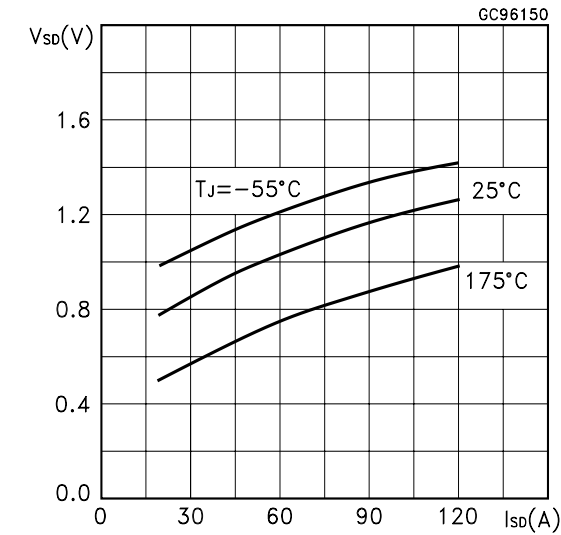0   3   6   9   12 $V_{DS}(V)$

STD110NH02L
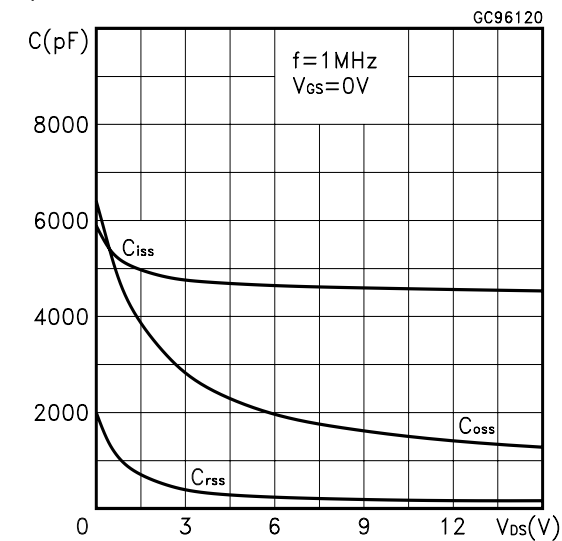
Normalized Gate Threshold Voltage vs Temperature
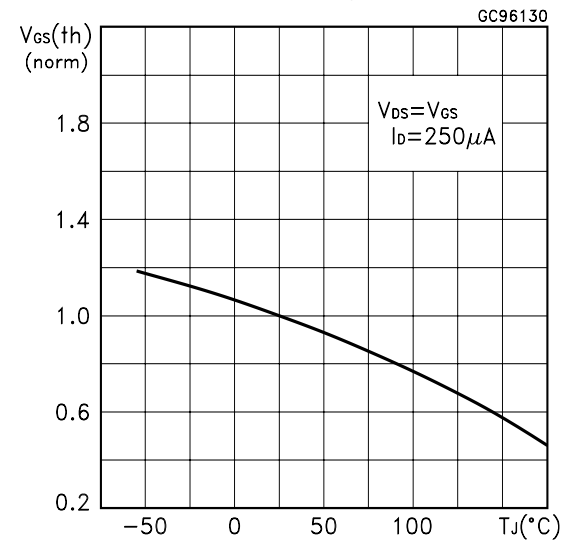
Normalized on Resistance vs Temperature
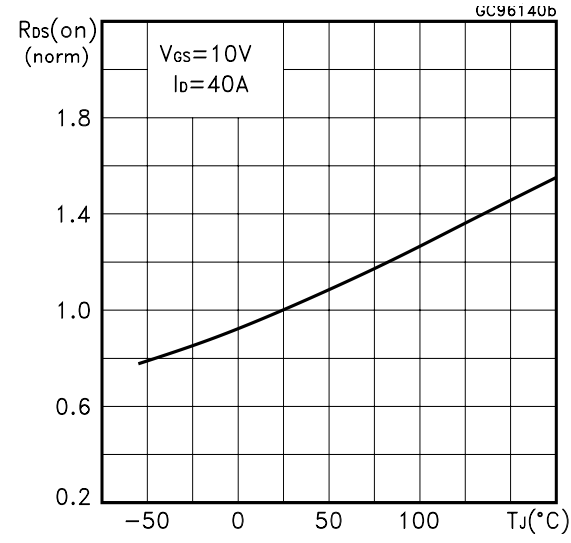
Source-drain Diode Forward Characteristics

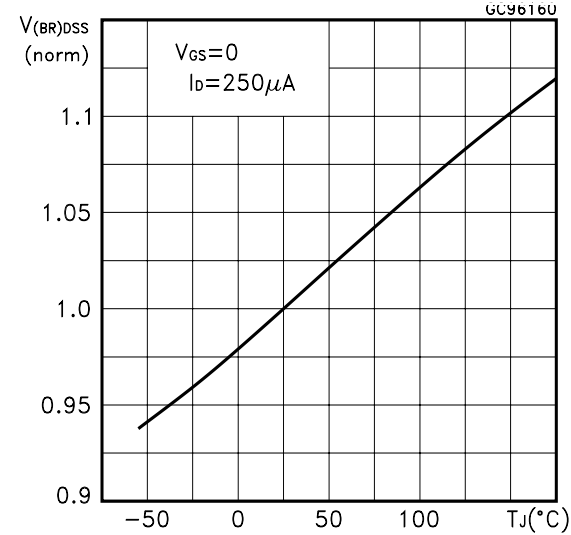

Normalized Breakdown Voltage vs Temperature

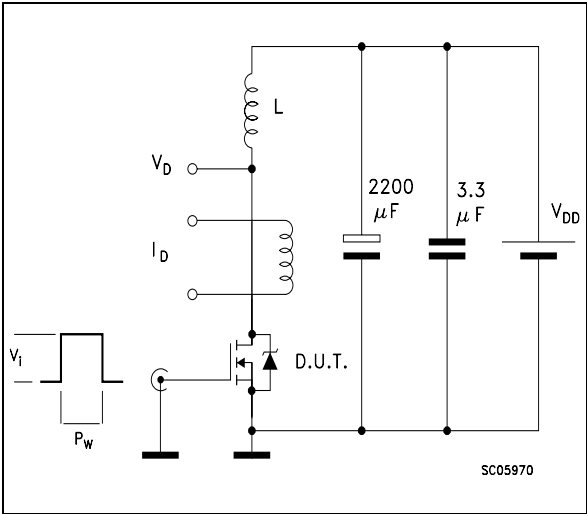**Fig. 1:** Unclamped Inductive Load Test Circuit
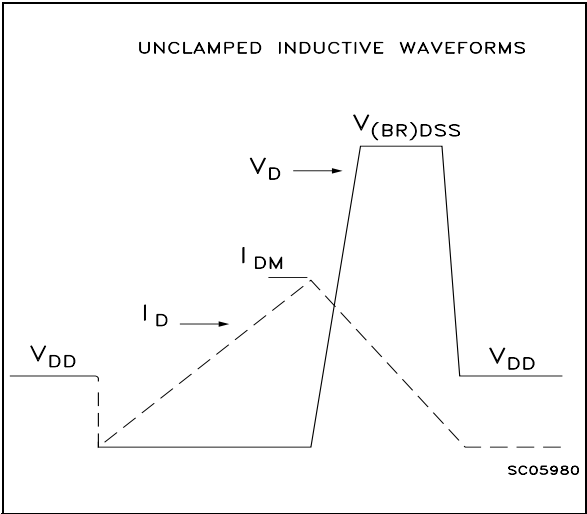

Fig. 2: Unclamped Inductive Waveform

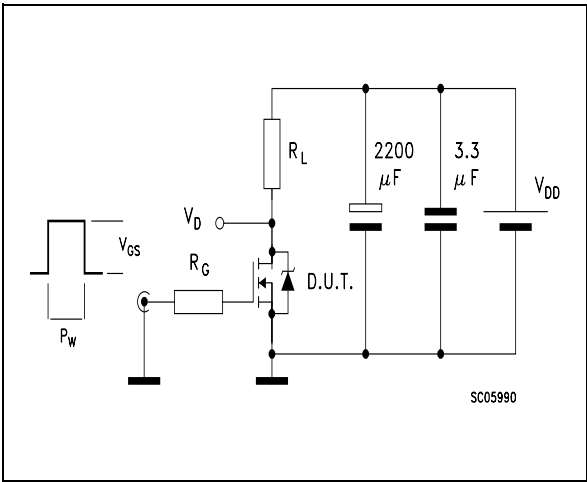**Fig. 3:** Switching Times Test Circuits For Resistive Load

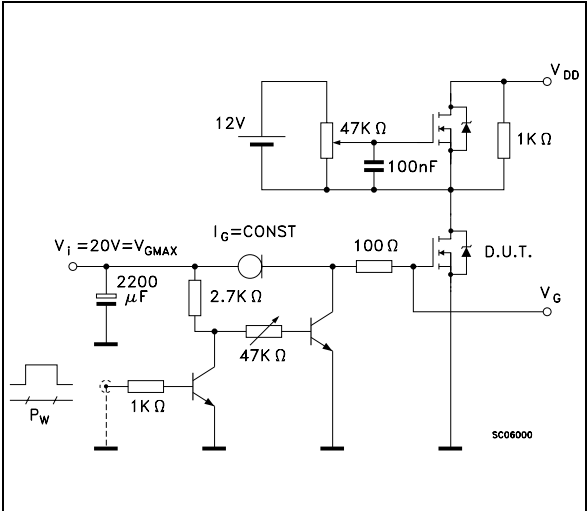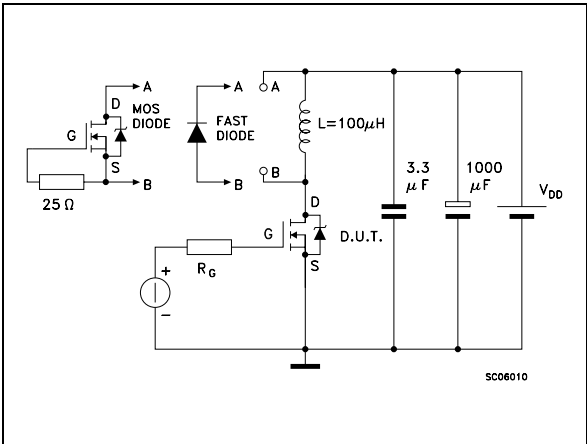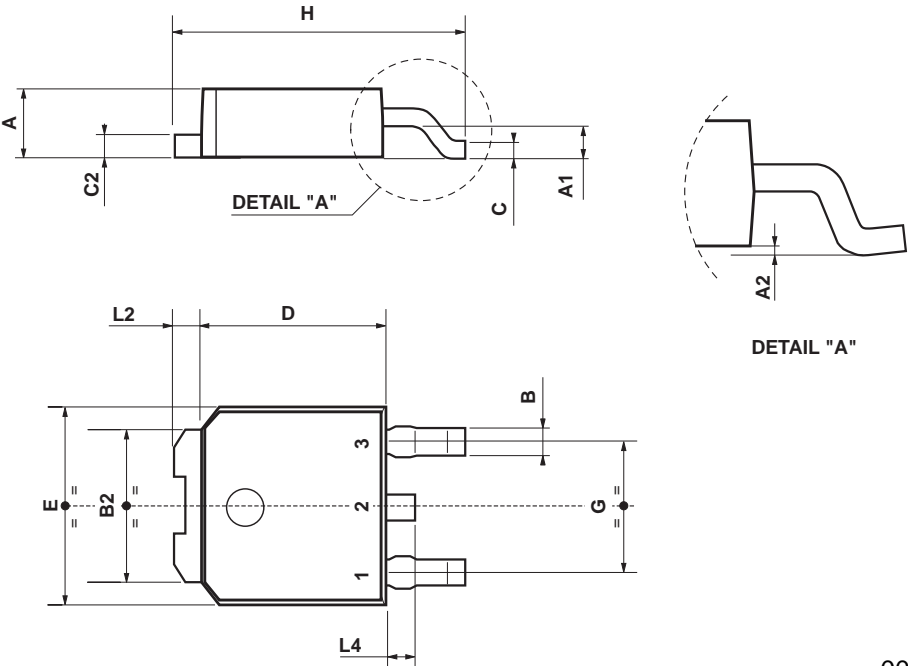**Fig. 4:** Gate Charge test Circuit

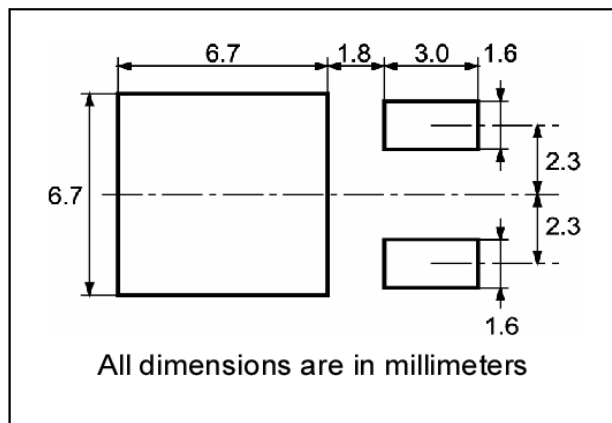**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039

0068772-B

DPAK FOOTPRINT

All dimensions are in millimeters

TUBE SHIPMENT (no suffix)*

BASE QTY
75

BULK QTY
3000

Tube length 532 (±0.5)

All dimensions are in millimeters
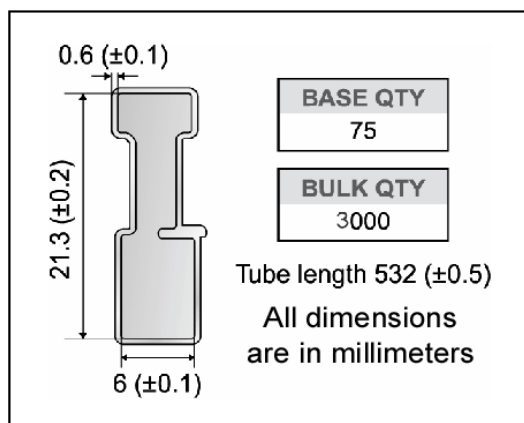
TAPE AND REEL SHIPMENT (suffix "T4")*

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

APPENDIX A
Buck Converter: Power Losses Estimation
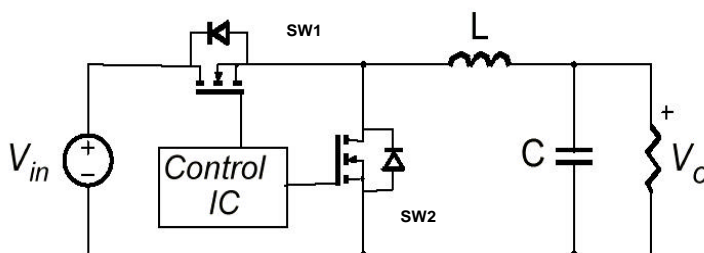
The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (**SW2**) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW_1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (**SW1**) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * d$	$R_{DS(on)SW2} * I_L^2 * (1-d)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \dfrac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$^1 V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_G)}$		$Q_{g(SW1)} * V_{gg} * f$	$\mathbf{Q_{gls(SW2)} * V_{gg} * f}$
P_{Qoss}		$\dfrac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\dfrac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

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[1] Dissipated by SW1 during turn-on

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