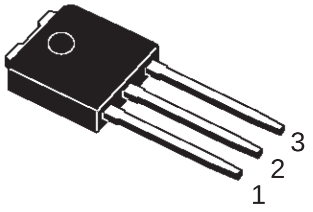
STD5NE10

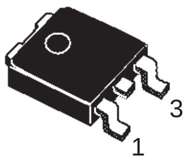
N - CHANNEL 100V - 0.32 Ω - 5A TO-251/TO-252 STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD5NE10	100 V	< 0.4 Ω	5 A

- TYPICAL $R_{DS(on)}$ = 0.32 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- AVALANCHE TESTED
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION
- ADD SUFFIX ”T4” FOR ORDERING IN TAPE & REEL



IPAK
TO-251
(Suffix ”-1”)



DPAK
TO-252
(Suffix ”T4”)

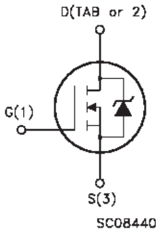
DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique ”Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- MOTOR CONTROL (DISK DRIVES, etc.)
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	5	A
I_D	Drain Current (continuous) at T_c = 100 °C	3.5	A
I_{DM}(•)	Drain Current (pulsed)	20	A
P_{tot}	Total Dissipation at T_c = 25 °C	25	W
	Derating Factor	0.17	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	0.6	V/ns
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \le 5A$, $di/dt \le 200$ A/µs, $V_{DD} \le V_{(BR)DSS}$, $Tj \le T_{JMAX}$

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	6	^{o}C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	100	^{o}C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink Typ	1.5	^{o}C/W
T_l	Maximum Lead Temperature For Soldering Purpose	275	^{o}C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 ^{o}C, $I_D = I_{AR}$, V_{DD} = 30V)	25	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^{o}C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 ^{o}C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (∗)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 2.5 A		0.32	0.4	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	5			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (∗)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 2.5 A		2.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		305 45 21		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 50 V I_D = 3.5 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, see fig. 3)		6.5 15		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 80 V I_D = 5 A V_{GS} = 10 V		14 6 4	18	nC nC nC

SWITCHING OFF

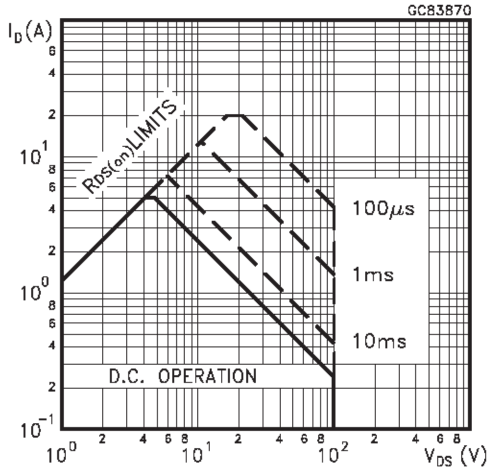
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 50 V I_D = 3.5 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, see fig. 3)		25 7		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 80 V I_D = 7 A R_G = 4.7 Ω V_{GS} = 10 V (Inductive Load, see fig. 5)		7 8 16		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				5 20	A A
V_{SD} (∗)	Forward On Voltage	I_{SD} = 8 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5 A di/dt = 100 A/µs V_{DD} = 50 V T_j = 150 °C (see test circuit, fig. 5)		75 210 5.5		ns nC A

(∗) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

Safe Operating Area for



Thermal Impedance