STF40NF06

N-CHANNEL 60V - 0.024Ω - 23A - TO-220FP
STripFET™II MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STF40NF06	60 V	< 0.028 Ω	23 A

- TYPICAL $R_{DS}(on)$ = 0.024Ω
- EXCEPTIONAL dv/dt CAPABILITY
- LOW GATE CHARGE AT 100°C
- APPLICATION ORIENTED CHARACTERIZATION
- 100% AVALANCHE TESTED

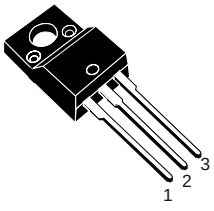
DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS

Figure 1: Package



TO-220FP

Figure 2: Internal Schematic Diagram

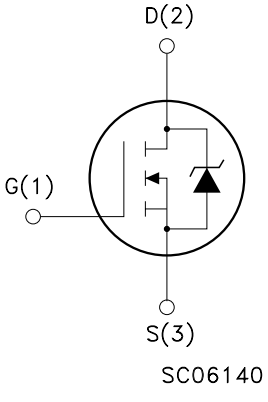


Table 2: Order Codes

Part Number	Marking	Package	Packaging
STF40NF06	F40NF06	TO-220FP	TUBE

Rev.2

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	23	A
I_D	Drain Current (continuous) at T_C = 100°C	16	A
I_{DM} (•)	Drain Current (pulsed)	92	A
P_{TOT}	Total Dissipation at T_C = 25°C	30	W
	Derating Factor	0.2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	10	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	250	mJ
V_{ISO}	Insulation Withstand Voltage (DC)	2500	V
T_{stg}	Storage Temperature	–55 to 175	°C
T_j	Operating Junction Temperature		

(1) $I_{SD} \leq 40A$, $di/dt \leq 300A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$.
(2) Starting T_j=25°C, I_D=20A, V_{DD}=30V
(•) Pulse width limited by safe operating area

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	5.0	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	275	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS}= Max Rating, T_C= 125°C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

Table 6: On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 11.5 A		0.024	0.028	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 30 V I_D =11.5A		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		920 225 80		pF pF pF

Table 8: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 30V, I_D = 20A R_G = 4.7Ω V_{GS} = 10V (see Figure 16)		27 11		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 48V, I_D = 10A, V_{GS} = 10V		32 6.5 15	43	nC nC nC

Table 9: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off-Delay Time Fall Time	V_{DD} = 30V, I_D = 20A, R_G=4.7Ω, V_{GS} = 10V (see Figure 16)		27 11		ns ns

Table 10: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				23	A
I_{SDM} (2)	Source-drain Current (pulsed)				92	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 23A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 40A, di/dt = 100A/µs, V_{DD} = 10V, T_j = 150°C (see test circuit, Figure 5)		63 150 4.8		ns nC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

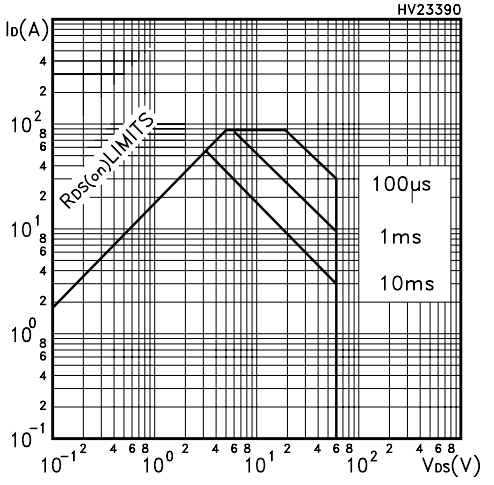


Figure 4: Output Characteristics

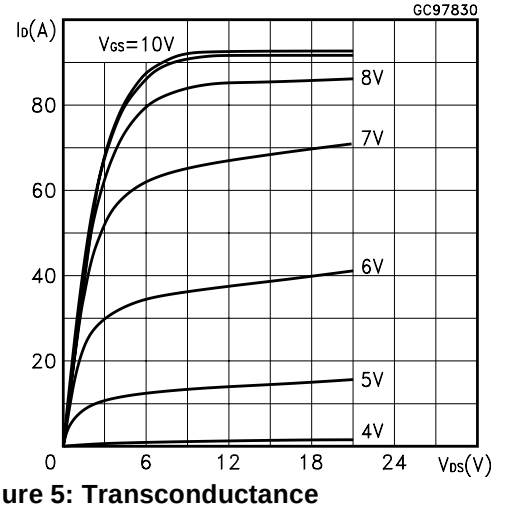


Figure 5: Transconductance

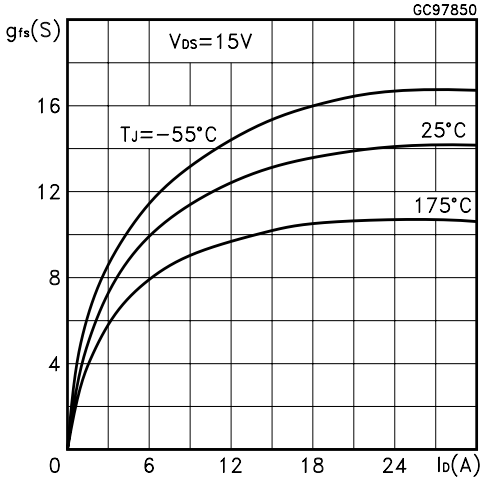


Figure 6: Thermal Impedance

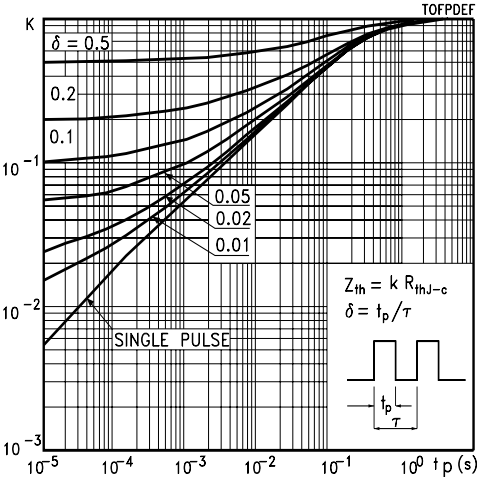


Figure 7: Transfer Characteristics

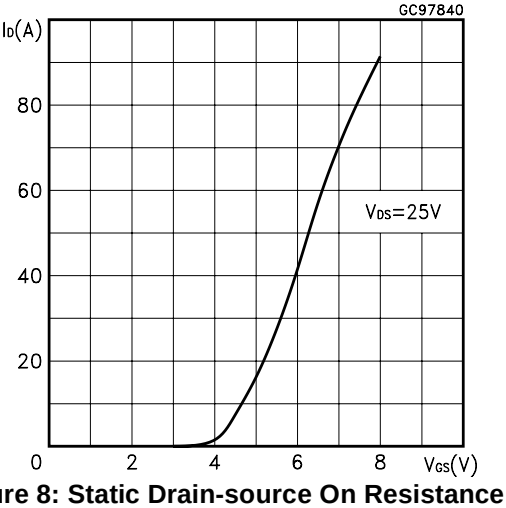


Figure 8: Static Drain-source On Resistance

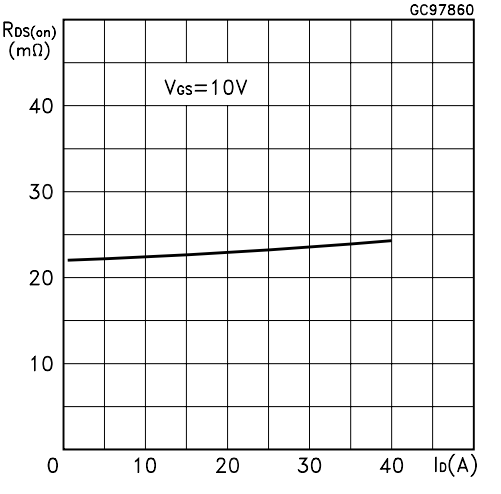


Figure 9: Gate Charge vs Gate-source Voltage

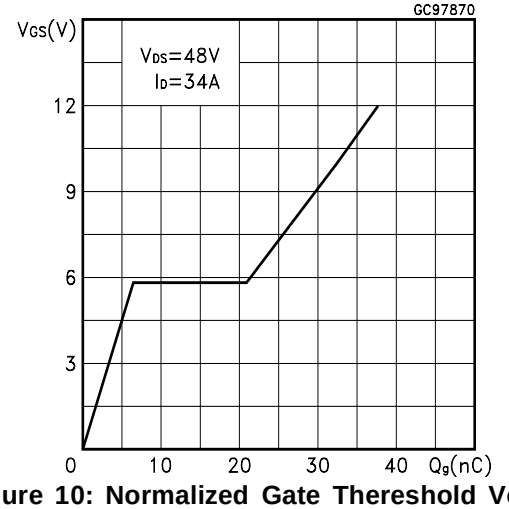


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

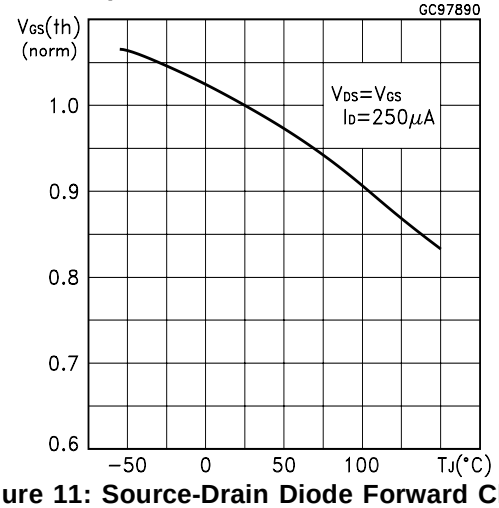


Figure 11: Source-Drain Diode Forward Characteristics

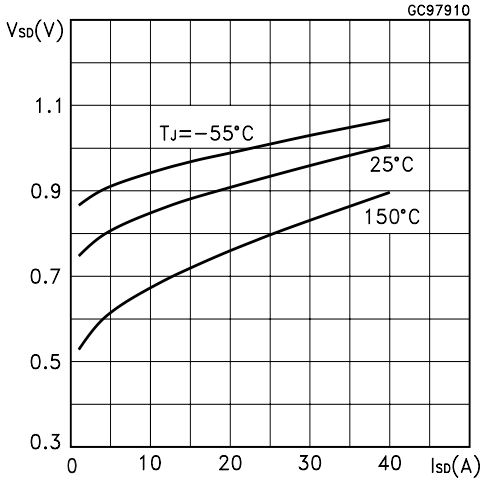


Figure 12: Capacitance Variations

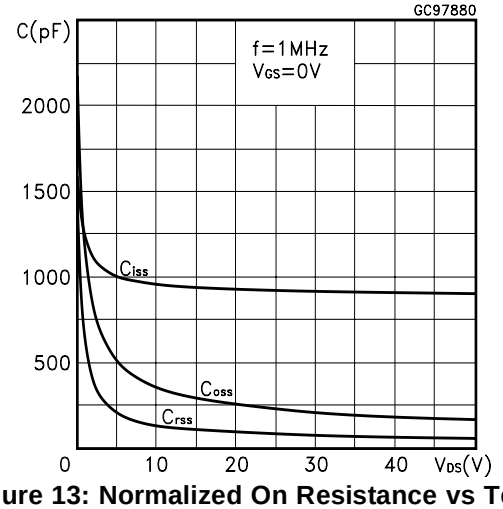


Figure 13: Normalized On Resistance vs Temperature

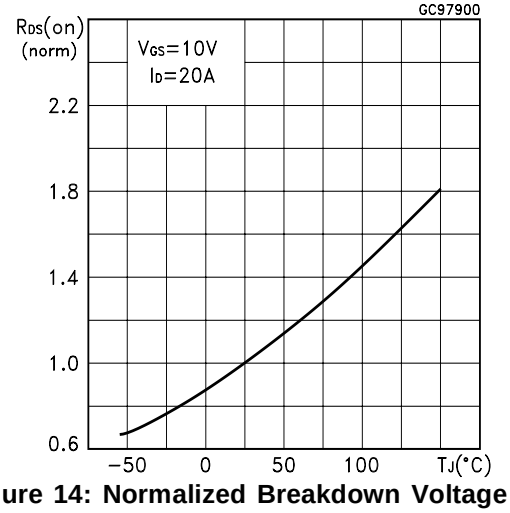


Figure 14: Normalized Breakdown Voltage vs Temperature

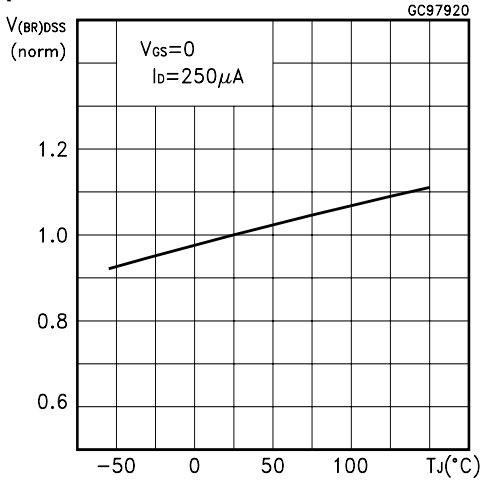


Figure 15: Unclamped Inductive Load Test Circuit

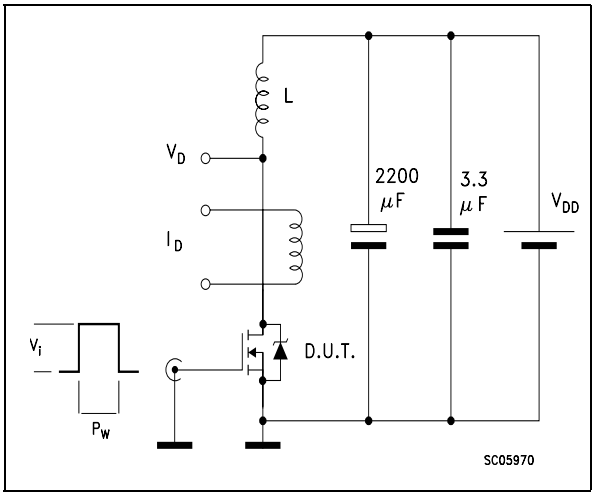


Figure 16: Switching Times Test Circuit For Resistive Load

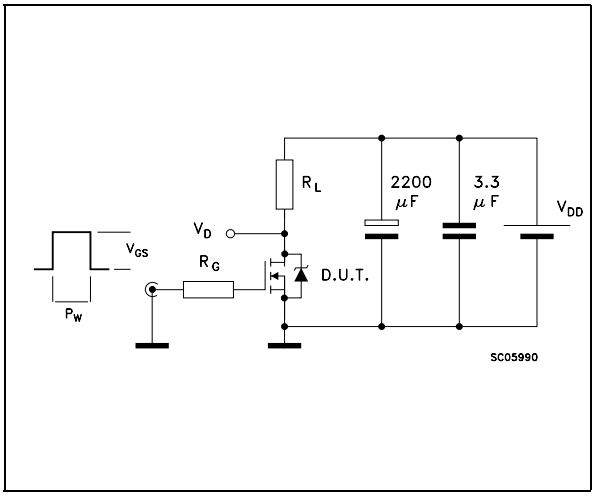


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

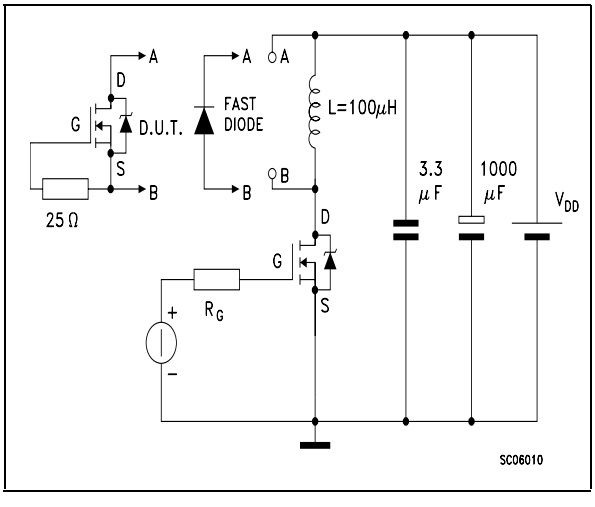


Figure 18: Unclamped Inductive Wafeform

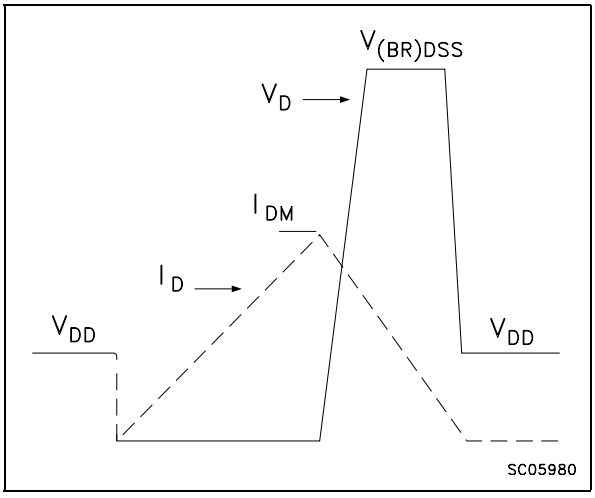
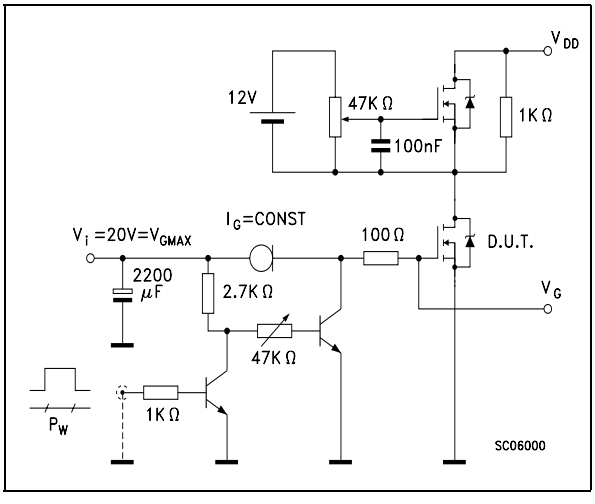


Figure 19: Gate Charge Test Circuit



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

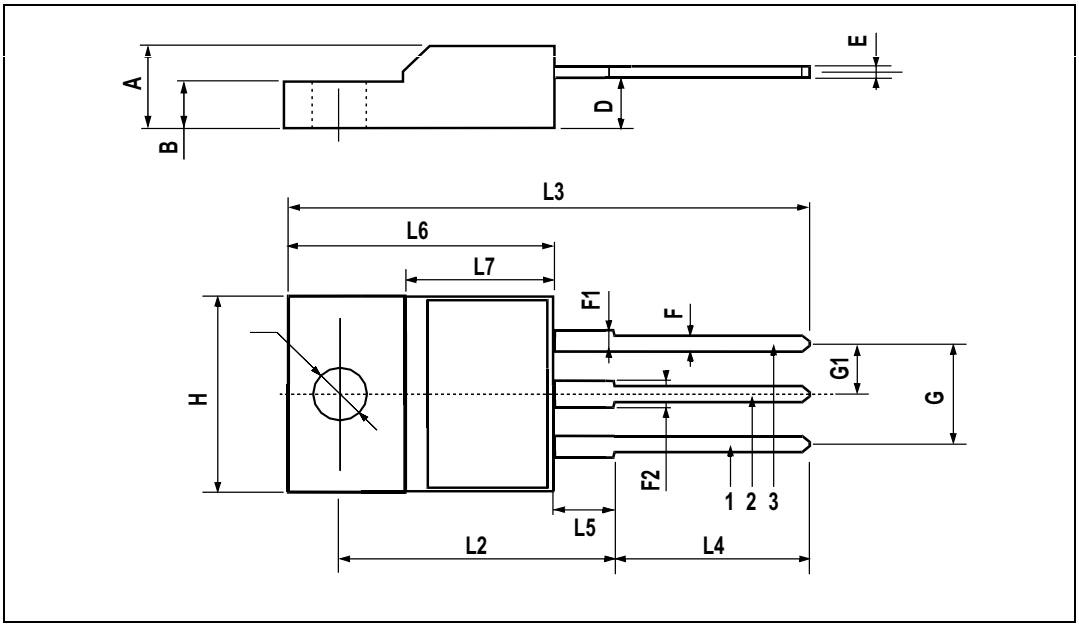


Table 11: Revision History

Date	Revision	Description of Changes
07-Oct-2004	1	First release
11-Nov-2004	2	Final datasheet