STL35NF10

N-CHANNEL 100V - 0.025Ω - 35A PowerFLAT™ LOW GATE CHARGE STripFET™ MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STL35NF10	100 V	< 0.030 Ω	35 A

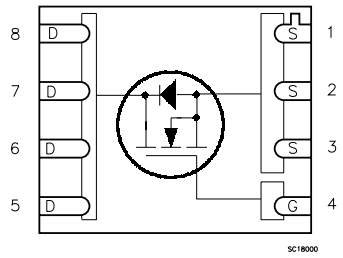
- TYPICAL $R_{DS}(on)$ = 0.025Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE

PowerFLAT™(6x5)
(Chip Scale Package)

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor shows extremely low on-resistance and minimal gate charge. The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH EFFICIENCY ISOLATED DC/DC CONVETERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuos) at T_C = 25°C Drain Current (continuos) at T_C = 100°C	35 22	A A
I_{DM} (●)	Drain Current (pulsed)	140	A
P_{TOT}	Total Dissipation at T_C = 25°C	80	W
	Derating Factor	0.64	W/°C
E_{AS} (1)	Single Pulse Avalanche Energy	135	mJ
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	–55 to 150	°C

(●) Pulse width limited by safe operating area

(1) Starting T_j = 25°C, I_D = 35A, V_{DD} = 50V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.56	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	2.8	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 17.5 A		0.025	0.030	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =20 V, I_D = 15 A		18		S
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1780		pF
C_{oss}	Output Capacitance			265		pF
C_{rss}	Reverse Transfer Capacitance			162		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 50 V, I_D = 17.5 A		28		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 1)		63		ns
Q_g	Total Gate Charge	V_{DD} = 80 V, I_D = 35 A,		60	80	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10 V		10		nC
Q_{gd}	Gate-Drain Charge	(see test circuit, Figure 2)		23		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 50 V, I_D = 17.5 A,		84		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10 V (see test circuit, Figure 1)		28		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				35	A
I_{SDM} (1)	Source-drain Current (pulsed)				140	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 18 A, V_{GS} = 0			1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 35 A, di/dt = 100A/µs,		114		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 25 V, T_j = 150°C		456		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 3)		8		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Switching Times Test Circuit For Resistive Load

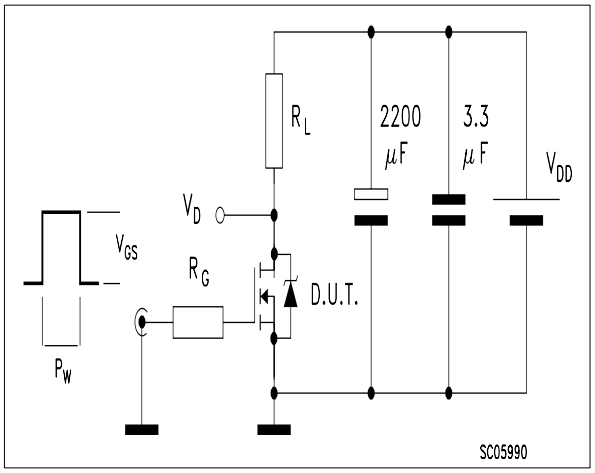


Fig. 2: Gate Charge test Circuit

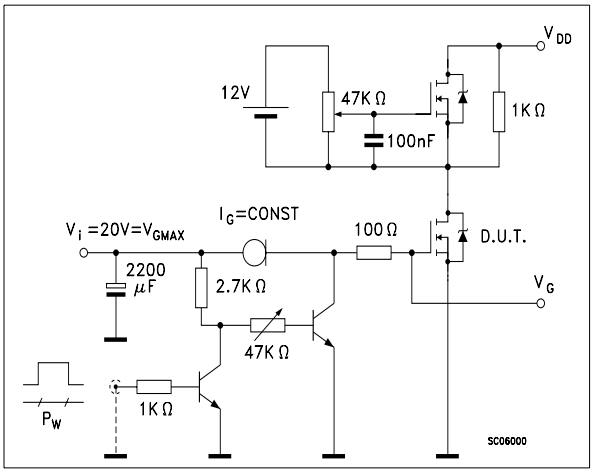
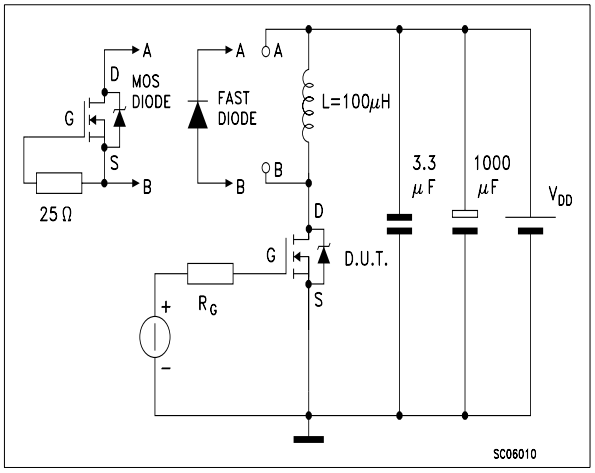


Fig. 3: Test Circuit For Diode Recovery Behaviour



PowerFLAT™(6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	0.031		0.039
A1		0.08			0.003	
b	0.36		0.48	0.014		0.018
D		4.89			0.191	
D2	3.95		4.05	0.154		0.158
E		6.00			0.235	
E2	2.95		3.05	0.115		0.119
e		1.27			0.049	
L	0.65		0.85	0.025		0.033