



STL8NH3LL

N-CHANNEL 30 V - 0.012 Ω - 8 A PowerFLAT™ ULTRA LOW GATE CHARGE STripFET™ MOSFET

PRELIMINARY DATA

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D (1)
STL8NH3LL	30 V	< 0.015 Ω	8 A

- TYPICAL R_{DS(on)} = 0.012 Ω @ 10V
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE
- LOW THRESHOLD DEVICE

DESCRIPTION

This application specific MOSFET is the latest generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

APPLICATIONS

- CONTROL FET IN BUCK CONVERTER

Figure 1: Package

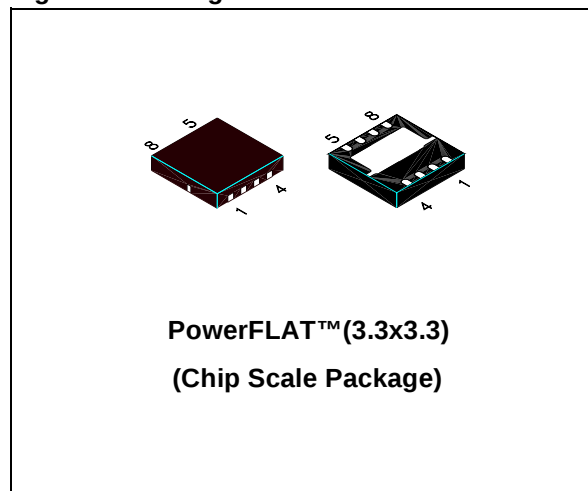


Figure 2: Internal Schematic Diagram

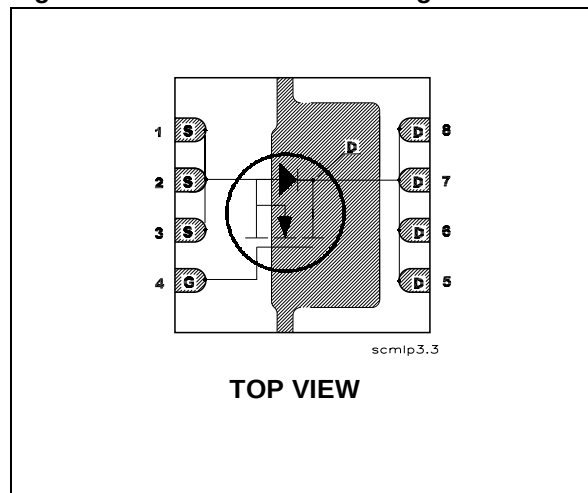


Table 2: Order Codes

Part Number	Marking	Package	Packaging
STL8NH3LL	L8NH3LL	PowerFLAT™ (3.3x3.3)	TAPE & REEL

Rev 2

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS}=0$)	30	V
V_{DGR}	Drain-gate Voltage ($R_{GS}=20\text{ k}\Omega$)	30	V
V_{GS}	Gate- source Voltage	± 16	V
$I_D(1)$	Drain Current (continuous) at $T_C=25^\circ\text{C}$ (Steady State)	8	A
$I_D(2)$	Drain Current (continuous) at $T_C=100^\circ\text{C}$ (Steady State)	5	A
$I_{DM}(3)$	Drain Current (pulsed)	32	A
$P_{TOT}(1)$	Total Dissipation at $T_C=25^\circ\text{C}$	50	W
$P_{TOT}(2)$	Total Dissipation at $T_C=25^\circ\text{C}$ (Steady State)	1.56	W
	Derating Factor (2)	0.4	W/ $^\circ\text{C}$
T_{stg}	Storage Temperature	– 55 to 150	$^\circ\text{C}$
T_j	Max. Operating Junction Temperature		

Table 4: Thermal Data

Rthj-Case	Thermal Resistance Junction-Case Max	2.5	$^\circ\text{C}/\text{W}$
Rthj-a (4)	Thermal Operating Junction-ambient	80	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_{CASE}=25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)**Table 5: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 4\text{ A}$		0.012 0.0135	0.015 0.017	Ω Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}(5)$	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 4\text{ A}$		TBD		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		965		pF
C_{oss}	Output Capacitance			285		pF
C_{rss}	Reverse Transfer Capacitance			38		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**Table 7: Switching On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{ V}$, $I_D=4\text{ A}$		15		ns
t_r	Rise Time	$R_G=4.7\Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 3)		32		ns
Q_g	Total Gate Charge	$V_{DD}=15\text{ V}$, $I_D=8\text{ A}$, $V_{GS}=4.5\text{ V}$ (see Figure 5)		9	12	nC
Q_{gs}	Gate-Source Charge			3.7		nC
Q_{gd}	Gate-Drain Charge			3		nC

Table 8: Switching

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD}=15\text{ V}$, $I_D=4\text{ A}$,		18		ns
t_f	Fall Time	$R_G=4.7\Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 3)		8.5		ns

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				8	A
$I_{SDM(3)}$	Source-drain Current (pulsed)				32	A
$V_{SD(5)}$	Forward On Voltage	$I_{SD}=8\text{ A}$, $V_{GS}=0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD}=8\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$		24		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=20\text{ V}$, $T_j=150^\circ\text{C}$		17.4		nC
I_{RRM}	Reverse Recovery Current	(see Figure 4)		1.45		A

(1) The value is rated according R_{thj-c} (2) The value is rated according R_{thj-a}

(3) Pulse width limited by safe operating area.

(4) When mounted on minimum footprint

(5) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Figure 3: Switching Times Test Circuit For Resistive Load

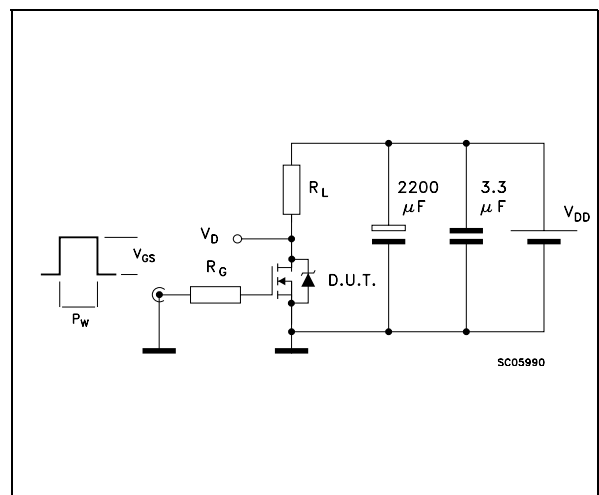


Figure 4: Test Circuit For Diode Recovery Times

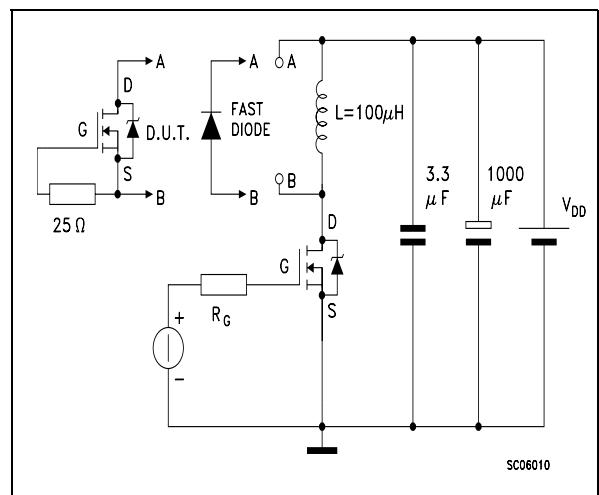
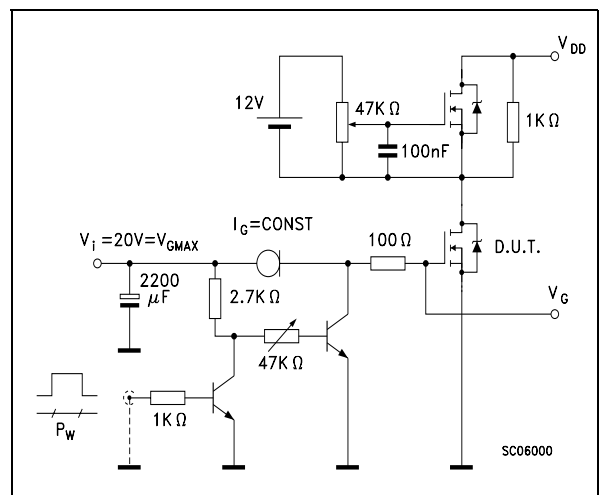


Figure 5: Gate Charge Test Circuit



PowerFLAT™ (3.3x3.3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.23	0.30	0.38	0.009	0.011	0.015
C		0.328			0.012	
C1		0.12			0.004	
D		3.30			0.13	
D2	2.50	2.65	2.75	0.098	0.104	0.108
E		3.30			0.13	
E2	1.25	1.40	1.50	0.049	0.055	0.059
F		1.325			0.052	
F1		0.975			0.038	
e		0.65			0.025	
L	0.30		0.50	0.011		0.019

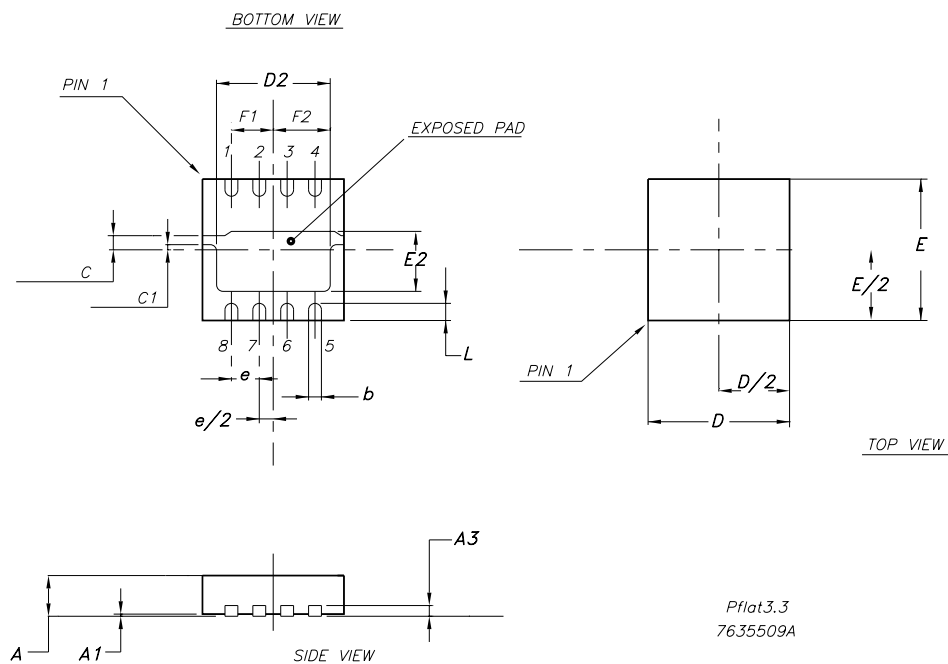


Table 10: Revision History

Date	Revision	Description of Changes
21-July-2004	1	First Release.
05-Oct-2004	2	Values changed

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