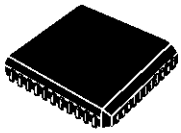
SGS-THOMSON MICROELECTRONICS

STLC5460

LINE CARD INTERFACE CONTROLLER

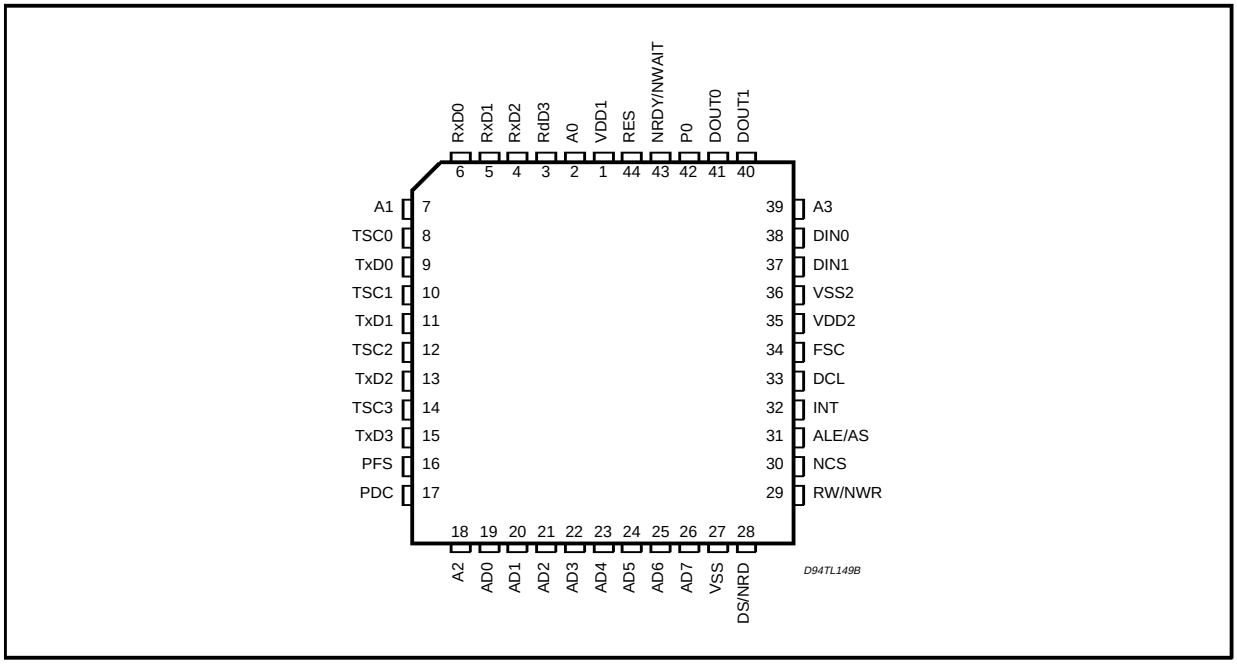
- BOARD CONTROLLER FOR UP TO 16 ISDN LINES OR 16 VOICE SUBSCRIBERS.
- TWO SERIAL INTERFACES :
  -PCM Four bidirectional multiplexes
  -GCI One (or two) at 2 Mb/s.
- NON BLOCKING SWITCH FOR 128 CHANNELS (16, 32 OR 64 KB/S BANDWIDTH).
- N CONSECUTIVE 64 kb/s CHANNELS FROM AN INPUT MULTIPLEX CAN BE SWITCHED AS A SINGLE N X 64 kbit/s CHANNEL TO AN OUTPUT MULTIPLEX AT 2048 kb/s.
- TIME SLOT ASSIGNMENT FREELY PROGRAMMABLE FOR EVERY CONNECTED SUBSCRIBER.
- PROGRAMMABLE PCM DATA RATES UP TO 8192 kb/s.CONSTANT DATA RATE AT 2 Mb/s ON GCI SIDE.
- PCM interface :
  - Simple and double clock frequency selectable;.
  - Programmable clock shift
  - Tristate mode control signals for external drivers.
- GCI interface :
  - Six bits or four bits Command/indicate channel selectable for analog or digital equipment
  - Command/Indicate Monitor channels validated or not
- Microprocessor access to two selected bidirectional channels of GCI and/or PCM.
- Multicontrollers for layer 1 functions :
  - C/I protocol controller for up to 16 C/I channels
  - Monitor protocol controller for up to 16 Monitor channels.
- Standard microprocessor interface with multiplexed address/data bus or separate address data buses.
- PLCC44 pins PACKAGE



PLCC44

ORDERING NUMBER: STLC5460

PIN CONNECTION (Top view)



DESCRIPTION

The Line Card Interface Controller, STLC5460, is a monolithic switching device for the path control of up to 128 channels of 16, 32, 64 kbps bandwidth. Two consecutive 64 kbps channels may also be handled as a quasi single 128 kbps channel. For these channels, the LCIC performs non-blocking space time switching between two serial interfaces: the system interface (or PCM interface) and the general component interface (GCI).

PCM interface can be programmed to operate at different data rates between 2048 and 8192 kbps. The PCM interface consists of up to four duplex ports with a tristate indication signal for each output line. The GCI interface can be selected to be PCM interface at 2Mbit/s.

The LCIC can be programmed to communicate with GCI compatible devices such as STLC3040 (SLIC), STLC5411 (U interface) and others. The device manages the layer 1 protocol buffering the Command/Indicate and Monitor channels for GCI compatible devices.

Due to its capability to switch channels of different bandwidths, the STLC5460 can handle up to 16 ISDN subscribers with their 2B+D channel structure in GCI configuration, or up to 16 analog subscribers. Since its interfaces can operate at different data rates, the LCIC is an ideal device for data rate adaptation between PCM interface up to 8Mb/s and GCI at 2Mb/s.

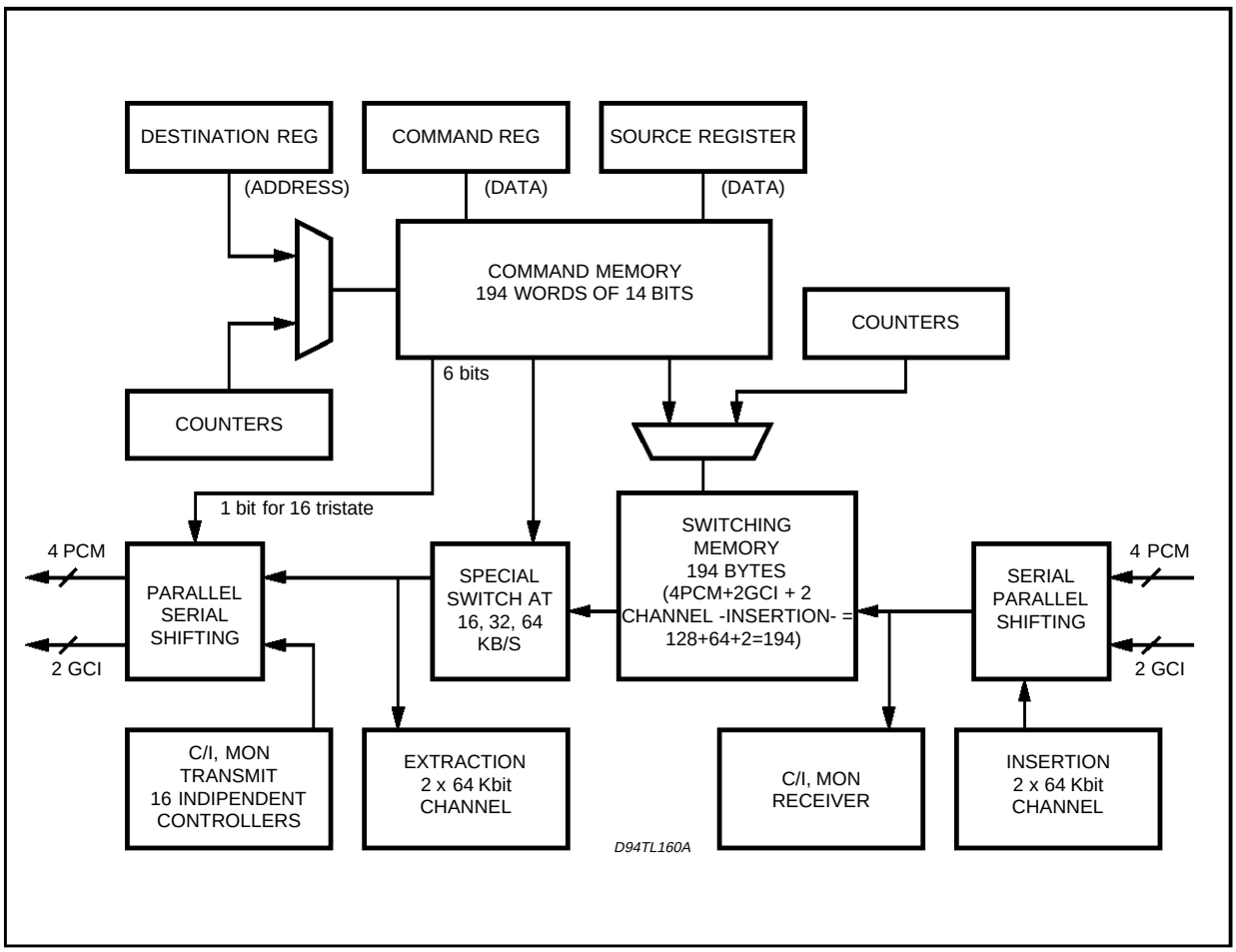
The device gives the possibility of checking the correct communication inside the PBX or Public Central Office providing :

- independent PCM delay setting
- PCM comparison function
- Pseudo Random Sequence Generator and Analyser.

Moreover, the LCIC is one of the key building blocks for networks with either central, distributed or mixed signaling and packet data handling architectures associated with ST5451 (HDLC controller).

The device is controlled by a standard 8 bit parallel microprocessor interface with a multiplexed address-data bus. The device may optionally be controlled by separate address and data buses.

BLOCK DIAGRAM



PIN DEFINITIONS AND FUNCTIONS

Symbol	Pin number	Type (*)	Function
VDD1	1	I	Supply Voltage 5V, ±5% .
A0	2	I (**)	Non Multiplexed Mode: this input interfaces to the system's address bus to select an internal register for a read or write access. Multiplexed Mode: A0 at VDD, NRDY/NWAIT pin delivers NWAIT A0 at VSS, NRDY/NWAIT pin delivers NREADY
RxD3 RxD2 RxD1 RxD0	3 4 5 6	I	Receive PCM interface Data : Serial data is received at these lines at standard TTL or CMOS levels.
A1	7	I (**)	Non Multiplexed Mode: this input interfaces to the system's address bus to select an internal register for a read or write access. Multiplexed Mode: A1 at VDD, NCS signal provided by the system is not inverted by the circuit. A1 at VSS, NCS signal provided by the system is inverted by the circuit.
TSC0 TSC1 TSC2 TSC3	8 10 12 14	OD	Tristate control for the PCM interface. These lines are low when the corresponding TxD outputs are valid.
TxD0 TxD1 TxD2 TxD3	9 11 13 15	O	Transmit PCM interface Data : Serial data is sent by these lines at standard TTL or CMOS levels. These pins can be tristated.
PFS	16	I	PCM interface frame synchronization pulse.
PDC	17	I	PCM interface data clock, single or double rate.
A2	18	I (**)	Non Multiplexed Mode: this input interfaces to the system's address bus to select an intenal register for a read or write access. Multiplexed Mode: A2 at VDD, AS/ALE signal providedby the system is not inverted by the circuit A2 at VSS, AS/ALE signal provided by the system is inverted by the circuit
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	19 20 21 22 23 24 25 26	I/O	Address Data Bus. If the multiplexed address/data µP interface bus mode is selected these pins transfer data and commands between the µP and the STLC5460. If a demultiplexed mode is used, these bits interface with the system data bus.
VSS1	27	I	Ground : 0V
DS/NRD	28	I	Motorola like mode: Data Strobe Intel Like Mode: Not Read The signal indicates a read operation, active low
RW/NWR	29	I	Motorola like mode: Read/Write Intel Like Mode: Not Write The signal indicates a Write operation, active low.
NCS	30	I	Not Chip select. A low on this line selects the STLC5460 for a read/write operation.

(*): (I) Input
(O) Output
(IO) In/Output
(OD) Open Drain

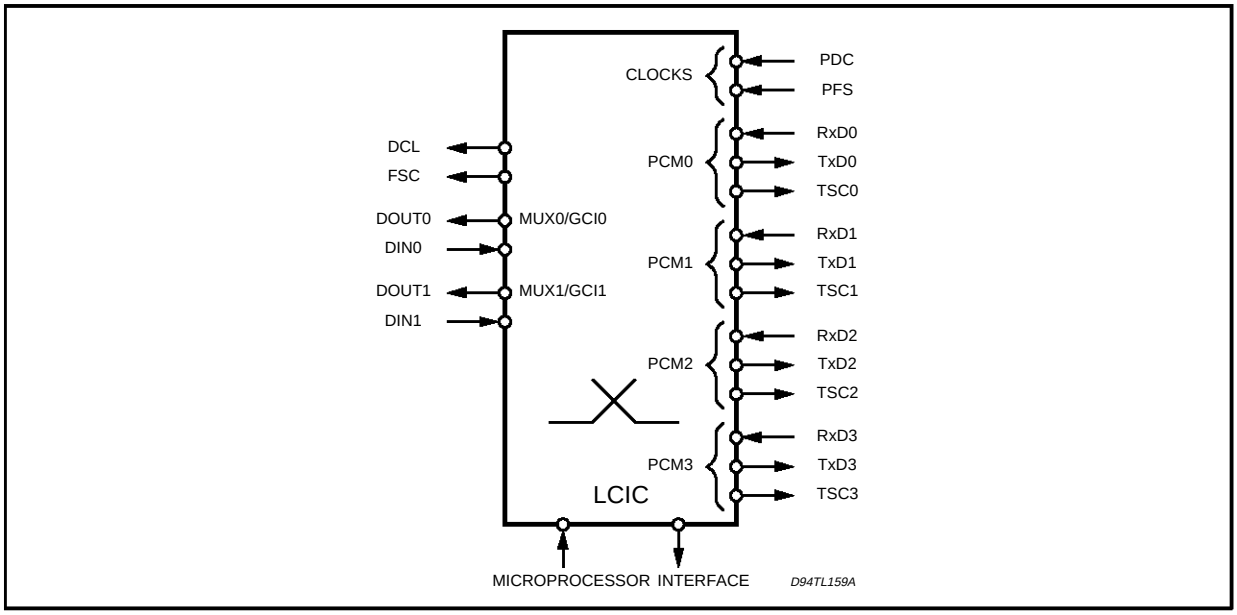
(**): With Pull up resistance.

PIN DEFINITIONS AND FUNCTIONS (continued)

Symbol	Pin n PLCC	Type	Function
AS/ALE	31	I	Multiplexed A/D mode: used to latch the address from ADn Non Multiplexed A/D Mode: This pin at VSS indicates Intel like interfaces This pin at VDD indicates Motorola like interfaces.
INT	32	OD	Interrupt line, active low.
DCL	33	0	Data clock output.
FSC	34	O	Frame synchronization output.
VDD2	35	I	Power supply : 5V
VSS2	36	I	Ground.
DIN1	37	I	GCI Data input 1
DIN0	38	I	GCI Data input 0
A3	39	I (**)	Non Multiplexed Mode: this input interfaces to the system's address bus to select an internal register for a read or write access. Multiplexed Mode: A3 at VDD, DS/NRD signal provided by the system is not inverted by the circuit A3 at VSS, DS/NRD signal provided by the system isinverted by the circuit
DOUT0	40	O	GCI Data Output 0
DOUT1	41	O	GCI Data Output 1
PO	42	I (**)	P0 at VSS: variable access mode P0 at VDD: fixed access mode
NRDY/N WAIT	43	OD	If P0 at VSS: Intel like mode: this pin delivers NRDY Motorola mode: this pin delivers NWAIT
RES	44	I	Reset. A logical high on this input forces the STLC5460 into the reset state

(*): (I) Input
(O) Output
(IO) In/Output
(OD) Open Drain
(**): With Pull up resistance.

Figure 1: GCI and PCM Interfaces.



LINE CARD APPLICATIONS

The LCIC is designed to fit both digital and analogue line card architectures.

It supports up to 16 ISDN subscribers or 16 voice subscribers. The level 1 devices are connected to ST5451 circuits to perform the D channel handling.

Analogue Line Card

In analogue line cards LCIC controls signalling, voice and data path of 64 kb/s channels.

When used in combination with L3040/L3000N, it allows to implement an optimised line card architecture:

the LCIC controls the configuration of L3040 and exchange signalling with the L3040.

Digital Line Card

In digital line cards LCIC controls the configuration of Level 1 circuits (U or S Interface) by means of MON channel configuration and performs activation/deactivation by means of Command/Indicate protocol. LCIC switches the B channels and can switch the D channels if the processing is centralised.

FUNCTIONAL DESCRIPTION

PCM INTERFACE

The PCM Interface Registers configure the data transmitted or received at the PCM port, for one PCM, the maximum data rate can change depending on the Mode selected:

PCM Mode 0: max rate 2048 kb/s with four PCM ports active

PCM Mode 1: max rate 4096 kb/s with two PCM ports active

PCM Mode 2: max rate 8192 kb/s with one PCM ports active.

The "actual data" rate may be varied in a wide range without programming.

An automate computes the number of clock per frame. Hence, the data rate can be stepped in 8, 16 or 32 kb/s in increments in PCM mode 0, 1, 2 respectively.

The clock frequency of PDC is equal to once or twice the data rate, See fig 1 and 2. When operating at single rate (2048 kb/s) and not at double clock frequency (4096 kHz), an onchip clock frequency doubler provides a 4098 kHz clock for the GCI interface (DCL).

The rising edge of PFS signal is used to determine the first bit of the first time slot of the frame. The length of PFS pulse is one bit-time at least and the length between two pulses can be also one bit time.

After reset, the LCIC reaches synchronism having received two consecutive correct PFS pulses. Synchronisation is considered lost by the device if the PFS signal is not repeated with the correct repetition rate which has been stored by the circuit at the beginning of synchronisation research.

The LSYNC bit in the Interrupt Register indicates if the component is synchronised or not: a logical 0 indicates the synchronous state, a logical "1" shows that the synchronism has been lost.

The relation between the framing signal PFS and the bit stream is controlled by the contents of IPOF, OPOF and CPOF registers. These registers denote the number of bit times the PCM frame is shifted. Each PCM multiplex can be programmed with different shifts .

Without programming the bit shift function of the PCM interface, the rising edge of the PFS signal marks the first bit of input PCM frame and the first bit of output PCM frame. See Fig 3

GCI Interface

The Monitor and the Command/Indicate channels may be validated or not, in this second case the B3 and B4 channels become standard channels at 64 kb/s.

When validated Command/Indicate channel may be configured with four bits for digital cards or six bits for analogue cards.

The clocks (Bit clock and frame clock) are delivered by the device with double rate clocking or simple rate clocking.

FSC and DCL are output signals derived from PFS and PDC which are input signals.

GCI			PCM			
DCL clock kHz		Data kb/s	PDC Clock (kHz)		Data rate kb/s	Mode
Simple (*)	Double		Simple	Double		
2.048	4.096	2.048	2.048		2.048	Mode 0
2.048	4.096	2.048		4.096	2.048	Mode 0
2.048	4.096	2.048	4.096		4.096	Mode 1
2.048	4.096	2.048		8.192	4.096	Mode 1
2.048	4.096	2.048	8.192		8.192	Mode 2
2.048	4.096	2.048		16.384	8.192	Mode 2

(*) as GCI format but with simple clock.

Figure 1: PCM Interface. Alignment in double clock mode.

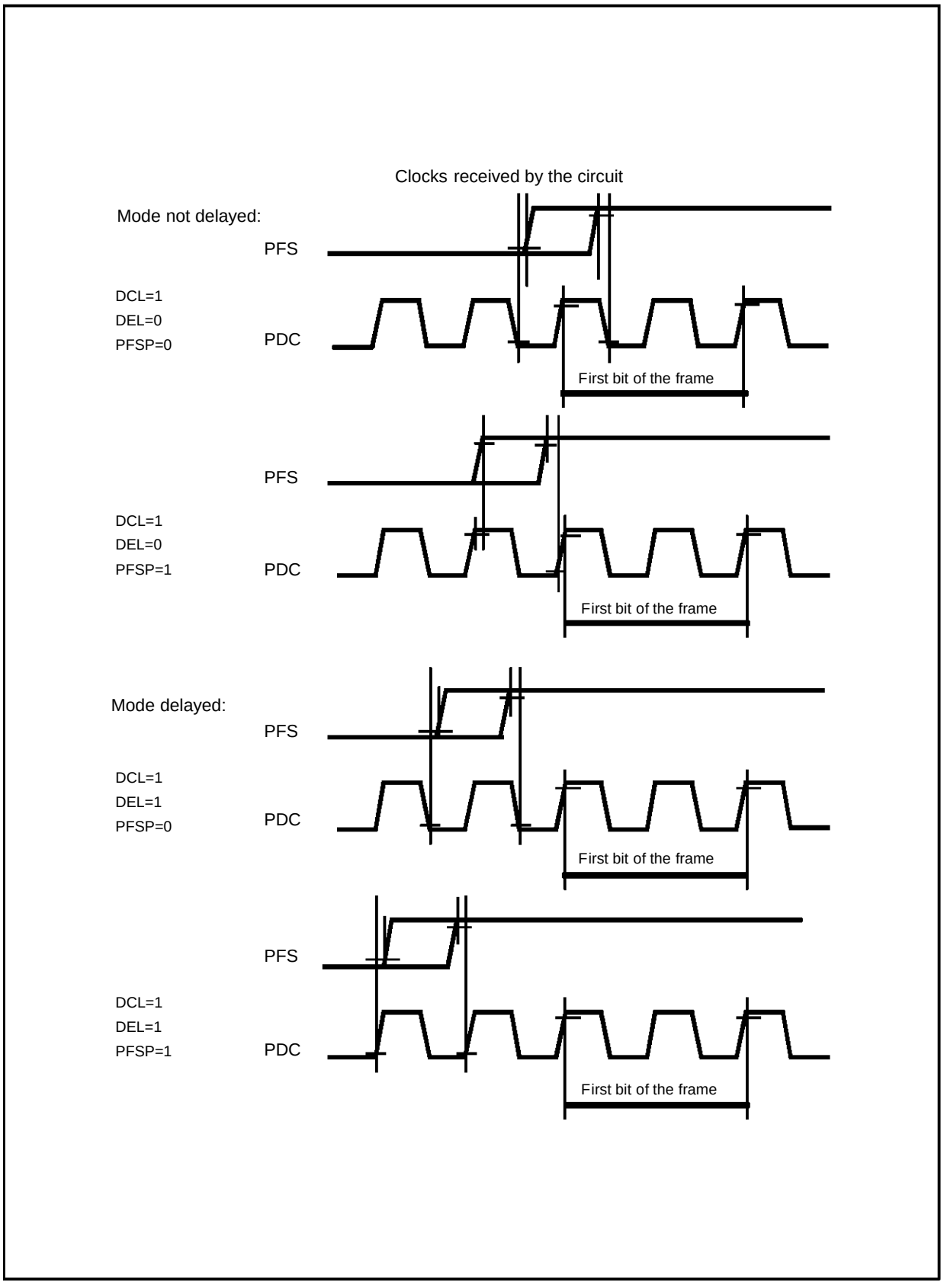


Figure 2: PCM Interface. Alignment in simple clock mode.

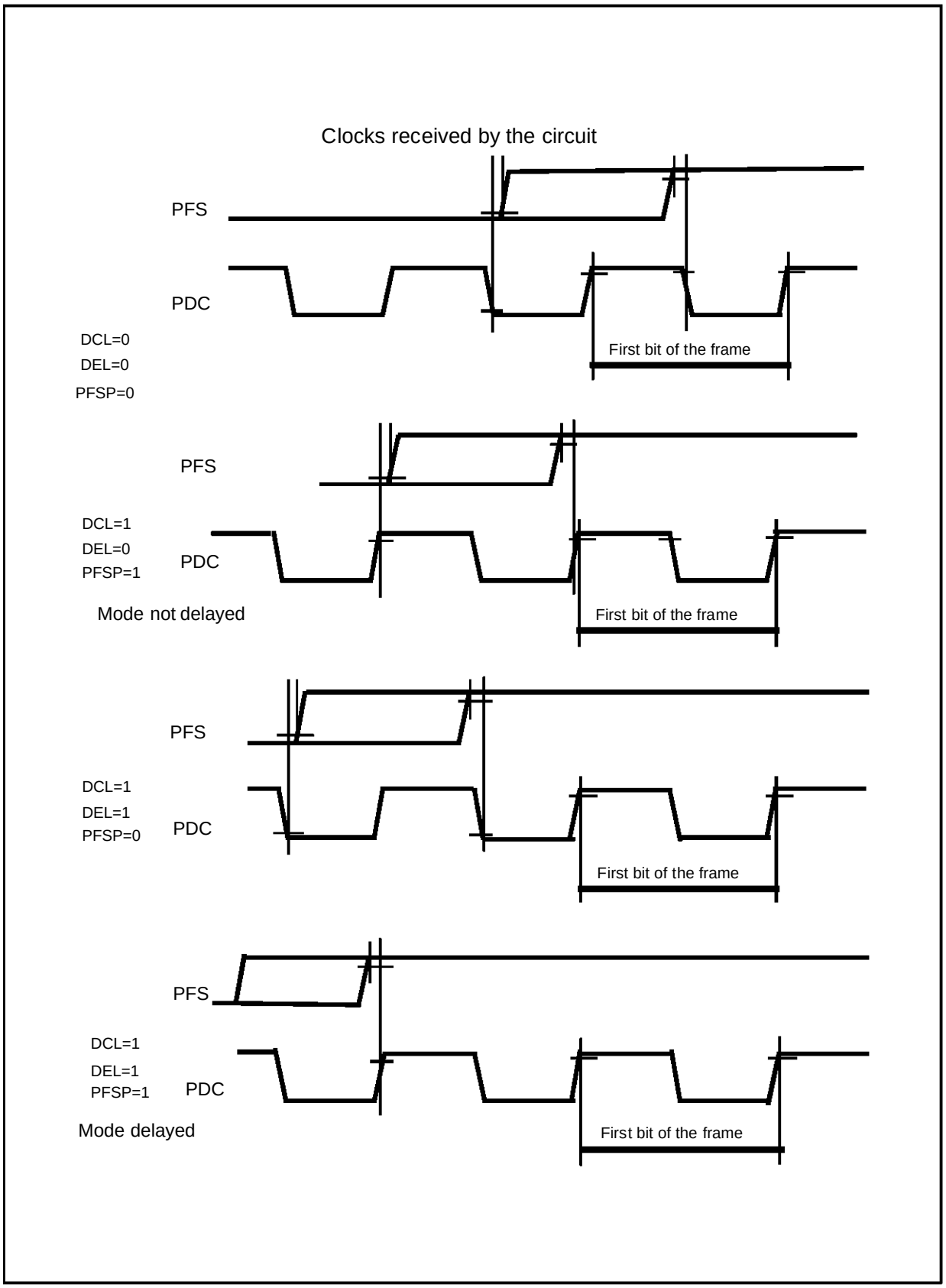
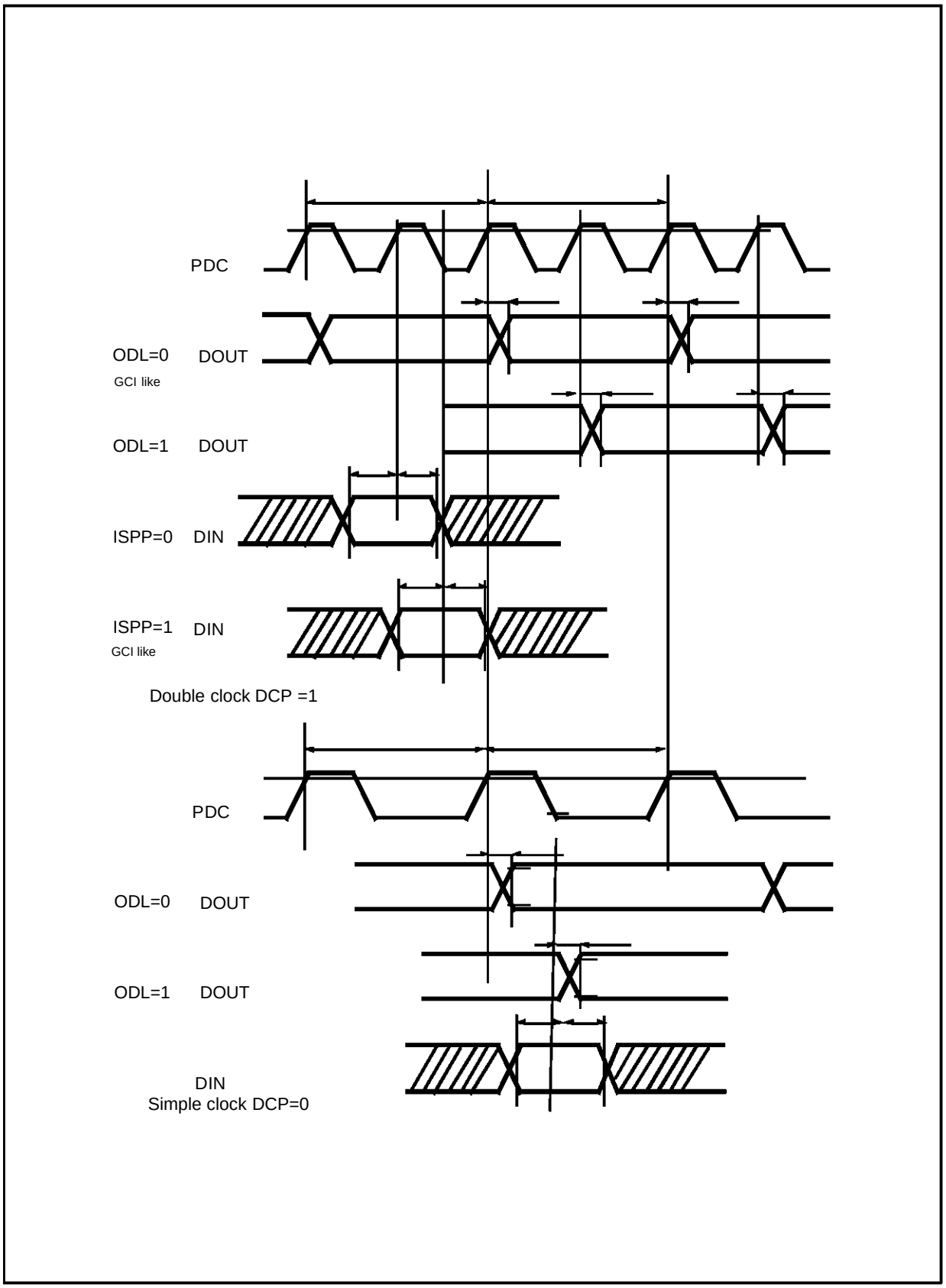


Figure 3: PCM Interface. Clock and Data in/Data out.



MEMORY STRUCTURE AND SWITCHING

The LCIC contains three memories: Auxiliary Memory (AM), Data Memory (DM) and Control Memory (CM).

The Auxiliary Memory consists of one block divided in four parts of 16 words.

This Auxiliary Memory is used for validated data from Monitor and Command/Indicate Rx channels and to transmit data to Monitor and Command/Indicate Tx channels.

The Data Memory buffers the data input from the PCM and the GCI interface. It has a capacity of 128 + 64 time slots to buffer 4 PCM frame of 32 time slots and two GCI interfaces. It is written periodically once every 125 microseconds controlled by the input counters associated to PCM interface and to GCI interface. To perform the switching the loopback function, this memory is read, random, in accordance with the control memory

The Control Memory has a capacity of 128 + 64 words of 14 bits: 8 of data and 6 of code. The 14 bits are written random, via microprocessor interface and read cyclically under the control of the output counters associated to PCM interface and GCI interface.

For control memory access and different functions, three registers are provided:

destination register:

it contains the address of a specific location of the control memory;

source register :

it contains the data (to be written or read) of the control memory corrisponding to the address indicated by the destination register;

command register:

it contains the code (6 bits to be written or read) of the control memory.

The content of command register defines the different capabilities: switching at 64 kb/s, 32 kb/s, 16 kb/s, loopback and also extraction/insertion from the microprocessor interface.

A memory access using the actual command register and source register is performed upon every destination register write access. The processing of the memory access takes at most 488ns.

MICROPROCESSOR INTERFACE

After Reset, the Microprocessor interface is in non-multiplexed mode (Address bus and Data bus must be non-multiplexed):

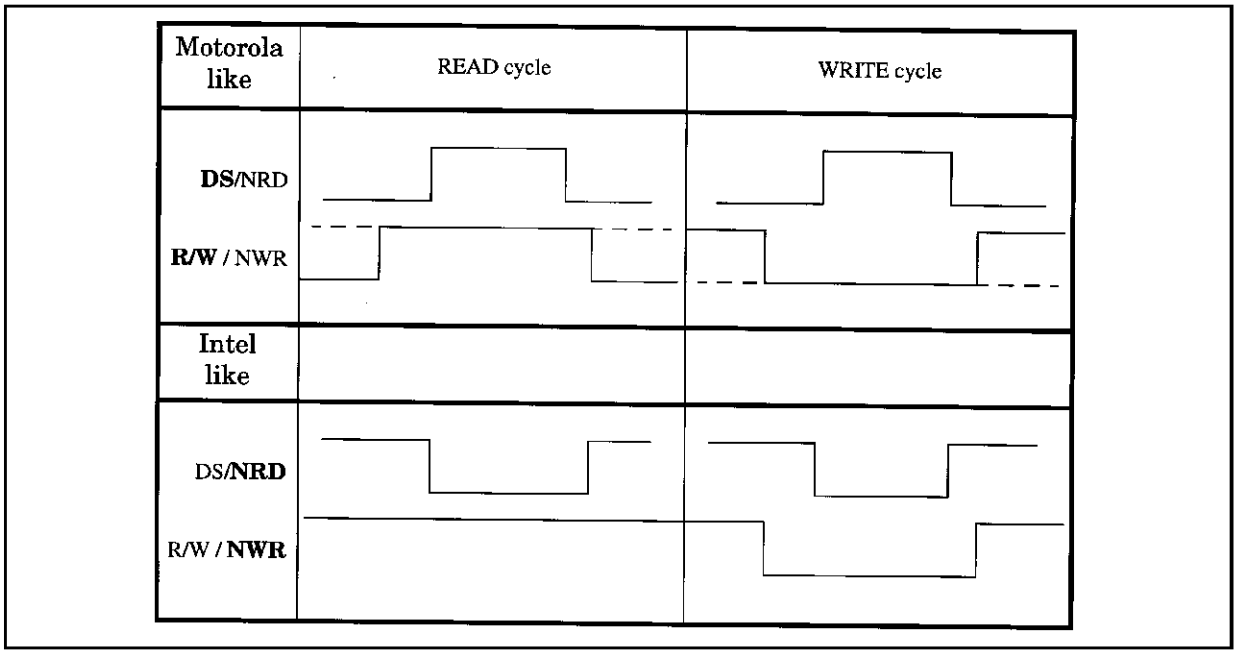
if ALE pin is hardwired at VSS, the Microprocessor interface is Motorola like, Address/Data are non-multiplexed.

if ALE pin is hardwired at VDD the Microprocessor interface is Intel like, Address/Data are non-multiplexed.

After Reset, as soon as two successive edges are detected on ALE pin (Rising and falling edges) by the circuit the Microprocessor interface switches in multiplexed mode (Address bus and Data bus must be multiplexed). The circuit is set automatically in Motorola like or in Intel like mode.

For the circuit Address bus and Data bus multiplexed or not multiplexed, the difference between Motorola like and Intel like mode is showed in fig. 4.

Figure 4.



The microprocessor interface type is set via P0 pin as shown hereafter :

P1 is an outputand it is not used if P0 = 1.

The device selects automatically either Motorola interface or Intel Interface.

P0	P1	Automatical selection
1	Z	Intel MUX mode Motorola MUX mode Intel DEMUX mode Motorola DEMUX mode
0	If A0 = 1	P1 pin delivers WAIT automatically
	If A0 = 0	P1 pin delivers READY automatically

Moreover, for a multiplexed mode µP interface, A1 to A3 pins mean :

A1 = 1: CS signal provided by the system is not inverted by the device

A1 = 0: CS signal provided by the system is inverted by the device

A2 = 1: AS signal provided by the system is not inverted by the device

A2 = 0: AS signal provided by the system is inverted by the device

A3 = 1: DS signal provided by the system is not inverted by the device

A3 = 0: DS signal provided by the system is inverted by the device.

C/I AND MON CHANNELS, EXTRA CHANNELS

The Command/indicate and Monitor channels can be validated or not:

if validated, the C/I and MON protocol controllers operate and it is not possible to use this channels for switching, if not validated the protocols are inhibited and the channels can be used as extrachannels for switching.

Command/Indicate Protocol

Sixteen C/I channels are implemented, one bit of the configuration register MCONF1, indicates the number of bits of the primitive (four or six bits) for all the channels.

To transmit a primitive into one of the 16 channels, the mp loads the primitive (4 or 6 bits) into source register and the number of the C/I channel into destination register with W/R bit of command register at ”0”.

The two more significant bits of the source register indicates if the primitive, bit0/5 of the same register, has not been transmitted yet, transmitted once, twice or more .

When a new primitive has been received twice identical, on one of the 16 C/I channels, an interrupt is generated, the number of the C/I channel (4 bits) is written in the Receive C/I status register , and the primitive received is in the Auxiliary Memory, all accessible to the µp

Moreover, the microprocessor can read directly the 16 primitives that have been received and stored into the Receive C/I Memory. To read this memory the µp load in the Source Register the number of Receive C/I channel it wants, and in the destination register reads the primitive (4 or 6 bits) with a seventh bit which indicates whether the primitive has been received once or twice identical. vedi figura read aux mem Receive C/I channels.

Monitor Channel Protocol

Sixteen Monitor channels are implemented. To transmit a message the µp load into destination register with W/R bit of Command Register at 1 the number of MON channels, and into source register the message; this byte is transmitted if BYTE Bit of Command Register is at 1.

This procedure is repeated for each byte of the message if it is longer than one byte.

When a new byte has been received twice identical from one of the sixteen Monitor channels

an interrupt is generated, the number of MON channel (4 bits) is written in Receive Monitor Status Register and the last byte received is written in Receive data Monitor Channel Memory. The remote transmitter will transmit the next byte after reading of this register by the local microprocessor.

INSERTION - EXTRACTION

This function allows to insert data into GCI and PCM channels and to extract data from GCI and PCM interface. These data are provided either by the microprocessor or by an internal Pseudo Random Sequence Generator.

Insertion

Two programmable registers (Insert A and B) contain the data to insert into two output time slots continuously. To perform an insertion, four registers are programmed by the microprocessor:

- in the Insert A and/or B Registers it writes the data to insert.
- in the Source registers it writes the A and/or B register address
- in the Destination Register it writes the output interface, PCM or GCI, and the Time Slot selected.

- in the Command Register it writes the indication if insert into 64 kb/s, 32 kb/s or 16 kb/s channel.

When the data has been inserted, status bit (INS) of status register is put at logical 1 and an interrupt is generated.

Extraction

Two programmable registers (Extract A and B) contain the data extracted from two input time slots. To perform an extraction, three registers are processed by the microprocessor :

- Extract A and/or B Registers to read the data extracted.

- The Source register to indicate the input interface, PCM or GCI, and the Time Slot selected.
  When the data is loaded in Extract A or Extract B Register, the bit EXT of STATUS register is put at logical 1,and an interrupt is generated.

LIST OF REGISTER

Name	MUX Mode			Read Only	DEMUX Mode	
	AD5 to AD1	(H)	RBS		A3 to A0	RBS
IIR	00000	(00)	X		0000	X
COMP	00001	(01)	X		0001	0
MCONF1	00010	(02)	X		0010	0
MCONF2	00011	(03)	X		0011	0
PCONF	00100	(04)	X		0100	0
CPOF	00101	(05)	X		0101	0
IPOF	00110	(06)	X		0110	0
OPOF	00111	(07)	X		0111	0
IPSH1	01000	(08)	X		1000	0
IPSH2	01001	(09)	X		1001	0
OPSH1	01010	(0A)	X		1010	0
OPSH2	01011	(0B)	X		1011	0
IPASS	01100	(0C)	X		1100	0
OPASS	01101	(0D)	X		1101	0
IMASS	01110	(0E)	X		1110	0
OMASS	01111	(0F)	X		1111	0
STATUS	10001	(11)	X	R	0001	1
ECR	10010	(12)	X		0010	1
CMR	10011	(13)	X		0011	1
SRC	10100	(14)	X		0100	1
DST	10101	(15)	X		0101	1
INSA	10110	(16)	X		0110	1
INSB	10111	(17)	X		0111	1
EXTA	11000	(18)	X	R	1000	1
EXTB	11001	(19)	X	R	1001	1
INT	11010	(1A)	X	R	1010	1
MASK	11011	(1B)	X		1011	1
RMOS	11100	(1C)	X	R	1100	1
TMOS	11101	(1D)	X	R	1101	1
RCIS	11110	(1E)	X	R	1110	1
TEST	11111	(1F)	X		1111	1

NB in Mux Mode AD7, AD6, AD0 and RDS bits are ignored

CONFIGURATION REGISTER DESCRIPTION

Initialisation and Identification Register (IIR)

7							0
RBS	RST	T1	T0	V3	V2	V1	V0

After Reset 3F (H)

T1/T0 Test functions

T1	T0	Description
0	0	Normal State
0	1	Command Memory or Auxiliary Auto Reset. If CM = 1 (Bit of Command Register): the six lower bits of command Register and the eight bits of Source Register are stored into each address of command Memory. If CM = 0 (Bit of Command Register) : the eight bits of Source Register are stored into each address of Monitor Auxililary Memory and the six lower bits of Source Register are stored intoCommand/Indicate Auxilliary Memory. The 16 C/I and Monitor channels are ready to transmit and to receive data.After AutoReset, BUSY and T0 goes to "0".
1	1	Auto Test. This function is reserved for manufacturer. - The Pseudo Random Sequence generator is connected instead of Insert A Register and Pseudo Random Sequence Analyzer is connected instead of Extract A Register. - The Command Memory is loaded thanks to a special algorithm in order to switch the sequence provided by the generator into TSO of PCMO, then the contents of TSO of PCMO into TS1 of PCMO, then the contents of TS1 of PCMO into TS2 of PCMO and so on. Finally, the contents of TS31 of MUX1 are taken into account by the Pseudo Random Sequence Analyzer.After loading Command Memory, 193 switching are set up in real time.The analyzer receives the Pseudo Random Sequence from the generator after switching. If LP = 1, the loopback is internal. If LP = 0, an external loopback must be performed. So, Command Memory and Data Memory can be checked in the same time.
1	1	Reserved. Initialise CM so that the content of each input Time Slot t of input multiplex m is switched to output Time Slot t of output multiplex m

RBS Register Bank Selection.
RBS = 0. The 16 first main registers are selected (0 to 15).

RST Reset Soft.
the programmable registers are reset.

V3/V0 these bits are fixed at 0

COMPARISON REGISTER (COMP)

7							0
NEWE	TIM	CP6	CP5	CP4	CP3	CP2	CP1

After Reset 00 (H)

NEWE New EXTRACT.
When NEWE = 1, EXT interrupt is generated only if a new word is loaded into EXTRACT Registers (A or B).

TIM Timer, associated to INS of INT Register and to TIMO/1 of CPOF register.
TIM = 1 TIM0/1 bits of CPOF register are taken into account
TIM = 0 an interrupt is generated each 125 µs.

CP 6/1 Comparison 6 to 1.
Bit stream of one PCM and bit stream of another PCM are compared at each bit time, if there is difference, PDIF interrupt is generated.

	Comparison between
CP1 = 1	PCM0 and PCM1
CP2 = 1	PCM1 and PCM2
CP3 = 1	PCM2 and PCM3
CP4 = 1	PCM0 and PCM2
CP5 = 1	PCM1 and PCM3
CP6 = 1	PCM0 and PCM3

MULTIPLEX CONFIGURATION 1 REGISTER (MCONF1)

7							0
CIM	MOM	CI4MI	CI4M0	-	-	GCIM1	GCIM0

After Reset 3F (H)

CIM Command/Indicate Mode.
CIM = 1: the controller ignores the new received primitive if the previous has not been read by the microprocessor.

CIM = 0: the controller overwrites the previous primitive without condition when it receives a new primitive.

MOM Monitor channel Mode
MOM = 1: if bytes are not received twice identical the message is aborted.
MOM = 0: if bytes are not received twice identical the MOM controller doesn't acknowledge the received byte (GCI standard).

CI4M1 Command Indicate 4 bits for Multiplex 1.
CI4M1 = 0: command Indicate primitive has six bits.
CI4M1 = 1: command Indicate primitive has four bits.

CI4M0 Command Indicate 4 bits for Multiplex 0.
CI4M0 = 0: command Indicate primitive has six bits.
CI4M0 = 1: command indicate primitive has four bits.

GCIM1 GCI Multiplex 1.
GCIM1 = 1: the multiplex M1 is GCI, it includes eight GCI channels.
GCIM1 = 0: the multiplex M1 includes 32 Time Slots. (PCM like channel)

GCIM0 GCI Multiplex 0.
GCIM0 = 1: the Multiplex M0 is GCI, it includes eight GCI channels.
GCIM0 = 0: the multiplex M0 includes 32 Time Slots. (PCM like channel)

MULTIPLEX CONFIGURATION 2 REGISTER (MCONF2)

7							0
-	-	M1D	M0D	ISPM	TIMD	MOD	DCKM

After Reset FF (H)

M1D Multiplex 1 Disable.
M1D = 1. Multiplex 1 output is at high impedance continuously, multiplex 1 input is forced to "1", if it is GCI.

M0D — Multiplex 0 Disable.
M0D = 1. Multiplex 0 output is at high impedance continuously, multiplex 0 input is forced to "1", if it is GCI.

TIMD — Timer Monitor Channel Disabled.
TIMD = 1. The timer 1ms is disabled for each Transmit Monitor Channel.

ISPM — Input Sampling Multiplex.
ISPM = 0. The input bit is sampled at half bit time.
ISPM = 1. The input bit is sampled at 3/4 bit time.

MOD — Multiplex Open Drain.
MOD = 1. The two multiplex outputs are open drain.
MOD = 0. The two multiplex outputs are at low impedance

DCKM — Double clock for Multiplex.
DCKM = 1. DCL is twice data rate (Ex : if Data Rate = 2048 kb/s,DCL = 4096 kHz).
DCKM = 0. DCL is simple clock.

PCM CONFIGURATION REGISTER (PCONF)

7							0
0	TSNB	DEL	PFSP	ODL	ISPP	POD	SCKP

After Reset 00 (H)

TSNB — Time Slot numbering.
TSNB defines the order of TS on the PCM when the data rate is 4 Mb/s or 8 Mb/s related to the order of TS on the PCM at 2 Mb/s (see table hereafter).

DEL — Delayed Mode for each PCM.
DEL = 1. A delay of one clock pulse is applied to the first bit of the frame of each PCM.
DEL = 0. PFS indicates the first bit of the frame for each PCM (if OFFSET and shift are zero).

PFSP — PCM Frame Synchronisation Sampling.
PFSP = 0. PFS signal is sampled on the fall edge of PDC signal.
PFSP = 1. PFS signal is sampled on the rise edge of PDC signal.

ODL — Output Delay.
ODL = 0. The bits are shifted out with zero delay.
ODL = 1. The bits are shifted out with a delay of one half bit time.

ISPP — Input Sampling PCM.
ISPP = 0. The input bit is sampled at half bit time.
ISPP = 1. The input bit is sampled at 3/4 bit time.

POD — PCM Open Drain.
POD = 1. The PCM outputs are open drain
POD = 0. The PCM outputs are at low impedance.

SCKP — Simple clock for PCM.
SCKP = 0. PDC signal is twice data rate. (Ex : if data rate = 2048 kb/s, PDC = 4096 kHz).
SCKP = 1. PDC is simple clock

TS and PCMn at 4 Mb/s with n = 0 or 2		TS0	TS1	TS2	TS3	TS30	TS31	TS32	TS62	TS63
TSNB = 1	TS at 2Mb/s	TS0	TS0	TS1	TS1	TS15	TS15	TS16	TS31	TS31
	PCM at 2Mb/s	PCMn	PCMn+1	PCMn	PCMn+1	PCMn	PCMn+1	PCMn	PCMn	PCMn+1
TSNB = 0	TS at 2Mb/s	TS0	TS1	TS2	TS3	TS30	TS31	TS0	TS30	TS31
	PCM at 2Mb/s	PCMn						PCMn+1		

TS and PCM0 at 8 Mb/s		TS0	TS1	TS2	TS3	TS4	TS124	TS32	TS62	TS63
TSNB = 1	TS at 2Mb/s	TS0	TS0	TS0	TS0	TS1	TS31	TS31	TS31	TS31
	PCM at 2Mb/s	PCM0	PCM1	PCM2	PCM3	PCM0	PCM0	PCM1	PCM2	PCM3
TS and PCM at 8Mb/s		TS0 to TS31			TS32 to TS63		TS64 to TS95		TS96 to TS127	
TSNB = 0	TS at 2Mb/s	TS0 to TS31			TS0 to TS31		TS0 to TS31		TS0 to TS31	
	PCM at 2Mb/s	PCM0			PCM1		PCM2		PCM3	

COMPLEMENTARY PCM OFFSET REGISTER (CPOF)

7							0
PMD1	PMD0	TIM1	TIM0	OOF1	IOF0	IOF1	IOF0

After Reset 00 (H)

PMD1/0 PCM Mode

PMD1	PMD0	The PCM are at
0	0	2048 kbit/s
0	1	4096 kbit/s
1	0	8192 kbit/s
1	1	Not used.

TIM 1/0 these bits are taken into account only if bit TIM of COMP register is at 1; in this case an interrupt is generated periodically and TIM 1/0 defines the period

TIM1	TIM0	Period
0	0	1ms
0	1	8ms
1	0	64ms
1	1	250ms

OOF1/0 Output Offset 1/0.
These two bits are associated with OOF2/9 ofOPOF Register.

IOF1/0 Input Offset 1/0.
These two bits are associated with IOF2/9 of IPOF Register.

INPUT PCM OFFSET REGISTER (IPOF)

7							0
IOF9	IOF8	IOF7	IOF6	IOF5	IOF4	IOF3	IOF2

After Reset 00 (H)

IOF9/2 Input PCM Offset 9 to 2.
Associated with IOF1/0, these ten bits indicate the delay between PFS signal and the first bit of the frame, for each input

OUTPUT PCM OFFSET REGISTER (OPOF)

7							0
OOF9	OOF8	OOF7	OOF6	IOF5	OOF4	OOF3	OOF2

After Reset 00 (H)

OOF9/2 Output PCM Offset 9 to 2.
Associated with OOF1/0 of complementary offset register, these ten bits indicate the delay between bit 0 of the frame out going versus bit 0 of the frame incoming.

INPUT PCM SHIFT 1 (IPSH1)

7							0
0	P1SH2	P1SH1	P1SH0	0	P0SH2	P0SH1	P0SH0

After Reset 00 (H)

P1SH2/0 PCM1 Shift 2 to 0.
This number (0 to 7) is added to Input PCM offset to obtain the total shift of the frame of PCM1.

P0SH2/0 PCM0 shift 2 to 0.
This number (0 to 7) is added to Input PCM offset to obtain the total shift of the frame of PCM0.

INPUT PCM SHIFT 2 (IPSH2)

7							0
0	P3SH2	P3SH1	P3SH0	0	P2SH2	P2SH1	P2SH0

After Reset 00 (H)

P3SH2/0 PCM3 Shift 2 to 0.
This number (0 to 7) is added to Input PCM offset to obtain the total shift of the frame of PCM3.

P2SH2/0 PCM2 Shift 2 to 0.
This number (0 to 7) is added to Input PCM offset to obtain the total shift of the frame of PCM2.

OUTPUT PCM SHIFT 1 (OPSH1)

7							0
P1E	P1SH2	P1SH1	P1SH0	P0E	P0SH2	P0SH1	P0SH0

After Reset 00 (H)

P1E Output PCM1 Enable.
P1E = 0. PCM1 output is at high impedance.
P1E = 1. PCM1 output is enable.

P1SH2/0 PCM1 shift 2/0.
This number (0 to 7) is added to output PCM offset to obtain the total shift of the frame of PCM1.

P0E Output PCM2 Enable.
P0E = 0. PCM0 output is at high impedance.
P0E = 1. PCM0 output is enabled.

P0SH2/0 PCM0 Shift 2/0.
This number (0 to 7) is added to output PCM offset to obtain the total shiftof the frame of PCM0.

OUTPUT PCM SHIFT 2 (OPSH2)

7							0
P3E	P3SH2	P3SH1	P3SH0	P2E	P2SH2	P2SH1	P2SH0

After Reset 00 (H)

P3E Output PCM3 Enable.
P3E = 0. PMC3 output is at high impedance.
P3E = 1. PCM3 output is enabled.

P3SH2/0 PCM3 Shift 2/0.
This number (0 to 7) is added to output PCM offset to obtain the total shiftof the frame of PCM3.

P2E Output PCM2 Enable.
P2E = 0. PCM2 output is at high impedance.
P2E = 1. PCM2 output is enabled.

P2SH2/0 PCM2 shift 2/0.
This number (0 to 7) is added to output PCM offset to obtain the total shift of the frame of PCM2

INPUT PCM ASSIGNMENT REGISTER (IPASS)

7							0
IP31	IP30	IP21	1P20	1P11	1P10	1P01	1P00

After Reset E4 (H)

IP31/IP30 Incoming PCM3 Assignment.

IP31	IP30	Incoming PCM3 receives data from
0	0	Pin RxD0
0	1	Pin RxD1
1	0	Pin RxD2
1	1	Pin RxD3 (Default value)

IP21/IP20 Incoming PCM2 Assignment.

IP21	IP20	Incoming PCM2 receives data from
0	0	Pin RxD0
0	1	Pin RxD1
1	0	Pin RxD2 (Default value)
1	1	Pin RxD3

IP11/IP10 Incoming PCM1 Assignment.

IP11	IP10	Incoming PCM1 receives data from
0	0	Pin RxD0
0	1	Pin RxD1(Default value)
1	0	Pin RxD2
1	1	Pin RxD3

IP01/IP00 Incoming PCM0 Assignment.

IP01	IP00	Incoming PCM2 receives data from
0	0	Pin RxD0(Default value)
0	1	Pin RxD1
1	0	Pin RxD2
1	1	Pin RxD3

OUTPUT PIN ASSIGNMENT REGISTER (OPASS)

7							0
OP31	OP30	OP21	OP20	OP11	OP10	OP01	OP00

After Reset E4 (H)

OP31/OP30 Output Pin 3 Assignment.

OP31	OP30	Pin TxD3 receives data from
0	0	Outgoing PCM0
0	1	Outgoing PCM1
1	0	Outgoing PCM2
1	1	Outgoing PCM3 (Default Value)

OP21/OP20 Output Pin 2 Assignment.

OP31	OP30	Pin TxD2 receives data from
0	0	Outgoing PCM0
0	1	Outgoing PCM1
1	0	Outgoing PCM2 (Default Value)
1	1	Outgoing PCM3

OP11/OP10 Output Pin 1 Assignment.

OP11	OP10	Pin TxD1 receives data from
0	0	Outgoing PCM0
0	1	Outgoing PCM1 (Default Value)
1	0	Outgoing PCM2
1	1	Outgoing PCM3

OP01/OP00 Output Pin 0 Assignment.

OP01	OP00	Pin TxD0 receives data from
0	0	Outgoing PCM0 (Default Value)
0	1	Outgoing PCM1
1	0	Outgoing PCM2
1	1	Outgoing PCM3

INPUT MULTIPLEX ASSIGNMENT REGISTER (IMASS)

7							0
-	-	-	-	0	IM1	0	IM0

After Reset 04 (H)

IM1 Incoming Multiplex 1 Assignment.

IM1	Incoming Multiplex 1 receives data from
0	Pin DIN 0
1	Pin DIN 1 (Default Value)

IM0 Incoming Multiplex 0 Assignment.

IM0	Incoming Multiplex 0 receives data from
0 1	Pin DIN 0 (Default Value) Pin DIN 1

OUTPUT MULTIPLEX ASSIGNMENT REGISTER (OMASS)

7							0
-	-	-	-	0	DO1	0	DO0

After Reset 04 (H)

DO1 Output 1 Pin Assignment.

DO1	DOUT 1 pin receives data from
0 1	Outgoing Multiplex 0 Outgoing Multiplex 1 (Default value)

DO0 Output 0 Pin Assignment.

DO1	DOUT 0 pin receives data from
0 1	Outgoing Multiplex 0 (Default value) Outgoing Multiplex 1

WORKING REGISTER DESCRIPTION

Command Register (CMR)

7							0
R/W	CM	CR5	CR4	CR3	CR2	CR1	CR0

After Reset 00 (H)

R/W Read/Write
R/W = 0. Write memory.
Address bits are provided by the Destination Register (DST)
Data bits are provided by the Source Register (SRC)

R/W = 1. Read Memory.
Address bits are provided by the Destination Register (DST)
Data bits will be in Source Register (SRC) when BUSY (Status Register) will go to ”0”.

CM Command memory.
CM = 1 Access to Command Memory
CM = 0 Access to Auxiliary Memory.

CR 5/0 The meaning of these bits depends on the value of CM and R/W. The description is given thereafter.

	CM = 1 Command Memory	CM = 0 Auxiliary Memory
Command Register Bit 5 to 0	Subchannel configuration	Command if Write Memory Status if Read Memory
Source Register	1 of 192 Input Time Slots or 1 of 2 Insertion Registers	Byte if MON channel or Primitive if C/I channel.
Destination Register	1 of 192 Output Time Slots or 1 of 2 Extraction Registers	1 of 16 MON channels or 1 of 16 C/I channels

Following you will find a detailed explanation case by case of the meaning of all the bits of this register.

FIRST CASE CM = 1: ACCESS TO COMMAND MEMORY

	CM	CR5	CR4	CR3	CR2	CR1	CR0
R/W	1	CH1	CH0	SS1	SS0	DS1	DS0

After Reset 00 (H)

R/W Read/Write

R/W = 0 (Write). The eight bits of Source Register and the six lower bits of this Command Register are loaded into the Command Memory (14 bits). The Address bits are given by the Destination Register (8 bits). Write cycle starts when Destination Register is loaded by the microprocessor.

R/W = 1 (Read).
The 14 bits of Command memory addressed by the Destination Register are loaded respectively into Command Register (6 bits) and Source Register (8 bits). Read cycle starts when Destination Register is loaded by the micro-processor.

CH0/1 Channel Data Rate

CH1	CH0	Description
0	0	The output is at high impedance during the time slot selected
0	1	16kb/s subchannel is selected
1	0	32kb/s subchannel is selected
1	1	64kb/s channel is selected

During the time slot selected, the output is at high impedance for the subchannels not selected.

SS 0/1 Source Subchannel selected.

Data Rate	SS1	SS0	Source channel
16kb/s	0	0	Bits 6-7
	0	1	Bits 4-5
	1	0	Bits 2-3
	1	1	Bits 0-1
32kb/s	0	0	Bits 4 to 5
	0	1	Bits 0 to 3

Bit 7 is trasmitted first.

DS 0/1 Destination Subchannel selected.

Data Rate	SS1	SS0	Source channel
16kb/s	0	0	Bits 6-7
	0	1	Bits 4-5
	1	0	Bits 2-3
	1	1	Bits 0-1
32kb/s	0	0	Bits 4 to 5
	0	1	Bits 0 to 3

Bit 7 is trasmitted first.

SECOND CASE CM = 0: ACCESS TO AUXILIARY MEMORY

Microprocessor writes Auxiliary Memory to transmit Primitives for each TX C/I channel and to transmit Bytes of message for each TX MON channel.

Microprocessor reads Auxiliary memory to recover Primitive received by each RX C/I channel and to recover the message received by each RX MON channel.

TX Command Indicate channel - Selected by Destination Register (DST)

	CM	CR5	CR4	CR3	CR2	CR1	CR0
R/W	0	-	-	-	-	PT1	PT0

R/W = 1 Read auxiliary memory

After writing this register with R/W=1 and when BUSY(status register) has gone to 0, the bits of the register have the following meaning:

CR5/CR2 Not used

PT0/1 Primitive trasmitted

PT1	PT0	Status
0	0	Primitive has not been transmitted yet
0	1	Primitive has been transmitted once
1	0	Primitive has been transmitted twice
1	1	Primitive has been transmitted more than twice.

R/W = 0 Write auxiliary memory.

CR0/CR5 not used

RX Command Indicate channel - Selected by Destination Register (DST)

	CM	CR5	CR4	CR3	CR2	CR1	CR0
R/W	0	-	-	-	-	OVR	PR

R/W = 1 Read auxiliary memory

After writing this register with R/W=1 and when BUSY(status register) has gone to 0, the bits of the register have the following meaning:

CR5/CR2 Not used

OVR Overrun
OVR = 1. The previous primitive has not been read by the microprocessor.

PR Primitive Received.
PR = 1. The primitive has been received once
PR = 0. The primitive has been received twice or more.
The primitive is in Source Register.

R/W = 0 Writing auxiliary memory.

CR0/CR5 not used

TX Monitor Channel selected by Destination Register.

R/W	CM	CR5	CR4	CR3	CR2	CR1	CR0
0	0	-	-	-	LAST	BYTE	INIT

IR/W = 0 Writing auxiliary memory.

CR5/CR3 not used

LAST Last Byte.
This bit is associated with BYTE.
If LAST = 1, last byte of the message.
If LAST = 0, current byte

BYTE Byte to transmit.

INIT When this bit is at 1, the MON channel defined in SRC Register is initialised and the Monitor Channel is idle (All "1"s are transmitted)

R/W	CM	CR5	CR4	CR3	CR2	CR1	CR0
1	0	-	T0	ABT	LAST	BYTE	IDLE

R/W = 1 Read auxiliary memory

After writing this register with R/W=1 and when BUSY(status register) has gone to 0, the bits of the register have the following meaning:

TO Time Out = one millisecond.
This bit goes to 1 when the remote receiver has not acknowledged the byte after 1 millisecond.

ABT Abort.
ABT = 1 The remote receiver has aborted the message transmitting.

LAST Last Byte.
This bit is associated with BYTE.
If LAST = 1, last byte of the message.
If LAST = 0, current byte.

BYTE BYTE = 1 Byte transmitting.
BYTE = 0 Byte transmitted and acknowledged by the Remote Receiver, a new byte can be transmitted.

IDLE IDLE = 1 Monitor channel, A bit, E bit are at "1".

RX Monitor channel- Selected by Destination Register

	CM	CR5	CR4	CR3	CR2	CR1	CR0
R/W	0	-	-	-	AB	BYTE	EOM

R/W = 1 Read auxiliary memory

After writing this register with R/W=1 and when BUSY(status register) has gone to 0, the bits of the register have the following meaning:

AB Abort.
AB = 1 The receiver has detected an error during the transmission.

BYTE New byte.
Byte = 1 A new byte is available in the Source Register

EOM End of Message
EOM = 1 : there is no significant byte in the Source Register. The previous byte which had been received was the last.

R/W = 0 Write auxiliary memory.

Writing initiates the RX Monitor Channel.

CR0/CR5 not used

SOURCE REGISTER (SRC)

When the bit CM of command register is at one, this register contains the data to be written in the control memory at the address indicated by the destination Register. It rappresents the address of the data memory, or of one of the insert register, corresponding to the input data to be switched to the output indicated by the destination register.

Following you will find a detailed explanation case by case of the meaning of all the bits of this register.

First case CM = 1 (Bit of Command Register)

Command Memory is selected.

7							0
PCM	SR6	SR5	SR4	SR3	SR2	SR1	SR0

After Reset 00 (H)

PCM = 1 The source is PCM Input.

PCM = 0 The source is not PCM. The Source is either Multiplex Inputs (GCI) or Insert Registers.

PCM = 1

PCM	SR6	SR5	SR4	SR3	SR2	SR1	SR0
1	N1	N0	TS4	TS3	TS2	TS1	TS0

After Reset 00 (H)

If PCM is at 2 Mb/s

N0/1	PCM Number : 0 to 3
TS0/4	Time Slot Number : 0 to 31

If PCM is at 4 Mb/s

N1	PCM at 4 Mb/s : 0 or 1
TS0/4 and N0	Time slot Number : 0 to 63 N0 = TS5

If PCM is at 8 Mb/s

TS0/4 and N0/1	Time Slot Number : 0 to 127. N0 = TS5, N1 = TS6.

PCM = 0 **The Source is Multiplex Input or Insertion Register.**

If N1 = 0 Multiplexes are selected (GCI or not) then

N0 = 0 Multiplex number : 0

N0 = 1 Multiplex number : 1

TS0/4 Time Slot Number : 0 to 31

If N1 = 1 Insertion Registers are selected.

N0 = 0 and TS0/4 = 0. A Insertion Register 40 (H) is the source

N0 = 1 and TS0/4 = 1. B Insertion Register 41(H) is the source .

Second case : CM = 0 (Bit of Command Register)

The auxiliary memory is selected.

If channel is Monitor channel (see Destination Register), the contents of Source Register are data :

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
M8	M7	M6	M5	M4	M3	M2	M1

It is proposed to initialise at FF, before starting normal operation using initialisation register T1 = 0 and T0 = 1.
M8 will be transmitted first.

If channel selected by DestinationRegister is Command/Indicate channels, the mean of bits of Source Register are :

- For TX C/I with R/W = 0 Write auxiliary memory.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
-	-	C6	C5	C4	C3	C2	C1

It is proposed to initialise at FF, before starting normal operation using initialisation register T1 = 0 and T0 = 1.

C1/C6 Primitive to transmit : C6 and C5 bits are taken into account depending on CI4M1 and CI4M0 bits of MCONF Register.C6 (or C4) will be transmitted first.

- For TX C/I with R/W = 1 Read auxiliary memory.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
PT1	PT0	C6	C5	C4	C3	C2	C1

PT 1/0 Status of Transmitting primitive.

PT1	PT0	Status
0	0	Primitive has not been transmitted yet
0	1	Primitive has been transmitted once
1	0	Primitive has been transmitted twice
1	1	Primitive has been transmitted more than twice.

C6 to C1 Primitive being transmitted.

For RX C/I with R/W = 0, write auxiliary memory. This Source Register is not taken into account.

For RX C/I with R/W = 1, read auxiliary memory.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
OVR	PR	C6	C5	C4	C3	C2	C1

OVR Overrun.
When OVR = 1, the previous primitive had not been read by the microprocessor;
the current primitive has been put instead of the previous primitive. The previous primitive has been lost.

PR Primitive Received.
PR = 1, the current primitive has been received identical twice or more.

C6 to C1 Primitive received.

DESTINATION REGISTER (DST)

First case CM = 1 (Bit of Command Register). Command Memory is selected.

7							0
PCM	DT6	DT5	DT4	DT3	DT2	DT1	DT0

After Reset 00 (H)

PCM = 1 The destination is PCM output

PCM = 0 The destination is not PCM. The destination is either Multiplex (GCI or not) or Extract Registers.

PCM = 1

PCM	DT6	DT5	DT4	DT3	DT2	DT1	DT0
1	N1	N0	TS4	TS3	TS2	TS1	TS0

PCM = 1 The destination is PCM output

If PCM are at 2 Mb/s:

N0/1 PCM number: 0 to 3

TS0/4 Time Slot number 0 to 31.

If PCM are at 4 Mb/s

N1 PCM at 4 Mb/s: 0 or 1

TS0/4 and N0 Time Slot number 0 to 63
(N0 = TS5)

If PCM is at 8 Mb/s

TS0/4 and N0/1 Time Slot Number: 0 to 63
N0 = TS5, N1 = TS6.

PCM = 0 The Destination is Multiplex output or Extraxtion Registers.

If N1 = 0 Multiplexes are selected (GCI or not), then

N0 = 0 Multiplex number: 0

N0 = 1 Multiplex number: 1

TS0/1 Time slot Number: 0 to 31

If N1 = 1 Extraction Registers are selected, then

N0 = 0 and TS0/4 = 0 A Extraction Register 40 (H) is the destination

N0 = 1 and TS0/4 = 1 B Extraction Register 41 (H) is the destination

Second Case CM = 0 (Bit of Command Register).

The auxiliary Memory is selected.

PCM	DT6	DT5	DT4	DT3	DT2	DT1	DT0
-	MON	TX	-	M0	G2	G1	G0

PCM Bit is not significant. The other bits are relevant only if multiplex is GCI (See bits of Multiplex Configuration Register : GCI M0 and/or GCI M1).

MON — Command/Indicate

MON = 0. The channel is Command/Indicate

MON = 1. The channel is MON channel.

TX — Transmitter

TX = 1. The transmit channel is selected.

TX = 0. The receive channel is selected.

M0 — Multiplex 0.

M0 = 0. The GCI multiplex 0 is selected.

M0 = 1. The GCI multiplex 1 is selected.

G2/G0 — GCI 0/2

One of eight GCI channels of the multiplex selected (one GCI channel is constituted by five sub-channels : B1, B2, D, C/I and MON).

If Multiplex is not GCI, the GCI channels are not validated. The 32 Time Slots of the multiplex can be used for switching.

STATUS REGISTER (STATUS)

7							0
BID	BUSY	PRSR	MONR	MONT	CIR	EXT	INS

After Reset 00 (H)

Each bit of this register is read only, except BID (bit) which can be written and read by the microprocessor.

BID — Bi-directional Switching.

BID = 1. two connection paths are established with the same µp instruction.
The µp writes successively into three register: Command Register, Source Register and the Destination register lastly, when the Destination register has been written a write command memory starts to set up the connection required by the µp.
The same information is used to establish a symmetrical connection:
Source register and Destination register are swapped, and so are the SS0/1 and DS0/1 bit of Command Register.

BID = 0: one connection path is established.
The µp writes successively into three register: Command register, Source register and Destination register lastly, when the Destination register has been written a write command memory start to set up the connection required by the µp.

BUSY — Busy.
The memories cannot be accessed if this bit is at ”1”. In this case, a new access of three memory access registers [Command Register (CMD); source Register (SRC) and Destination Register (DST)] will be ignored. If the microprocessor has Twait cycles (working with DTACK or READY), the test BUSY is not necessary.

PRSR — Pseudo Random Sequence Recovered.
When the PRS analyser is validated, PRS bit is put to ”one” if the synchronization is performed.

MONR — Monitor Channel Receive.
When this bit is at ”1”, a byte has been received from one or more Monitor channel. The microprocessor must read the Receive Monitor Status Register (RMS)

MONT — Monitor Channel Transmit.
When this bit is at ”1”, one (or more) channel is transmitting a message and is ready to transmit a new byte of this message.The microprocessor must read the Transmit Monitor Status Register (TMS).
When this bit is at ”0”, each channel is IDLE, and is ready to transmit a new message.

CIR — Command/Indicate Receive.
When this bit is at ”1”, a new primitive has been received from one or more Command/Indicate channel. The microprocessor can read the Receive Command/Indicate Status Register (RCIS).

EXT — Extract Status.
This bit is put ot ”1” when a new byte has been written in the extract registers A or/ and B, when it is at ”1” the Extract Registers can be read during 120 microseconds before changing. The bit is reset after the reading of the STATUS Register.

INS — Insert Status.
When this bit is at ”0”, the Insert Register A or/and B can be written during 120 µs before the next transmission. After the Insert Registers have been written the bit goes automatically to ”1”, the bit is put at ”0” after the reading of the status register.

INSERTION A REGISTER (INS A)

7							0
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0

After Reset 00 (H)

IA 0/7 — This register contains the data to insert during the Time Slot (s) of the output multiplex(es) indicated by the Command Memory. After transferring INS, interrupt is generated

INSERTION B REGISTER (INS B)

7							0
IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

After Reset 00 (H)

IB 0/7 — This register contains the data to insert during the Time Slot(s) of the output multiplex(es) indicated by the Command Memory. After transferring, INS interrupt is generated.

EXTRACTION A REGISTER (EXT A)

7							0
EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0

After Reset 00 (H)

EA 0/7 This register contains the data extracted during the Time Slot of Input multiplex indicated by the Command Memory. After loading, EXT interrupt is generated, in accordance with NEWE bit of Comparison Register

EXTRACTION B REGISTER (EXT B)

7							0
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0

After Reset 00 (H)

EB 0/7 This register contains the data extracted during the Time Slot of Input multiplex indicated by the Command Memory. After loading, EXT interrupt is generated in accordance with NEWE bit of Comparison Register.

INTERRUPT REGISTER (INT)

7							0
LSYNC	PDIF	PRS	MONR	MONT	CIR	EXT	INS

After Reset 00 (H)

LSYNC Lost synchronisation.
LSYNC = 0, PFS signal frequency is correct.

LSYN = 1. PFS signal has not occurred when expected,
or if Double clock the number of clock pulses received is odd,
or the data rate of one PCM received is not Modulo 4 bits at 8 Mb/s,
or the data rate of one PCM received is not Modulo 2 bits at 4 Mb/s.

PDIF PCM different.
PDIF = 1. If one (or more) comparison (validated by the Comparison Register) between PCM is different.

PRS Pseudo Random Sequence .
When the PRS analyser is validated (SAV =1), PRS bit is put to ”one” if the synchronisation is performed or lost (see PRSR bit of Status Register).

MONR Monitor Channel Receive.
When this bit is at ”1”, a byte has been received from the Monitor Channel defined by Receive Monitor Status Register (or an event)

MONT Monitor Channel Transmit.
When this bit is at ”1”, the Monitor Channel (defined by Transmit Monitor Status Register) acknowledges the last command required by the microprocessor.

CIR Command Indicate Receive.
When this bit is at ”1”, a new primitive has been received from the Command/Indicate channel defined by the Receive Command/Indicate Status Register

EXT Extract
When this bit goes to ”1”, the Extract Register A or/and B can be read during 120 microseconds before changing.

INS Insert
When this bit goes to ”1”, the content of Insert Register A or/and B has been transmitted. During 120 microseconds before the next transmission, the microprocessor can write a new word in accordance with TIM (Bit of CR Register).

MASK REGISTER (MASK)

7							0
MLSYNC	MPDIF	MPRS	MMONR	MMONT	MCIR	MEXT	MINS

After Reset FF (H)

Each interrupt of Interrupt Register can be masked by the mask bit associated if this last is at "1".

RECEIVE MONITOR STATUS REGISTER (RMOS)

7							0
EVENT	BYTE	EOM	AB	MO	G2	G1	G0

After Reset 00 (H)

After Reading, Event bit goes to "0".

EVENT — EVENT.
EVENT = 1. An event is occurred concerning the RX Monitor Channel identified by M0, G2, G1, G0.
EVENT = 0. No event occurred concerning the RX Monitor Channels.

BYTE — A new byte is available in Auxiliary Memory. The microprocessor can read this byte

EOM — End of message.
The previous byte which has been taken into account by the microprocessor was the last of the message.

AB — ABORT.
ABORT = 1. The message received has been aborted by the transmitter.

M0 — GCI Multiplex 0 if MO = 0
GCI Multiplex 1 if MO = 1.

G 0/2 — GCI channel 0 to 7 for each multiplex.

TRANSMIT MONITOR STATUS REGISTER (TMOS)

7							0
EVENT	BACK	TO	ABT	MO	G2	G1	G0

After Reset 00 (H)

EVENT — EVENT = 1.
An event is occurred concerning the TX Monitor Channel identified by MO, G2, G1, G0.
EVENT = 0.
No event concerning the TX Monitor Channels.

BACK — Byte acknowledged.
BACK = 1. The current byte transmitted has been acknowledged by the remote receiver.
NB : when EVENT = 1 and TO = 0 and ABT = 0 and BACK = 0, it means end of message. A newmessage can be transmitted.

TO — Time Out.
The remote receiver has not acknowledged the byte transmitted during 1millisecond (the Timer is validated in accordance with TIMD of MultiplexConfiguration 2 Register).

ABT — ABORT.
The byte transmitting has been aborted.

MO — GCI Multiplex 0 if MO = 0
GCI Multiplex 1 if MO = 1.

G 0/2 — GCI channel 0 to 7 for each multiplex.

RECEIVE COMMAND/INDICATE STATUS REGISTER (RCIS)

7							0
EVENT	RRP	OVR	0	MO	G2	G1	G0

After Reset 00 (H)

EVENT — EVENT = 1.
A primitive has been received twice identically. The number of Command/Indicate channels is give by MO, G2, G1, G0.

RRP — Read Receive Primitive
RRP = 1 the mp has to read the primitive received in order to allow the next on to be processed.

OVR — OVERRUN
OVR = 1. The previous primitive has not been read by the microprocessor.

MO — If MO = 0, Multiplex 0
if MO = 1, Multiplex 1.

G 0/2 — GCI 0 to GCI 7 channel of each multiplex.

TEST REGISTER (TEST)

7							0
FWD	WITG	DCA	SAV	LP	PRSC	DCG	SGV

After Reset 00 (H)

FWD — False Word Detection
FWD = 1, the counter indicates the number of wrong bytes
FWD = 0, the counter indicates the number of wrong bits.

WITG — Word integrity.
WITG = 1. The first bit of the Pseudo Random Sequence (2*11-1) is the firstbit of the channel (or subchannel) selected in the Time Slot at the beginning of the transmission.
‘ WITG = 0. The first bit of the PRS is transmitted without taking into accountthe place in the Time Slot.

DCA — Double channel for analyser.
DCA = 1. The analyser receives Pseudo Random Sequence from two channels.
DCA = 0. The analyser receives Pseudo Random Sequence from one channel.

SAV — Sequence Analyser Validation. When this bit goes to ”1”, the Analyser of Pseudo Random Sequence (2*11-1) is connected instead of Extract A Register i f DCA = 0, instead of Extract A and Extract B registers if DCA = 1. Then the synchronisation is researched.
When SAV = 0, the analyser is initiated.
NB : When DCA= 0, Insert B register can be used normally.

LP — Loopback.
When LP = 1, the six data streams going out (PCM 0/3 and MUX 0/1) are respectively connected instead of data stream coming from the 6 inputs (PCM 0/3 and MUX 0/1). The loopback is transparent or not, depending on M0D,M1D, P0E, P1E, P2E, P3E bits of Multiplex and PCM Configuration Registers.

PRSC — Pseudo Random Sequence Corrupted.
When this bit changes from 0 to 1, one PRS bit is corrupted if DCG = 0, two PRS bits are corrupted if DCG = 1 (one bit in each channel). After transmitting corrupted bit(s), PRSC changes from ”1” to” 0”.

DCG — Double channel for Generator.
DCG = 1. The generator transmits Pseudo Random Sequence to two channels.
DCG = 0. The generator transmits Pseudo Random Sequence to one channel.

SGV — Sequence Generator Validation.
When this bit goes to ”1”, the generator provides Pseudo Random Binary Sequence 2 * 11-1 in accordance with CCITT Recommendation O.152. The generator is

connected instead of Insert A Register if DCG = 0, and instead of Insert A and Insert B Registers if DCG = 1.
When SGV goes to ”1”, the current contents of Command Register (CMD) is taken into account by the generator. In this case, Command Register means :

7							0
0	0	BCH1	BCH0	0	0	ACH1	ACH0

BCH1/0 Insert B channel 1/0.
If generator transmits sequence instead of Insert B register, the data rate for this channel is given by BCH1/0

BCH1	BCH0	
0	0	8 kb/s
0	1	16 kb/s
1	0	32 kb/s
1	1	64 kb/s

ACH1/0 Insert A channel 1/0
If generator transmits sequence instead of insert A Register, the data rate for this channel is given by ACH1/0.

ACH1	ACH0	
0	0	8 kb/s
0	1	16 kb/s
1	0	32 kb/s
1	1	64 kb/s

If DCG = 1, the data rate of PRS generator is the sum of data rate Insert B channel and Insert A channel.
If DCG = 0, the data rate of PRS generator is equal to data rate of Insert A channel.

ERROR COUNTER REGISTER (ECR)

7							0
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

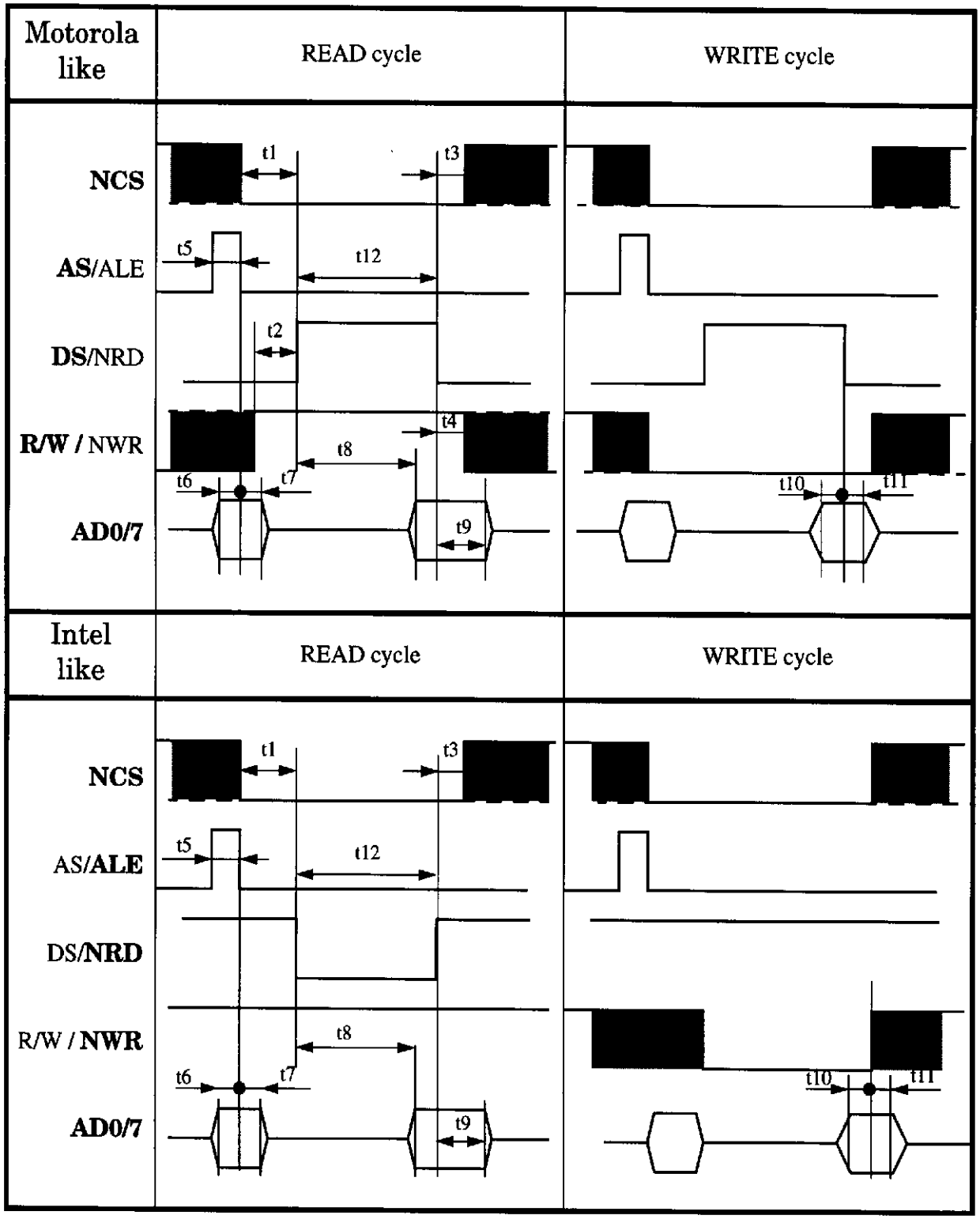
After RESET 00 (H).

If the Pseudo Random Sequence Analyser is validated (SAV = 1), this register indicates the number of errored bits received after the synchronisation of the Pseudo Random Sequence. When Error Counter Register indicates all ”1”s, the synchronisation is lost. After reading by the microprocessor, ECR is put to ”0”.

MICROPROCESSOR INTERFACE TIMING

tx	Parameter	T min	T max	Unit
t1	Set up time Not Chip Select / DS/NRD	10		ns
t2	Set up time R/W / NWR / DS/NRD	10		ns
t3	Hold time Not Chip Select / DS/NRD	0		ns
t4	Hold time R/W / NWR / DS/NRD	0		ns
t5	Width AS/ALE	20		ns
t6	Set up time Address / AS/ALE	10		ns
t7	Hold time Address / AS/ALE	10		ns
t8	Data valid after DS/NRD (rising edge) (30 pF)		40	ns
t9	Hold time Data after DS/NRD (falling edge)	0		ns
t10	Hold time Data / DS/NRD	10		ns
t11	Set up time Data / DS/NRD	10		ns
t12	Width DS/NRD	30		ns
t13	NRDY/NWAIT delay DS/NRD	30		ns
t14	NRDY/NWAIT delay / Data	0		ns
t15	NRDY/NWAIT delay / DS/NRD NRDY/NWAIT delay / R/W / NWR		30	ns

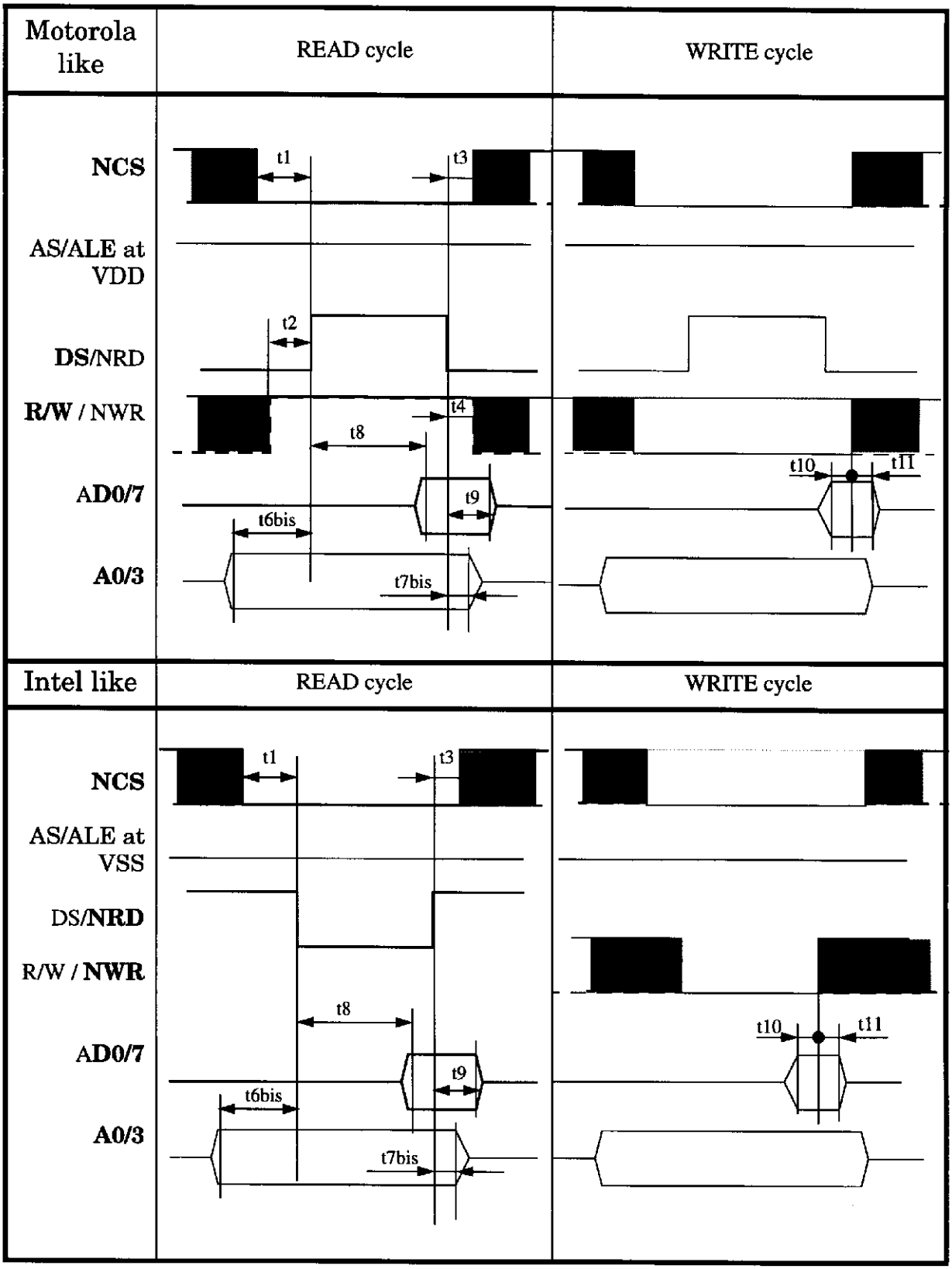
MICROPROCESSOR INTERFACE TIMING
Multiplexed Address/Data Microprocessor interface



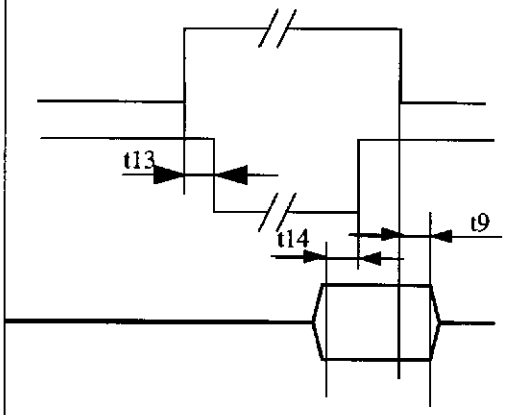
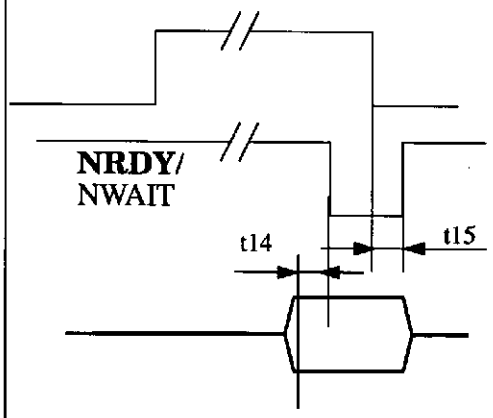
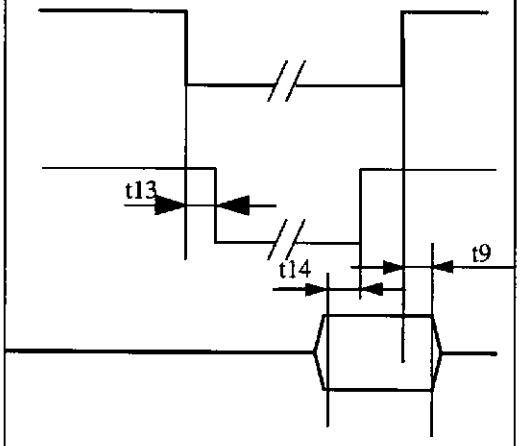
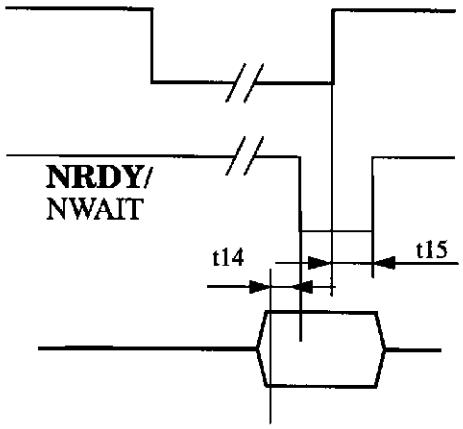
In this diagram, the polarity of signals is given for A1, A2, A3 at VDD.
READ cycle and WRITE cycle are without waiting.

MICROPROCESSOR INTERFACE TIMING

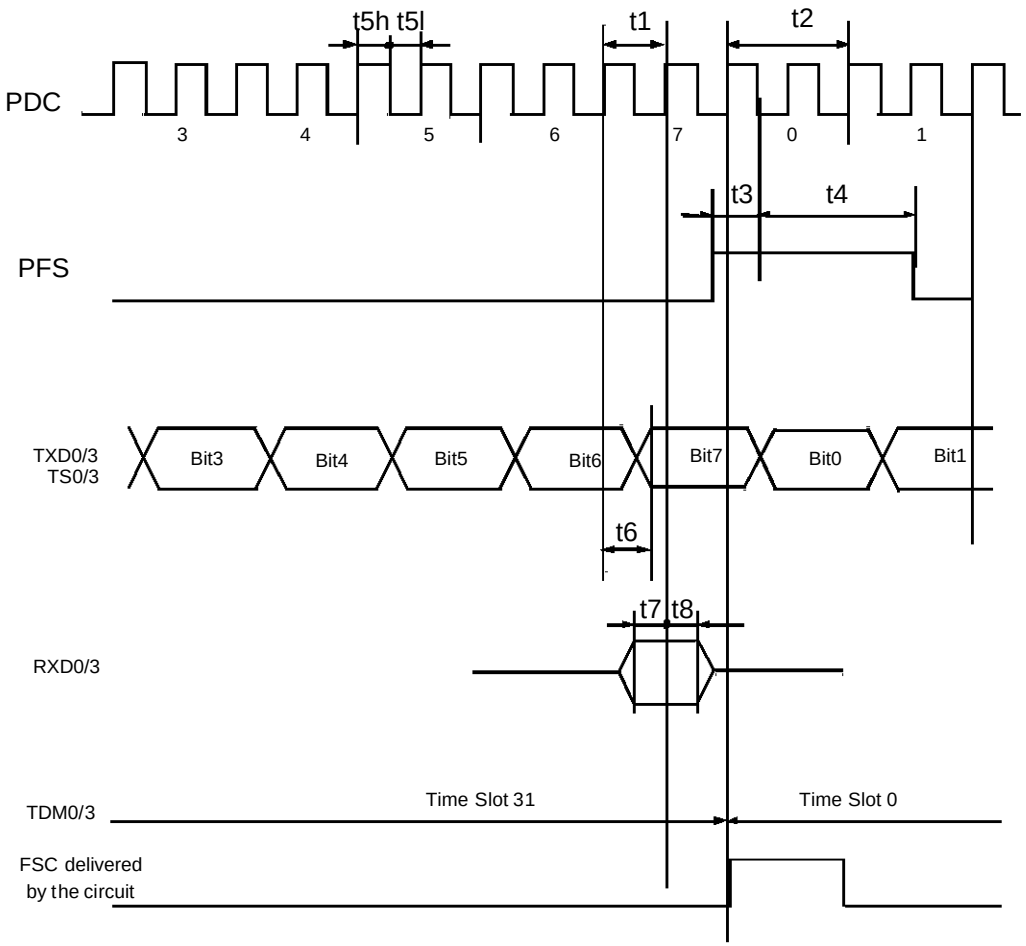
Non-multiplexed Address/Data Microprocessor interface



MICROPROCESSOR INTERFACE TIMING
Variable Cycle Microprocessor interface

Motorola like	NWAIT	NREADY
DS/NRD NRDY/ **NWAIT** **AD0/7 Read cycle**		
Intel like	**NWAIT**	**NREADY**
DS/**NRD** or R/W / **NWR** NRDY/ **NWAIT** **AD0/7 Read cycle**		

CLOCK TIMING
Synchronization signals delivered by the system

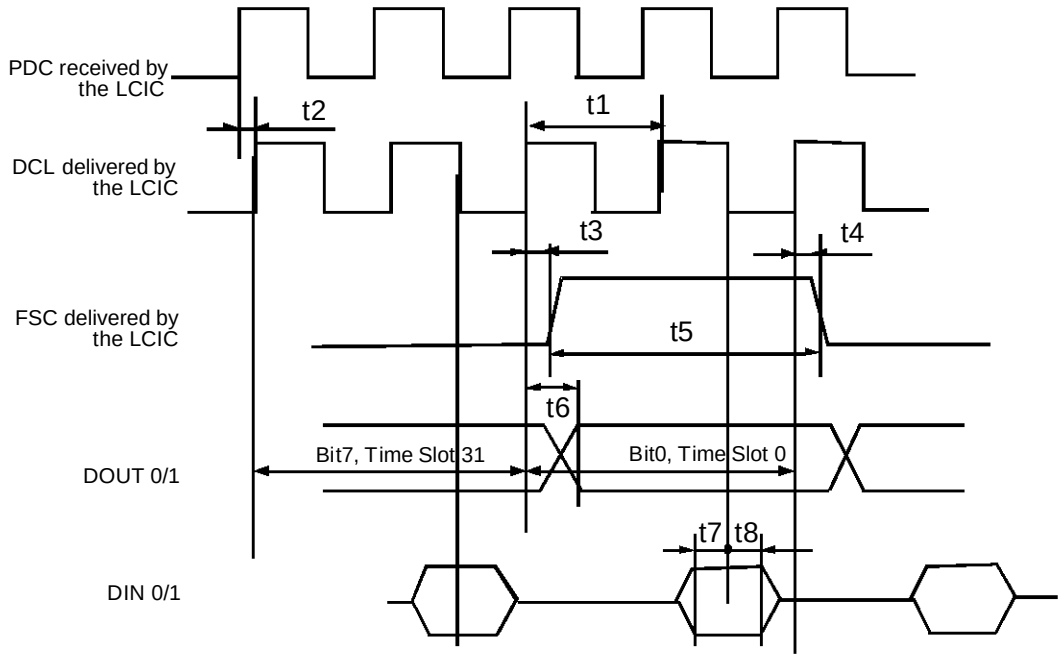


DEL, ISPP and PFSP bits of PCM Configuration Register are at zero (no delay))

Clocks received by the LCIC

tx	Parameter	T min.	T typ.	T max.	Unit
t1=1/f1	Clock Period if f1 = 16384KHz Clock Period if f1 = 8192KHz Clock Period if f1 = 4096KHz	60 120 239	61 122 244	62 124 249	ns ns ns
t2	Bit-time if f1 = 16384KHz Bit-time if f1 = 8192KHz Bit-time if f1 = 4096KHz		122 244 488		ns ns ns
t3	Set up time PFS/PDC	20		t1-20	ns
t4	Hold time PFS/PDC	20		12500-t1	ns
t5	Clock ratio t5h/t5l	75	100	125	%
t6	PDC to data 50pF PDC to data 100pF			50 100	ns ns
t7	Set up time data/DCL	20			ns
t8	Hold time data/DCL	20			ns

CLOCK TIMING
TDM synchronization



The four Multiplex Configuration Registers are at zero (no delay between FSC and Multiplexes)

Clocks delivered by the LCIC

tx	Parameter	T min.	T typ.	T max.	Unit
t1	Clock Period if 4096KHz Clock Period if 2048KHz	Id PDC	244 488	Id PDC	ns ns
t2	Delay between PDC and DCL (30pF)		5	30	ns
t3	Delay between DCL and rising edge FSC (30pF)			30	ns
t4	Delay between DCL and falling edge FSC (30pF)			30	ns
t5	Duration FSC		488		ns
t6	DCL to data 50pF DCL to data 100pF			50 100	ns ns
t7	Set up time data/DCL	20			ns
t8	Hold time data/DCL	20			ns

DC SPECIFICATION

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	5V Power Supply Voltage	-0.5 to 6.5	V
	Input or Output Voltage	-0.5, VDD +0.5	V
T_{stg}	Storage Temperature	-55, +125	°C

Power Dissipation

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P	Power Consumption	V_{DD} = 5.25V		105	135	mW

Recommended DC Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	5V Power Supply Voltage		4.75		5.25	mW
T_{oper}	Operating Temperature		-40		+85	°C

Note 1: All the following specifications are valid only within these recommended operating conditions.

TTL Input DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
I_{IL}	Low Level Input Current	V_I = 0V			1	µA
I_{IH}	High Lvel Input	$V_i = V_{DD\ Max}$			-1	µA
I_{IH_PULLUP}	High level input current for pullup	$Vi = V_{DD\ Max}$			-50	µA
C_{IN}	Input Capacitance (see Note 2)	f = 1MHz @ 0V		2	4	pF
C_{OUT}	Output Capacitance			4		pF
$C_{I/O}$	Bidir I/O Capacitance		4	8		pF

Note 2: Excluding package

CMOS Output DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	I_{OL} = 4mA I_{OL} = 2mA			0.5 0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = 4mA I_{OH} = 4mA	V_{DD}-0.5 V_{DD}-0.4			V

Protection

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ESD}	Electrostatic Protection	C = 100pF, R = 1.5kΩ	2000			V

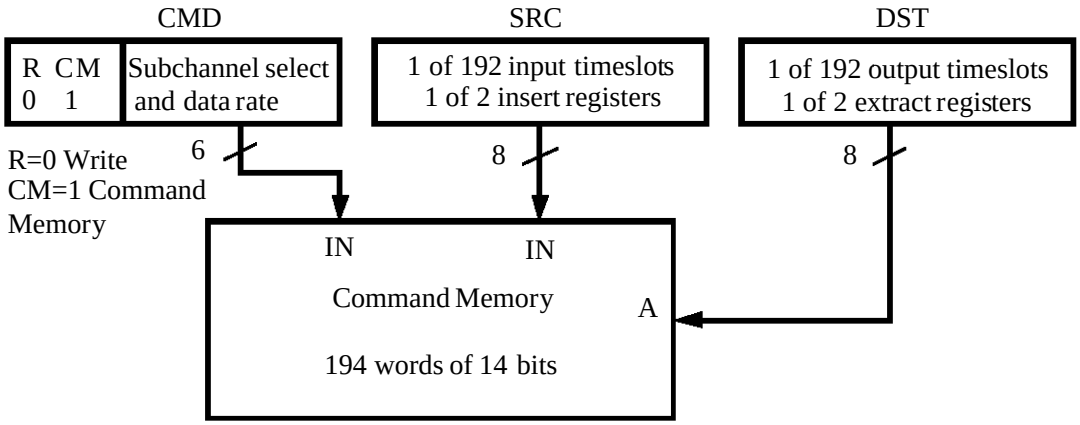
APPENDIX

MEMORY ACCESSES

COMMAND MEMORY ACCESSES. CM=1

Write Command Memory:

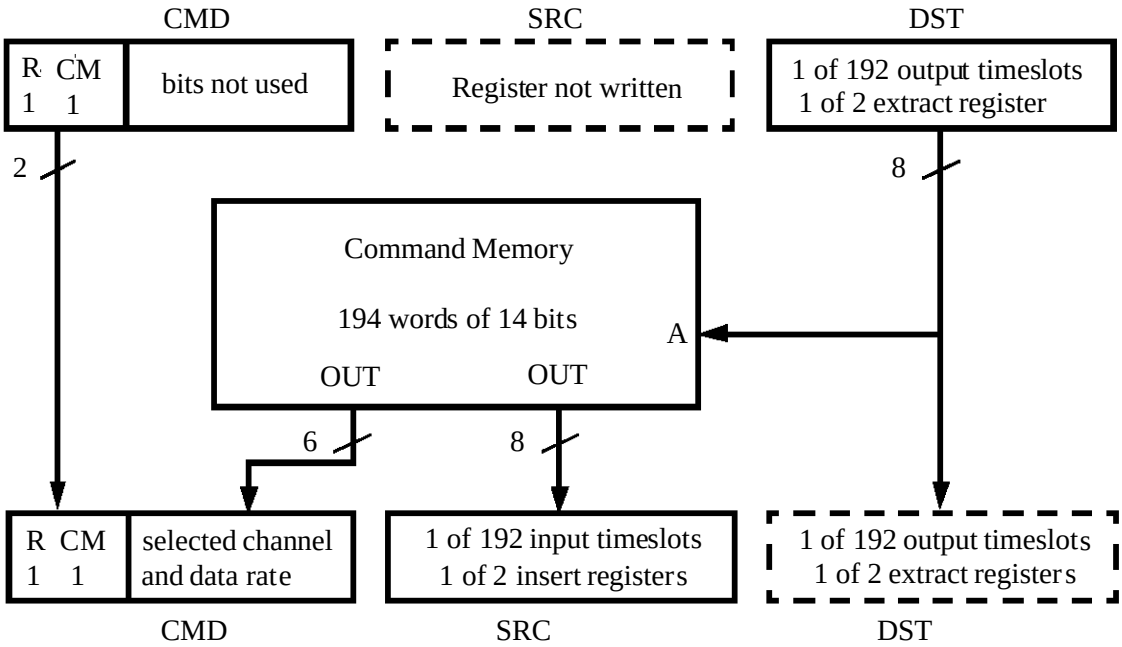
CMD and SRC registers are written if their bits have not the right value.
CMD and SRC registers can be written in any order.
DST register is always written the last



Read Command Memory in two steps:

First step: register writing

CMD register is written if its bits are not the right value.
SRC register is not written.
DST register is always written the last.



Second step: register reading:

CMD and SRC registers may be read in any order.
DST register is not changed.

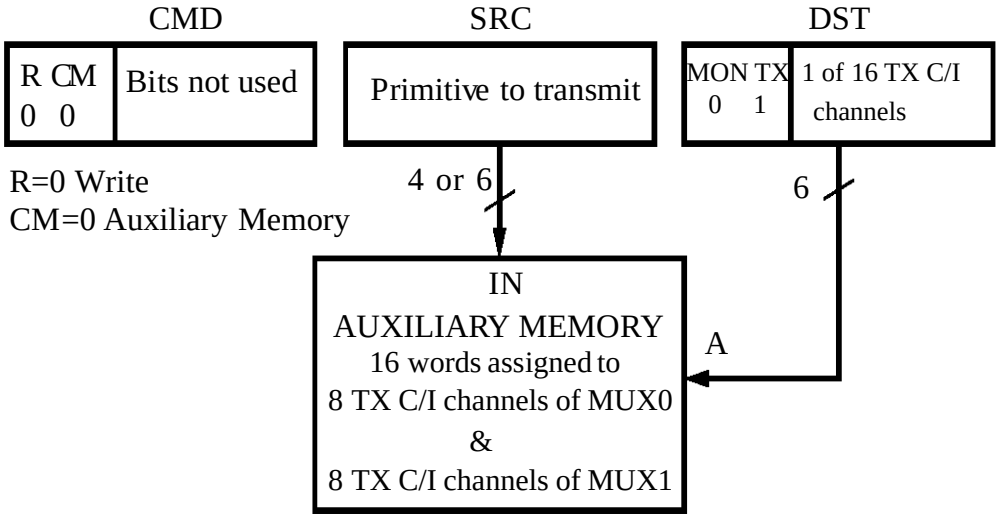
AUXILIARY MEMORY ACCESSES: CM=0

Write Auxiliary Memory: **Transmit command / indicate** channels

CMD and SRC registers are written if their bits have not the right value.

CMD and SRC registers can be written in any order.

DST register is always written the last.



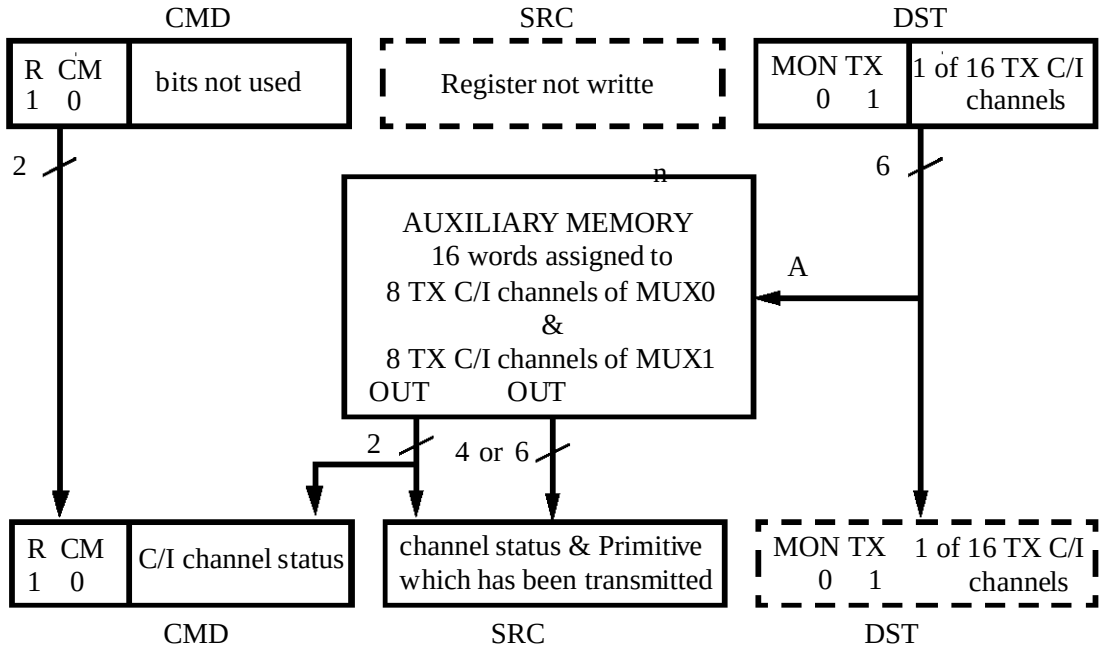
Read Auxiliary Memory in two steps: **Transmit command / indicate** channels

First step: register writing:

CMD register is written if its bits are not the right value.

SRC register is not written.

DST register is always written the last.



Second step: register reading:

CMD and SRC registers may be read in any order.
DST register is not changed.

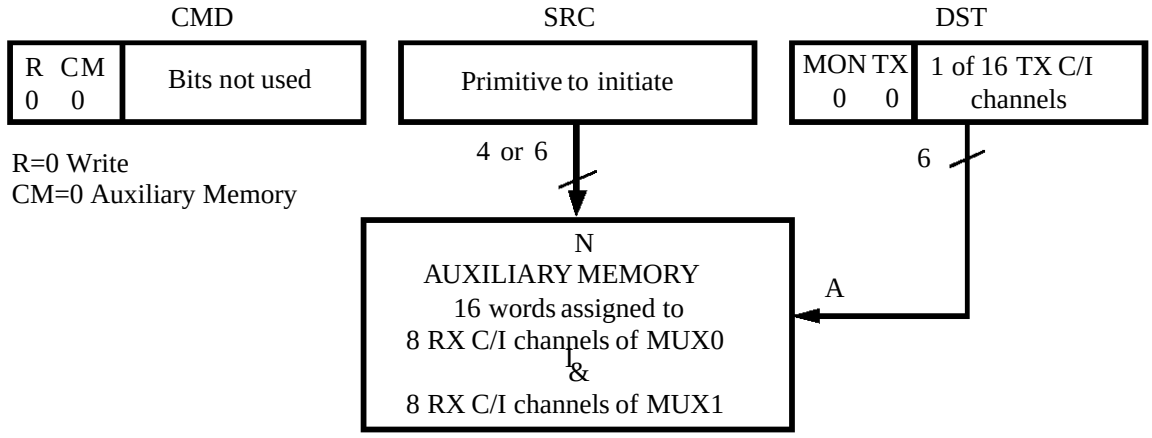
AUXILIARY MEMORY ACCESSES: CM=0

Write Auxiliary Memory: **Receive command / indicate** channels

CMD and SRC registers are written if their bits have not the right value.

CMD and SRC registers can be written in any order.

DST register is always written the last.



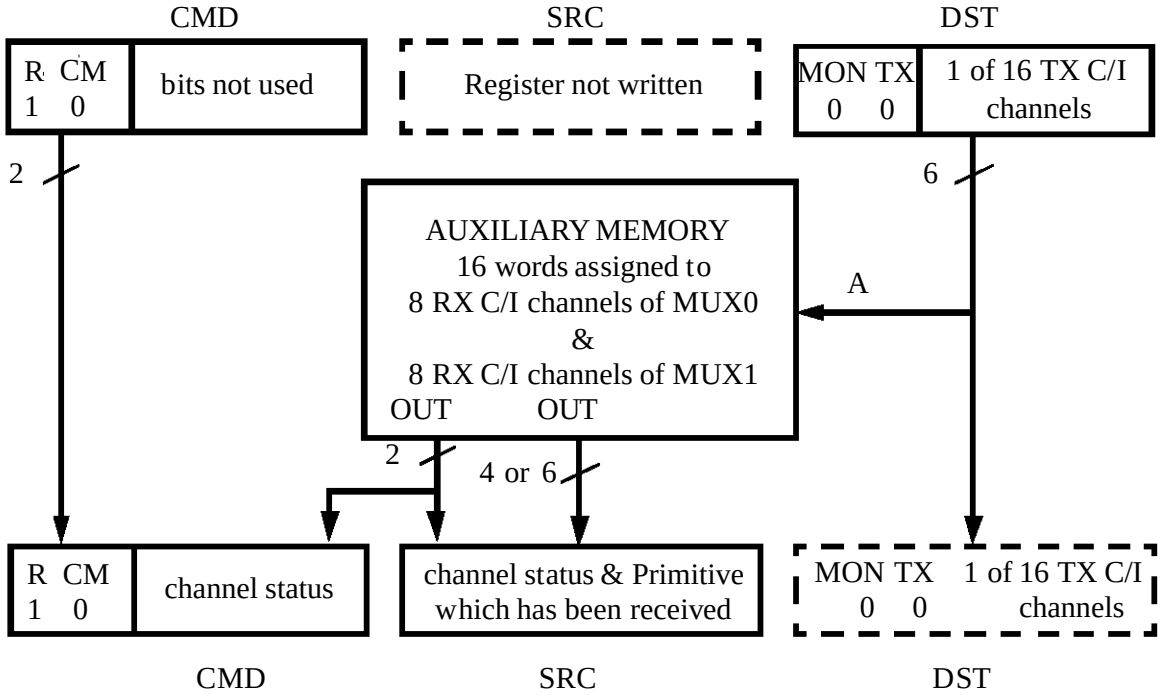
Read Auxiliary Memory in two steps: **Receive command / indicate** channels

First step: register writing:

CMD register is written if its bits are not the right value.

SRC register is not written.

DST register is always written the last.



Second step: register reading:

CMD and SRC registers may be read in any order.

DST register is not changed.

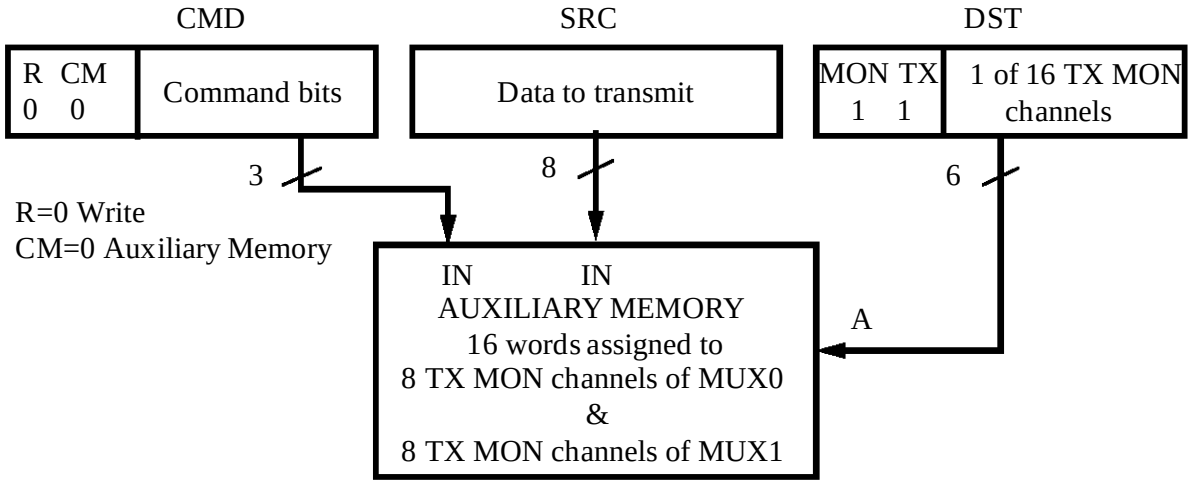
AUXILIARY MEMORY ACCESSES: CM=0

Write Auxiliary Memory: **Transmit Monitor** channels

CMD and SRC registers are written if their bits have not the right value.

CMD and SRC registers can be written in any order.

DST register is always written the last.



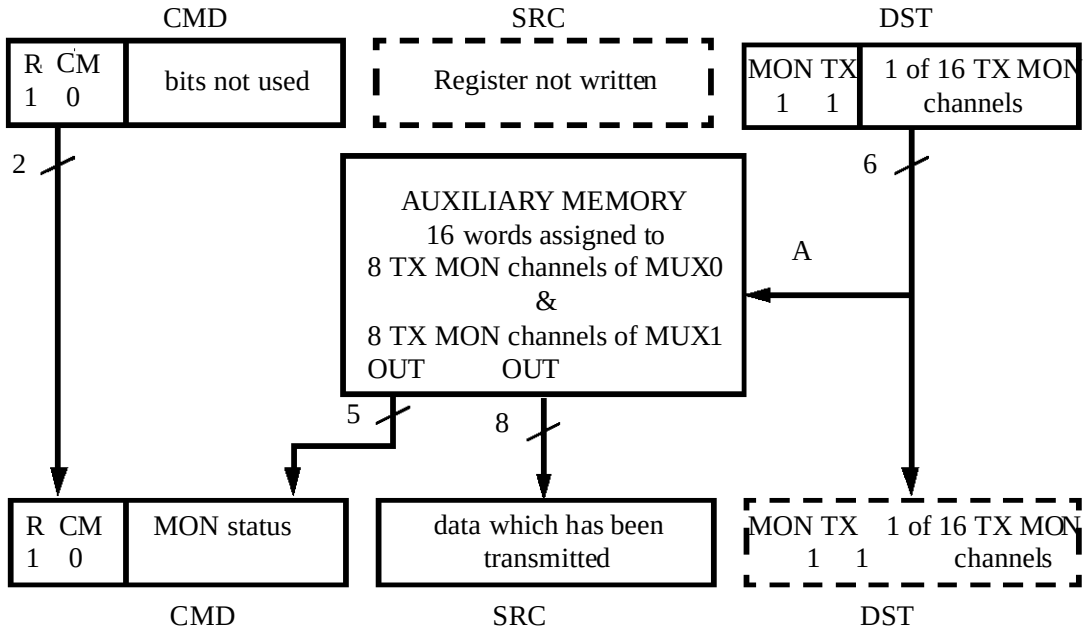
Read Auxiliary Memory in two steps: **Transmit Monitor** channels

First step: register writing:

CMD register is written if its bits are not the right value.

SRC register is not written.

DST register is always written the last.



Second step: register reading:

CMD and SRC registers may be read in any order.

DST register is not changed.

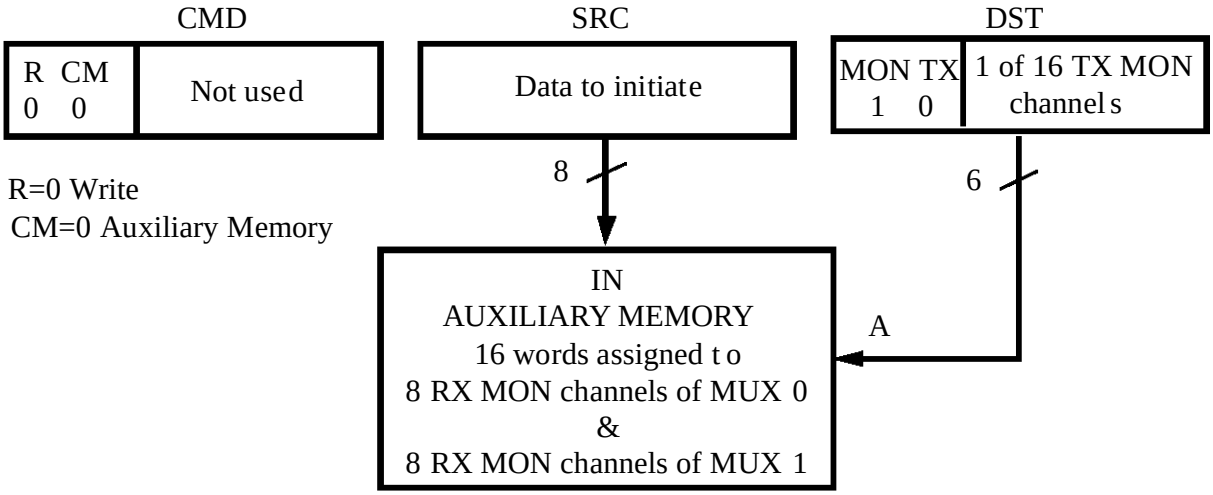
AUXILIARY MEMORY ACCESSES: CM=0

Write Auxiliary Memory: **Receive Monitor** channels

CMD and SRC registers are written if their bits have not the right value.

CMD and SRC registers can be written in any order.

DST register is always written the last.



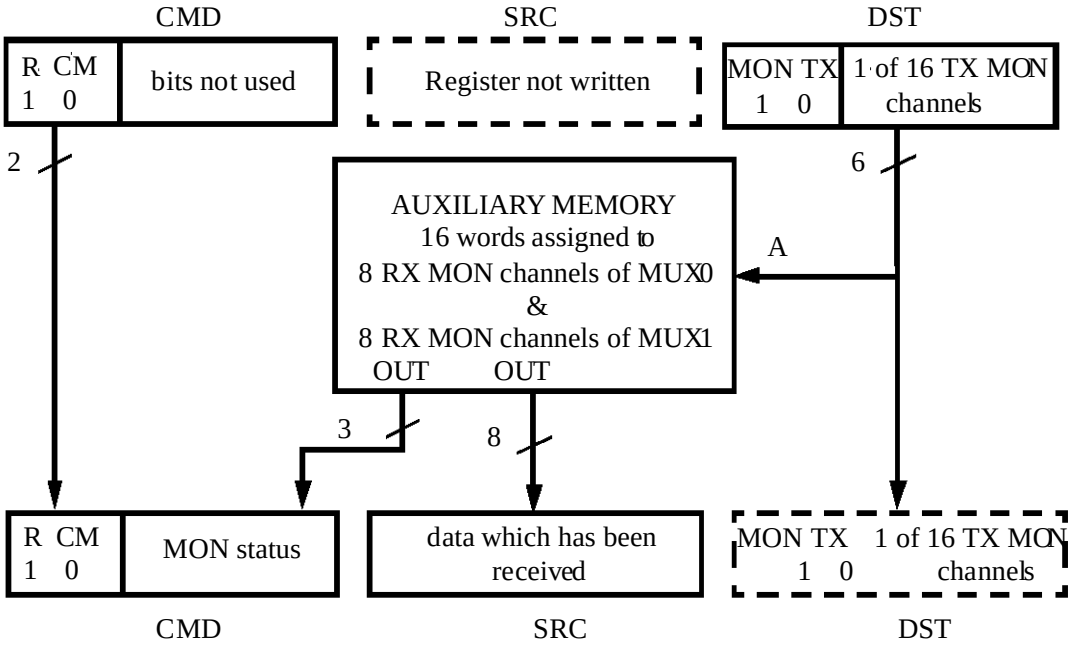
Read Auxiliary Memory in two steps: **Receive Monitor** channels

First step: register writing:

CMD register is written if its bits are not the right value.

SRC register is not written.

DST register is always written the last.



Second step, register reading:

CMD and SRC registers may be read in any order.

DST register is not changed.

Table 1: Data Memory Address

INPUT	Source Register							
	PCM	N1	N0	TS4	TS3	TS2	TS1	TS0
PCM 0	1	0	0	TS 0 to TS 31				
PCM 1		0	1	TS 0 to TS 31				
PCM 2		1	0	TS 0 to TS 31				
PCM 3		1	1	TS 0 to TS 31				
MUX 0	0	0	0	TS 0 to TS 31				
MUX 1			1	TS 0 to TS 31				
INSERT REG. A		1	0	0	0	0	0	0
INSERT REG. B			0	0	0	0	0	1

Table 2: Control Memory Address

INPUT	Destination Register							
	PCM	N1	N0	TS4	TS3	TS2	TS1	TS0
PCM 0	1	0	0	TS 0 to TS 31				
PCM 1		0	1	TS 0 to TS 31				
PCM 2		1	0	TS 0 to TS 31				
PCM 3		1	1	TS 0 to TS 31				
MUX 0	0	0	0	TS 0 to TS 31				
MUX 1			1	TS 0 to TS 31				
EXTRACT REG. A		1	0	0	0	0	0	0
EXTRACT REG. B			0	0	0	0	0	1

Table 3: Auxiliary Memory Addresss

MUX	CHANNEL		Destination Register							
			-	MON	TX	-	M0	G2	G1	G0
MUX 0	CI	RX	-	0	0	-	0	GCI channel 0 to 7		
		TX		0	1			GCI channel 0 to 7		
	MON	RX		1	0			GCI channel 0 to 7		
		TX		1	1			GCI channel 0 to 7		
MUX 1	CI	RX		0	0		1	GCI channel 0 to 7		
		TX		0	1			GCI channel 0 to 7		
	MON	RX		1	0			GCI channel 0 to 7		
		TX		1	1			GCI channel 0 to 7		

Table 4: Auxiliary Memory Data

CHANNEL	Source Register							
TX Command Indicate	-	-	C6	C5	C4	C3	C2	C1
RX Command Indicate	OVR	PR	C6	C5	C4	C3	C2	C1
TX and RX Monitor	M8	M7	M6	M5	M4	M3	M2	M1

C1/6: Primitive
PR: Primitive received
OVR: Overrun
M1/8: Byte

MEMORY ACCESS ALGORITHM

Figure 4: Control or Auxiliary Memory Accesses

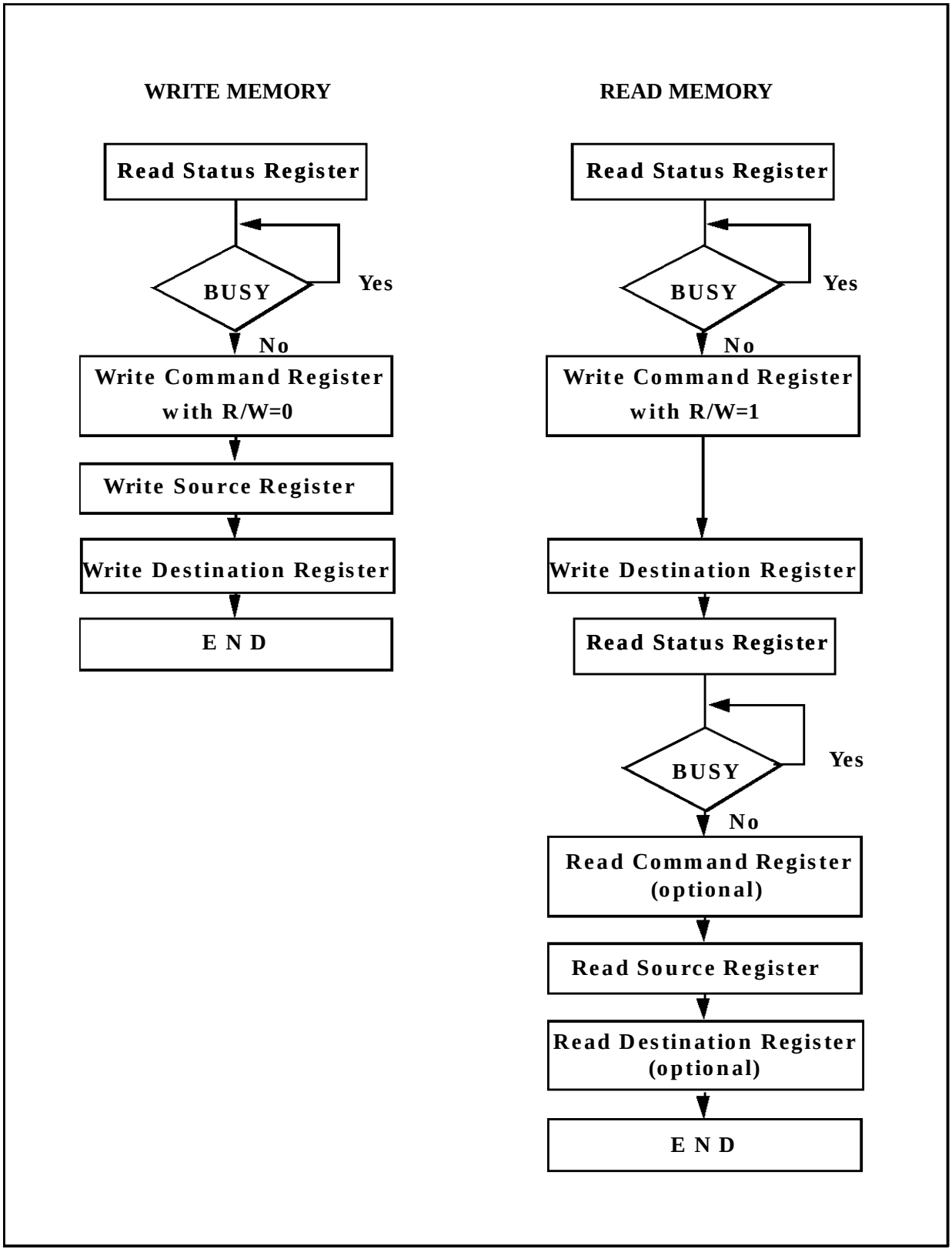


Figure 5: Bidirectional Switching

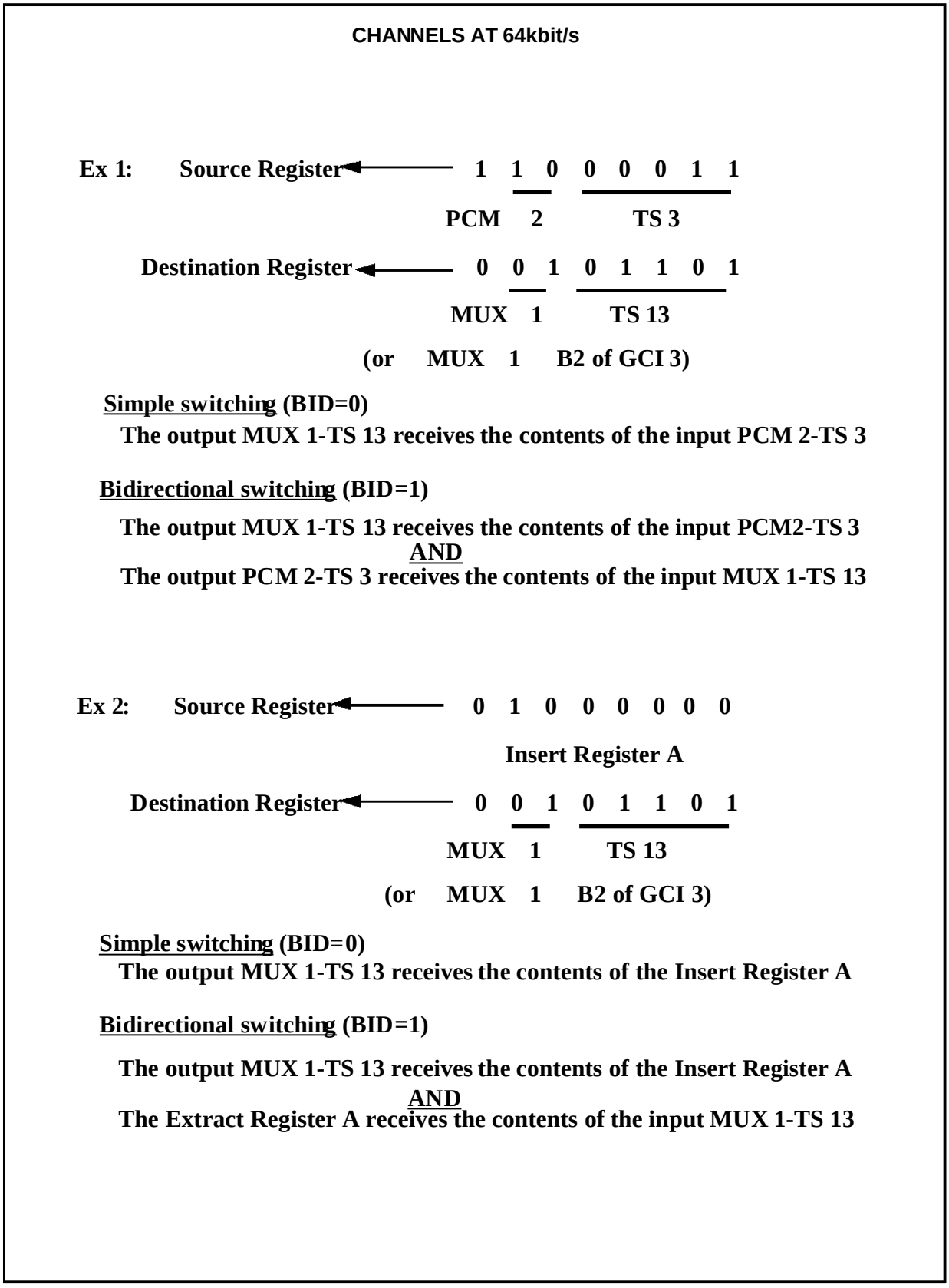


Figure 6: Bidirectional Switching and Loopback

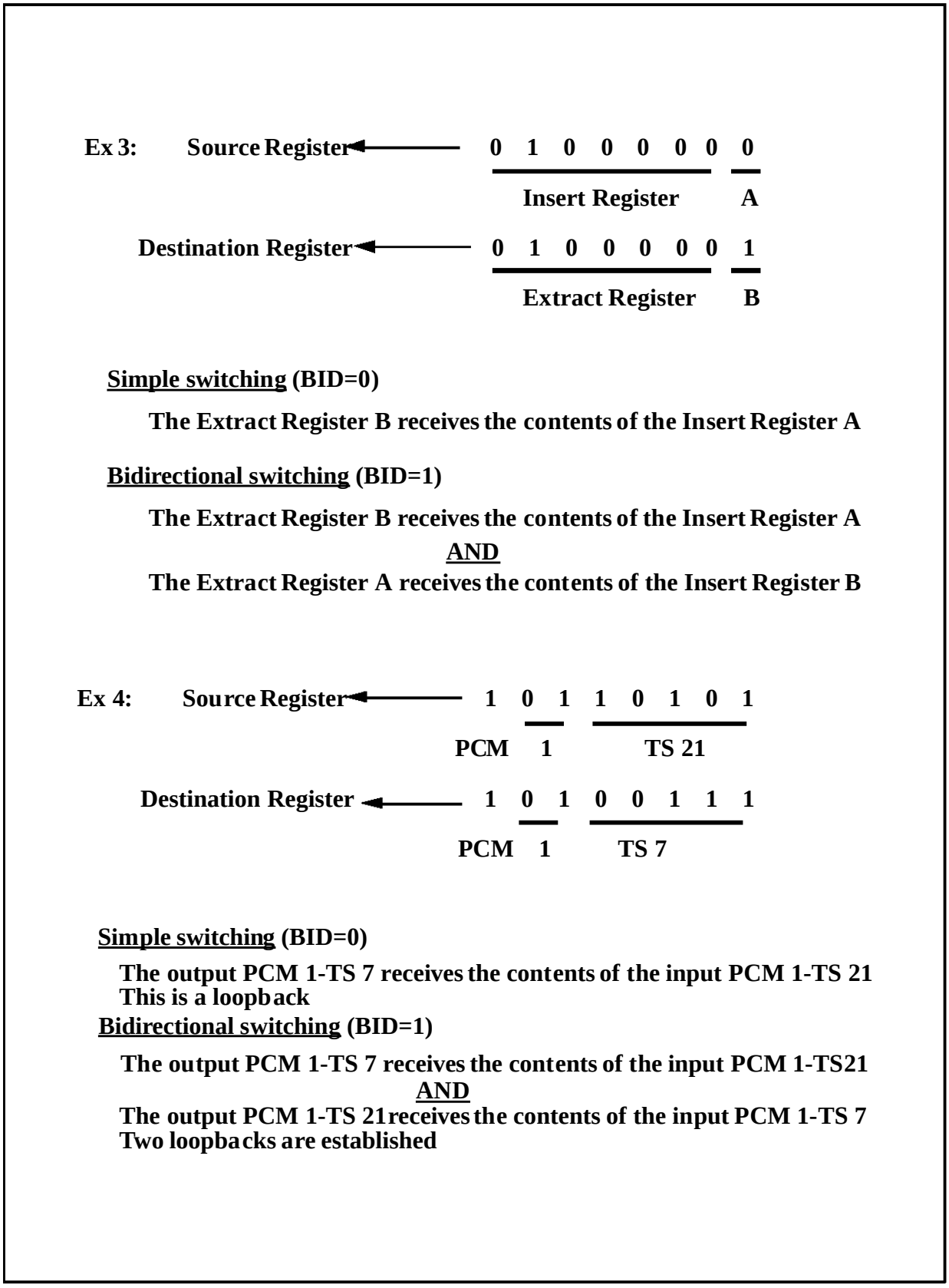


Figure 7: Switching & Broadcast

One source to several destinations

Ex 5:PCM to MUX

Source Register ← 1 0 1 0 0 0 1 0

PCM 1 TS 2

Destination Register ← 0 0 1 0 1 1 0 1

MUX 1 TS 13

(or MUX 1 B2 of GCI 3)

Destination Register ← 0 0 0 1 1 0 0 1

MUX 0 TS 25

(or MUX 0 B2 of GCI 6)

Broadcast

The output MUX 1-TS 13 receives the contents of the input PCM 1-TS 2

AND

The output MUX 0-TS 25 receives the contents of the input PCM 1-TS 2

and so on

Ex 6:Insert Register A to MUX

Source Register ← 0 1 0 0 0 0 0 0

Insert Register A

Destination Register ← 0 0 0 1 1 1 0 0

MUX 0 TS 28

(or MUX 0 B1 of GCI 7)

Destination Register ← 0 0 1 1 0 1 0 1

MUX 1 TS 21

(or MUX 1 B2 of GCI 5)

Broadcast

The output MUX 0-TS 28 receives the contents of the Insert Register A

AND

The output MUX 1-TS 21 receives the contents of the Insert Register A

Figure 8: Bidirectional Switching Channels at 16kbit/s

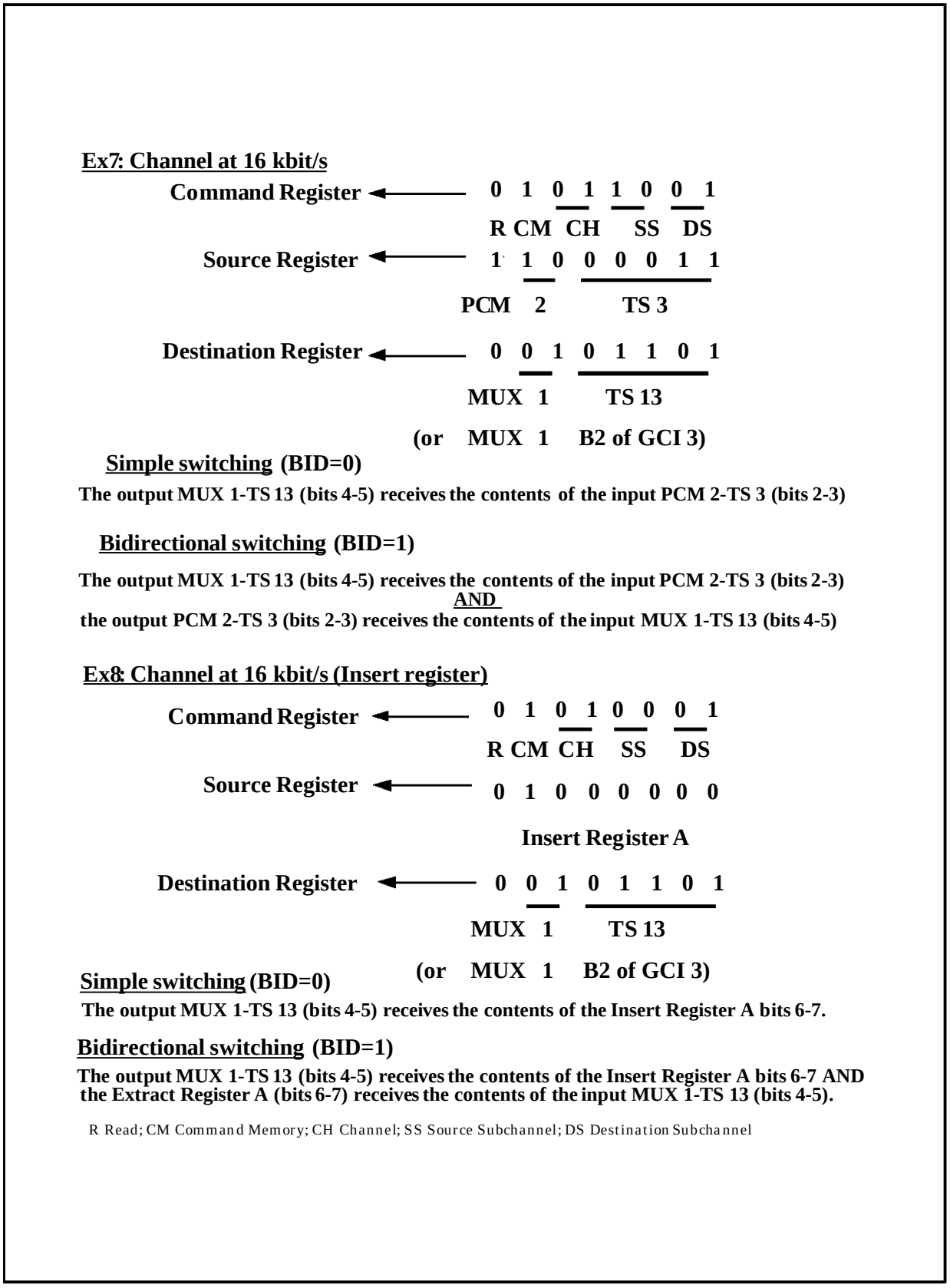
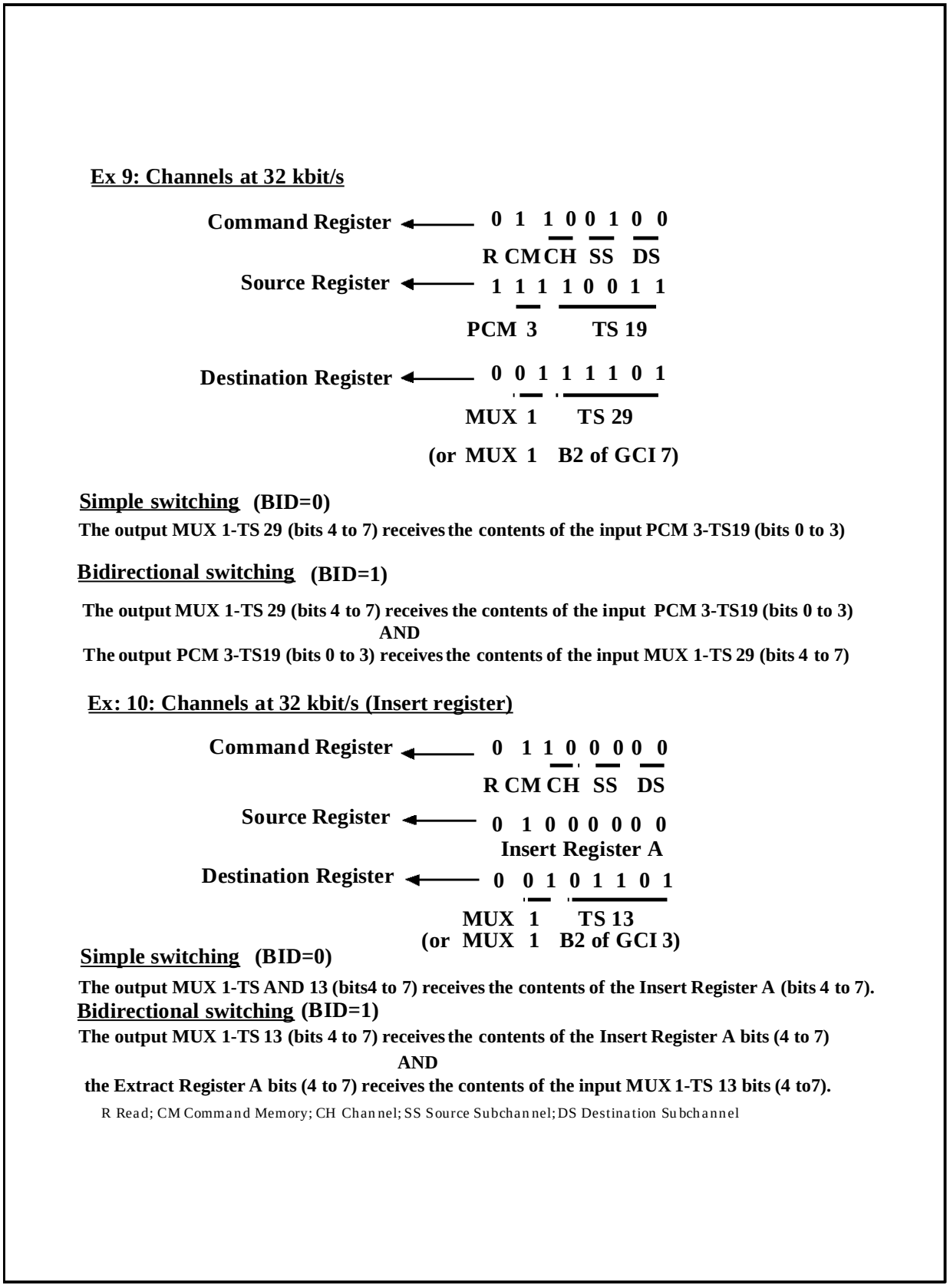
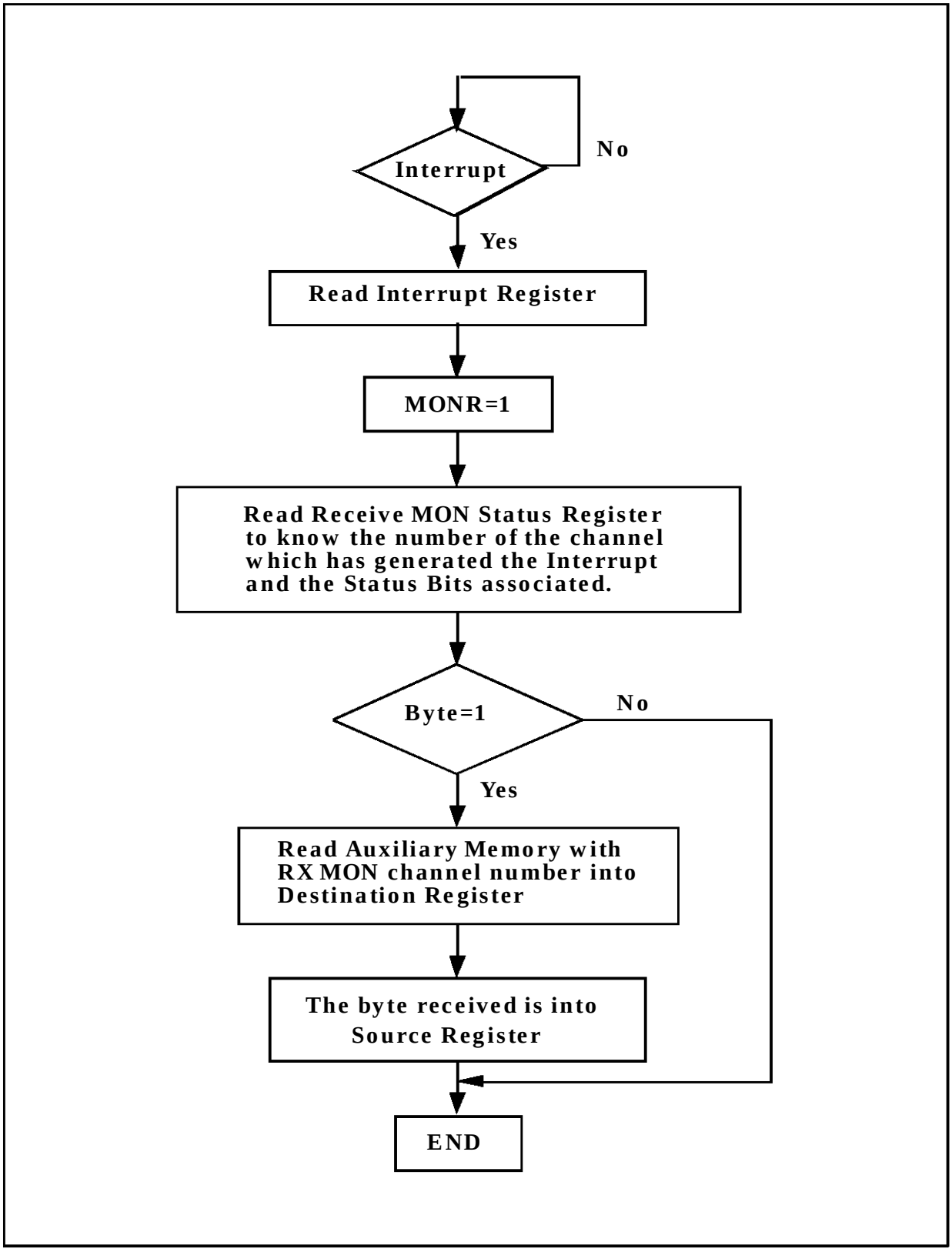


Figure 9: Bidirectional Switching Channels at 32kbit/s



INTERRUPT EXAMPLE

Figure 10: Interrupt Generated by RX Monitor Channel.



PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045