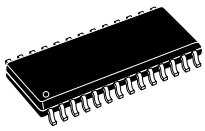
STLC60133N

XDSL LINE DRIVER

PRODUCT PREVIEW

- LOW NOISE : 4nV/$\sqrt{Hz}$
- HIGH PEAK OUTPUT CURRENT: 500 mA
- HIGH SPEED
  - 140MHz Gain Bandwidth
  - 30MHz Gain Flatness
  - 400 V/us Slew Rate
- LOW POWER OPERATION
  - ±5V to ±15V Voltage Supply
  - 3.5 mA/Amp (typ) Supply current
  - Power reduced Current
- LOW SINGLE TONE DISTORTION
- THERMAL AND OVERLOAD PROTECTION
- HTSSOP28 PACKAGE
- -40 TO +85°C OPERATING RANGE



HTSSOP28

ORDERING NUMBER: STLC60133N

Temperature Range: -40°C to +85°C

DESCRIPTION

The STLC60133N is a dual amplifier featuring a high slew rate and a large bandwidth optimized for XDSL applications. The device is available in a HTSSOP 28 pin package (4x9 mm) with an exposed leadframe.

Thanks to its small package this line driver is suitable for high density ADSL line card.

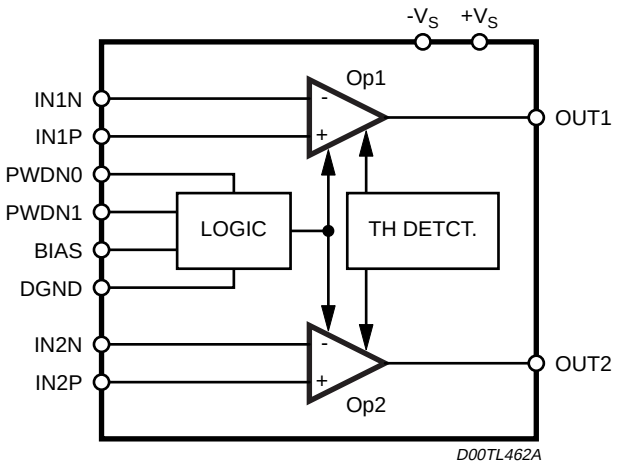
Two digital pins (PWDN0 and PWDN1) allow the driver to work in full performance mode, in low-power mode or two intermediate bias states.

The low-power mode biases the output stage in order to provide a low impedance at the amplifier outputs for back termination.

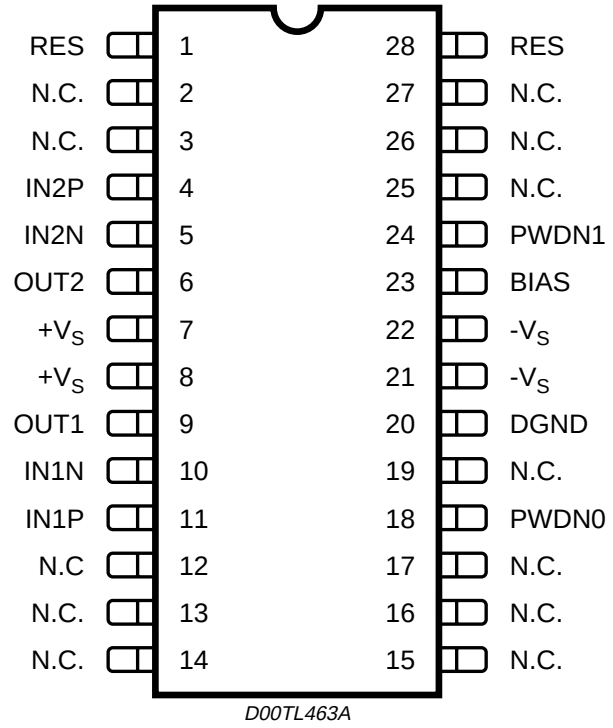
The STLC60133N is designed optimizing bandwidth and distortion performances. For proper device operating it is necessary to work with a gain level greater than 15.6dB.

Typical differential gain is normally +27dB, while typical common mode gain is 15.6dB

Figure 1. BLOCK DIAGRAM



PIN CONNECTION



D00TL463A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive Supply voltage (note1)	+16.5	V
V_{SS}	Negative Supply voltage (note1)	-16.5	V
V_{id}	Differential Input Voltage (note2)	±5	V
V_i	Common mode Input Voltage	±1	V
T_{op}	Operating Free Air Temperature Range	-40 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Junction temperature	165	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient (note 3)	29	°C/W

OPERATING RANGE

Symbol	Parameter	Value	Unit
T_{op}	Operating Temperature Range	-40 to 85	°C
V_{CC}	Positive Supply voltage (note1)	+5 to +15	V
V_{SS}	Negative Supply voltage (note1)	-5 to -15	V
V_{DGND}	Digital Ground level	$V_{SS}<V_{DGND}<V_{CC}-5$	V
V_{icm}	Common Mode Input Voltage Range	±1	V

Notes
1) All voltages values , except differential voltage , are with respect to network ground terminal .
2) Differential voltages are non-inverting input terminal with respect to the inverting input terminal
3) Specification is for device on a 4 layer board within 10 square inches of oz. copper at +85°C and 200m/s air velocity. With 0m/s air velocity the parameter increases up to 33°C/W

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PIN DESCRIPTION

N°	Pin	Description
1, 28	RES	To be left not connected
2, 3, 12, 13, 14, 15, 16, 17, 19, 25, 26, 27	NC	Not Connected
4	IN2P	Non Inverting Input of Op. Amplifier 2
5	IN2N	Inverting Input of Op. Amplifier 2
6	OUT2	Ouput of Op. Amplifier 2
7, 8	+Vs	Positive Supply Voltage
9	OUT1	Ouput of Op. Amplifier 1
10	IN1N	Inverting Input of Op. Amplifier 1
11	IN1P	Non Inverting Input of Op. Amplifier 1
18	PWDN0	Power Down 0 logic input
20	DGND	Digital GND
21, 22	-Vs	Negative Supply Voltage
23	BIAS	Bias Control pin
24	PWDN1	Power Down 1 logic input

Power Down Management

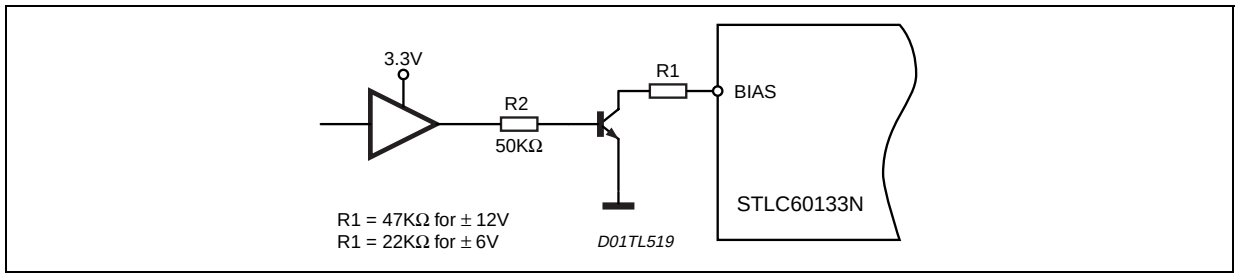
The STLC60133N provides several quiescent bias levels from full performance, to reduced bias (in three steps through PWDN0/1 pins) or to full OFF operation (through BIAS pin). According to the different XDSL application (both site CO and CPE), different bias levels can be chosen maintaining good MTPR performances. In the following table are shown the bias levels versus the PWDN values.

PWDN1	PWDN0	Bias Level
1	1	100%
1	0	80%
0	1	60%
0	0	40% (low Zout but not OFF)
X	X	Full OFF (High Zout via 75uA pulled out of BIAS pin)

The bias level is programmed by the TTL logic level applied to the PWDN pins. The DGND pin is the logic ground reference for the PWDN pins. For normal operation the BIAS pin shall be left open.

The BIAS control pin can be used to adjust the internal biasing and thus the quiescent current. By pulling out a current of 0µA to 50µA, the quiescent current can be adjusted from 100% (full ON) to a full OFF condition. However, considering the internal parameter spread to full shutdown the STLC60133N is recommended to pull down a 75µA current from the BIAS pin. In the following figure is shown an implementation of a complete amplifier shutdown. To partially reduce the internal biasing also the PWDN pins can be used.

Figure 2. Logic drive of bias pin for complete Amplifier Shutdown.



THERMAL SHUTDOWN

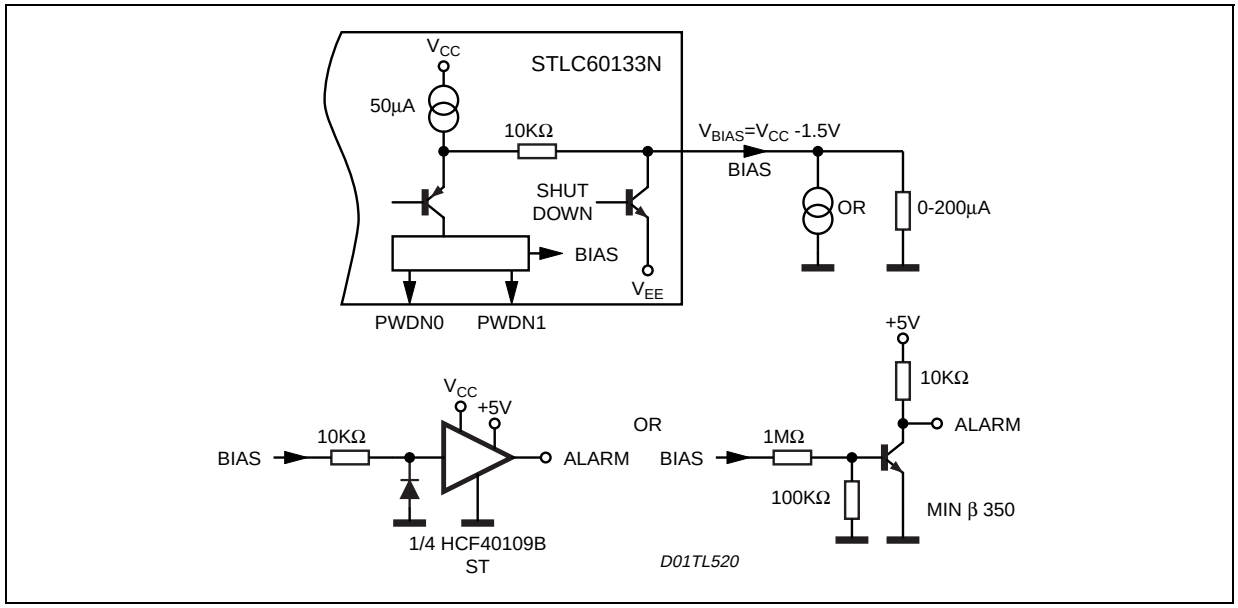
A thermal protection is embedded in the STLC60133N. In case of thermal overload the device is shut down at 160°C and returns to normal operation when the temperature becomes lower than 145°C.

During the thermal shutdown the voltage at the BIAS pin goes to the DGND rail; when the device returns to the normal operation the voltage at the BIAS pin goes to the positive rail. In this condition the BIAS pin can be used as thermal overload indicator.

MAXIMUM POWER DISSIPATION

Maximum Junction Temperature allowed for proper device operation is T_j = 140°C. A Typical Thermal Resistance Junction to ambient of 29°C/W can be obtained mounting the device on a 4 layer board whithin 10 square inches of copper and having the exposed pad contacting a proper copper area . It shall be noted that the exposed pad of the device is electrically not connected to the V_{SS} negative supply.

Figure 3. Shutdown and alarm circuit



ELECTRICAL CHARACTERISTCS

Test Conditions: (V_{CC} = ±12V , Tamb = 0 to 70°C , Single amplifier in normal condition (PWDN0 = 1, PWDN1 = 1), unless otherwise specified). The limits listed below are guaranted in the above temperature range (0-70°C) by specific testing at different temperature or by product characterisation.

TRANSMISSION PATH

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SR	Slew Rate	G = 6, Vout = 2Vpp		400		V/us
GBW	Gain Bandwidth	G = 6, Vout = 2Vpp, f = 5MHz	90	140		MHz
THD	Single ended Distortion	G = 6, f = 1MHz, Vout = 12Vpp, Rl = 16.5Ω Rl = 100Ω		 -47 -52		dBc
DTHD	Differential THD (2)	G = 6, f = 1MHz, Vout = 24Vpp, Rl = 33Ω Rl = 100Ω	 -50 -55			dBc
IMD	Single ended IMD	G = 6, Vout = 3Vp each tone, f = 500KHz, Δf = 10KHz Rl = 16.5Ω Rl = 100Ω		 -70 -75		dBc
DIMD	Differential IMD (2)	G = 6, Vout = 6Vp each tone, f = 500KHz, Δf = 10KHz Rl = 33Ω Rl = 100Ω	 -66 -72			dBc
IB	Input Biasing			5		μA
OZ	Output Impedance	PWDN0 = PWDN1 = 0; f = 1MHz			2	Ω
VN	Voltage Noise (RTI)	f = 30KHz		4	10	nV/$\sqrt{Hz}$
IOV	Input Offset Voltage				6	mV
ICMR	Input Common Mode Voltage Range	f = 1 MHz	-1		+1	V
CMRR	Common Mode Rejection Ratio	f = 1 MHz, Vin = 100mV		40		dB
OVS	Output Voltage Swing	Single ended, Rl = 100Ω, G = 6	-11		+11	V
LOC	Linear Output Current	Single ended, Rl = 10Ω, G = 6	400	600		mA
SCC	Short Circuit Current (1)	Single ended		1000	1400	mA
QC	Quiescent Current	PWDN1, PWDN0 = 1,1 PWDN1, PWDN0 = 1,0 PWDN1, PWDN0 = 0,1 PWDN1, PWDN0 = 0,0		3.5 2.9 2.2 1.6		mA/Amp
SC	Shutdown Current	75μA out of Bias pin		1.5	2.0	mA/Amp
PSRR	Power Supply Rejection ratio	f = 500kHz, V = 100mV	30			dB
BIASV	Bias Pin Voltage		10	10.5		V
DCG	DC Gain			80		dB
HIZ	Output impedance in Shut Down mode		500			kΩ

Notes: 1. The output stage of the STLC60133N is designed for maximum load current capability. As a result, shorting the output to common can cause the STLC60133N to source or sink 1.4A.
2. Guaranteed by product characterization.

ELECTRICAL CHARACTERISTICS

Test conditions (V_{CC} = ±6V, T_{amb} = 0 to 70°C ,Single amplifier in normal condition (PWDN0 = 1, PWDN1 = 1), unless otherwise specified.) The limits listed below are guaranted in the above temperature range by (0-70°C) specific testing at different temperature or by product characterisation.

TRANSMISSION PATH

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SR	Slew Rate	G = 6, Vout = 2Vpp		400		V/us
GBW	Gain Bandwidth	G = 6, Vout = 2Vpp, f = 5MHz	90	140		MHz
THD	Single Ended Distortion	G = 6, f = 1MHz, Vout = 6Vpp, Rl = 25Ω Rl = 100Ω		 -46 -51		dBc
DTHD	Differential THD (2)	G = 6, f = 1MHz, Vout = 12Vpp, Rl = 25Ω Rl = 100Ω	 -50 -55			dBc
IMD	Single Ended IMD	G = 6, Vout = 1.5Vp each tone, f = 500KHz, Δf = 10KHz Rl = 25Ω Rl = 100Ω		 -76 -81		dBc
DIMD	Differential IMD (2)	G = 6, Vout = 3Vp each tone, f = 500KHz, Δf = 10KHz Rl = 25Ω Rl = 100Ω	 -77 -82			dBc
IB	Input Biasing			5		µA
VN	Voltage Noise (RTI)	f = 30KHz		4	10	$nV/\sqrt{Hz}$
IOV	Input Offset Voltage				6	mV
ICMR	Input Common Mode Voltage Range	f = 1 MHz	-1		+1	V
CMRR	Common Mode Rejection Ratio	f = 1 MHz, Vin = 100mV		40		dB
OVS	Output Voltage Swing	Single ended, Rl = 100Ω, G = 6	-5		+5	V
LOC	Linear Output Current	Single ended, Rl = 10Ω, G = 6	300	420		mA
SCC	Short Circuit Current (1)	Single ended,		1000	1400	mA
QC	Quiescent Current	PWDN1, PWDN0 = 1,1 PWDN1, PWDN0 = 1,0 PWDN1, PWDN0 = 0,1 PWDN1, PWDN0 = 0,0		2.9 2.4 1.8 1.4		mA/Amp
SC	Shutdown Current	75µA out of Bias pin		1.5	2.0	mA/Amp
PSRR	Power Supply Rejection ratio	f = 500kHz, V = 100mV	30	40		dB
BIASV	Bias Pin Voltage		4	4.5		V
DCG	DC Gain			80		dB
HIZ	Output impedance in Shut Down mode		500			kΩ

Notes: 1. The output stage of the STLC60133N is designed for maximum load current capability. As a result, shorting the output to common can cause the STLC60133N to source or sink 1.4A.
2. Guaranteed by product characterization.

DIGITAL INTERFACE (PWDN0, PWDN1, Vcc = ±12 V or ±6 V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{il}	Input low voltage		0		0.8	V
V_{ih}	Input high voltage		2.2		5.5	V

THERMAL PROTECTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{hsd}	Thermal shut down threshold			160		°C
T_{hist}	Thermal detector histeresys			15		°C

Figure 4. Single ended Test Circuit G = 6

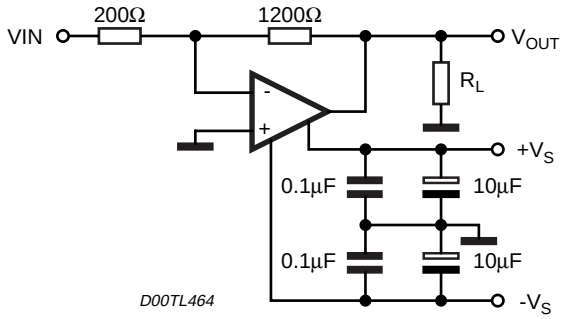
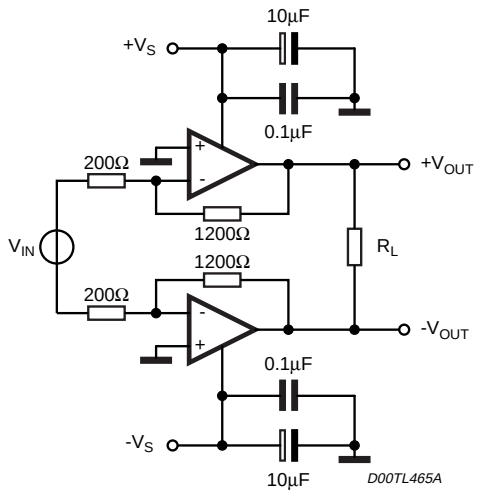


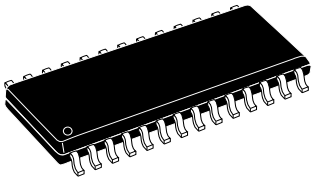
Figure 5. Differential Test Circuit G = 6



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.0
A1			0.15			0.006
A2	0.8	1.0	1.05	0.031	0.039	0.041
b	0.19		0.3	0.007		0.012
c	0.09		0.2	0.003		0.008
D (*)	9.6	9.7	9.8	0.377	0.382	0.385
D1		5.5			0.216	
E	6.2	6.4	6.6	0.244	0.252	0.260
E1 (*)	4.3	4.4	4.5	0.169	0.173	0.177
E2		3.0			0.118	
e		0.65			0.026	
L	0.45	0.6	0.75	0.018	0.024	0.029
L1		1.0			0.039	
k	0° (min), 8° (max)					
aaa		0.1			0.004	

(*) Dimensions D and E1 does not include mold flash or protusions. Mold flash or protusions shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



HTSSOP28 (Exposed Pad)