



STP12NM50 - STP12NM50FP STB12NM50 - STB12NM50-1

N-CHANNEL 550V @ T_{jmax} -0.30 Ω - 12A TO-220/FP/D²/I²PAK
Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STB12NM50	550 V	< 0.35 Ω	12 A
STB12NM50-1	550 V	< 0.35 Ω	12 A
STP12NM50	550 V	< 0.35 Ω	12 A
STP12NM50FP	550 V	< 0.35 Ω	12 A

- TYPICAL R_{DS(on)} = 0.30 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- LOW INPUT CAPACITANCE AND GATE CHARGE
- 100% AVALANCHE TESTED
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB12NM50T4	B12NM50	D ² PAK	TAPE & REEL
STB12NM50-1	B12NM50	I ² PAK	TUBE
STP12NM50	P12NM50	TO-220	TUBE
STP12NM50FP	P12NM50FP	TO-220FP	TUBE

Figure 1: Package

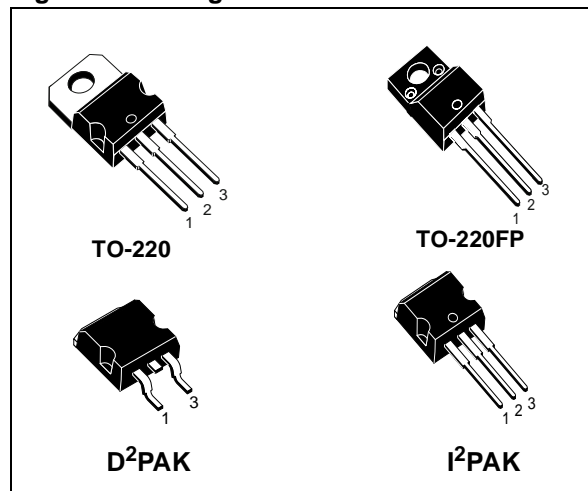


Figure 2: Internal Schematic Diagram

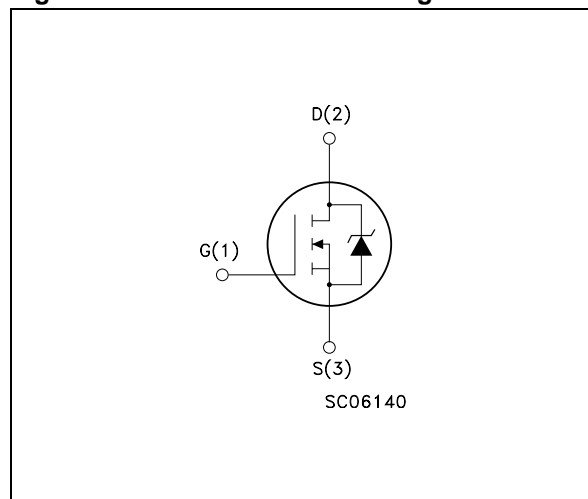


Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		STB12NM50 STB12NM50 STP12NM50	STP12NM50FP	
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	12	12 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	7.5	7.5 (*)	A
I _{DM} (●)	Drain Current (pulsed)	48	48 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	160	35	W
	Derating Factor	1.28	0.28	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)	--	2500	V
dv/dt (1)	Peak Diode Recovery voltage slope	15		V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-65 to 150 -65 to 150		°C °C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 12A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220/ D ² PAK / I ² PAK	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	0.78	3.57	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	6	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	400	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)
Table 6: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30 V			± 100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 6 A		0.30	0.35	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 6\text{ A}$		5.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1000 180 25		pF pF pF
$C_{oss\ eq}$ (3).	Equivalent Output Capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }400\text{ V}$		90		pF
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 250\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17)		20 10		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 20)		28 8 18	39	nC nC nC
R_g	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.6		Ω

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				12 48	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 18)		270 2.23 16.5		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150^\circ\text{C}$ (see Figure 18)		340 3 18		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3) $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area For TO-220/D²PAK/I²PAK

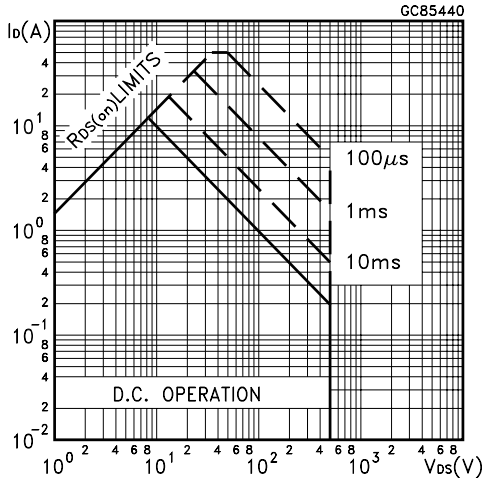


Figure 4: Safe Operating Area For TO-220FP

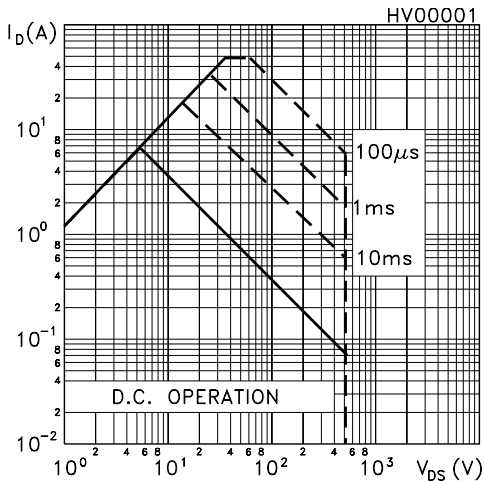


Figure 5: Output Characteristics

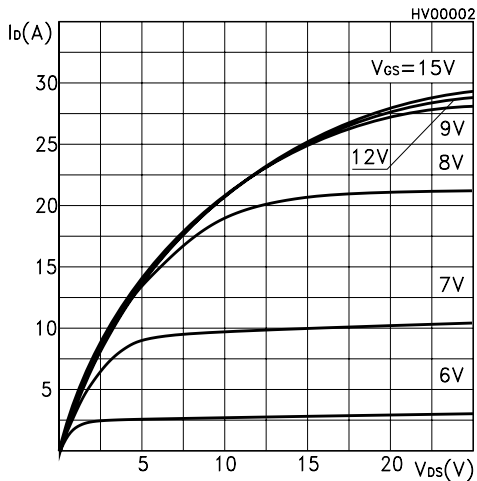


Figure 6: Thermal Impedance TO-220/D²PAK/I²PAK

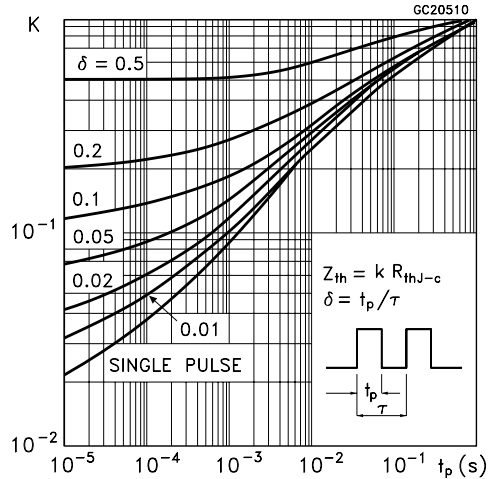


Figure 7: Thermal Impedance For TO-220FP

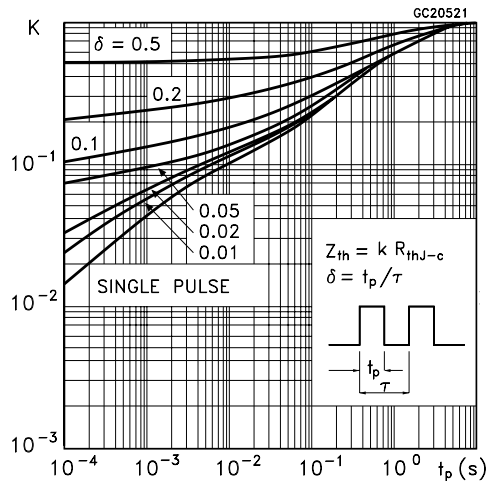


Figure 8: Transfer Characteristics

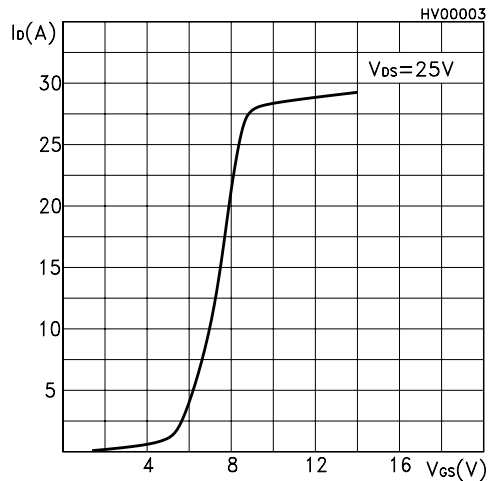


Figure 9: Transconductance

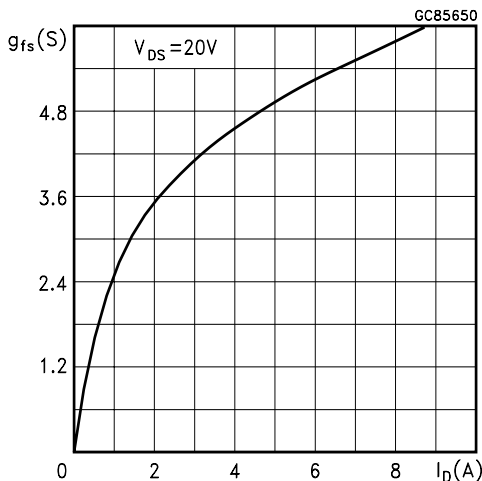


Figure 10: Gate Charge vs Gate-source Voltage

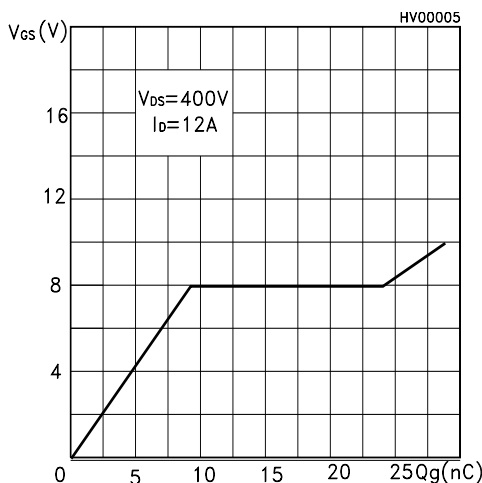


Figure 11: Normalized Gate Threshold Voltage vs Temperature

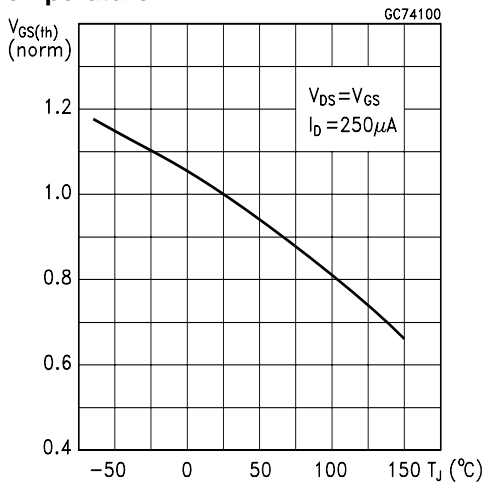


Figure 12: Static Drain-Source On Resistance

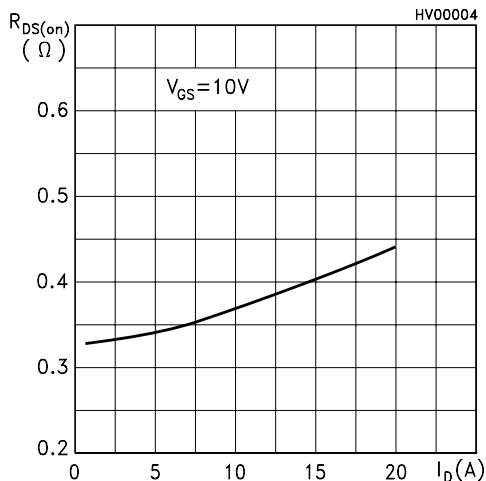


Figure 13: Capacitance Variations

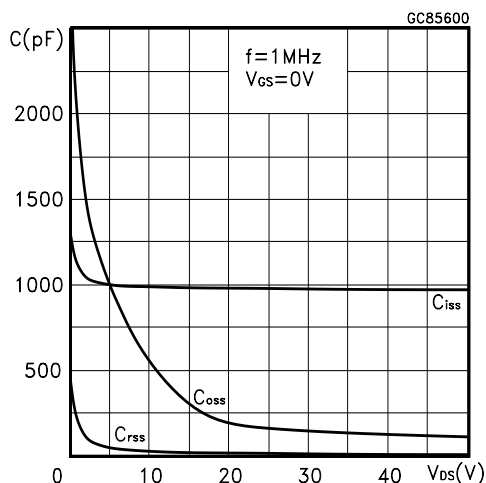


Figure 14: Normalized On Resistance vs Temperature

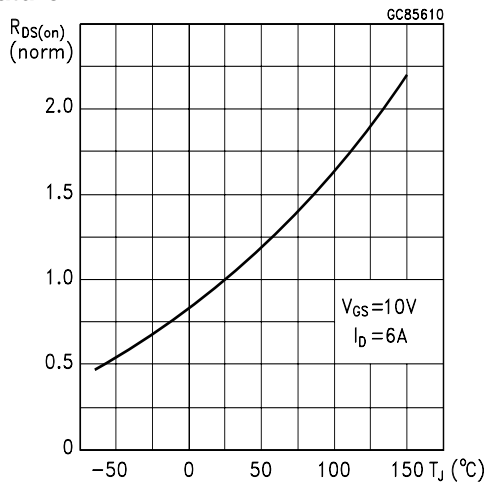


Figure 15: Source-Drain Forward Characteristics

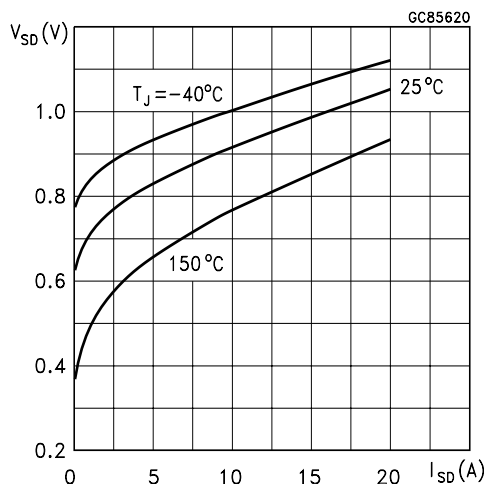


Figure 16: Unclamped Inductive Load Test Circuit

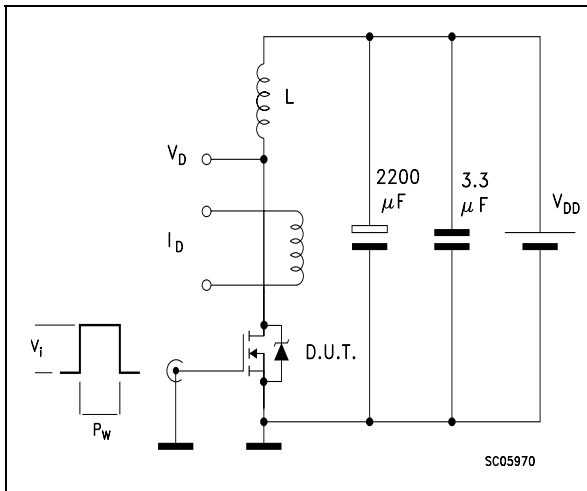


Figure 17: Switching Times Test Circuit For Resistive Load

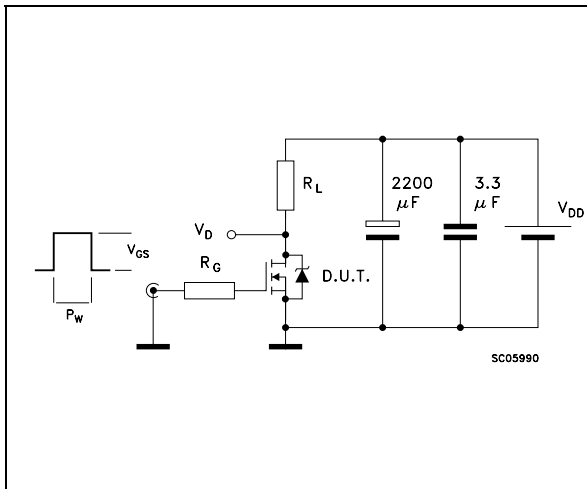


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

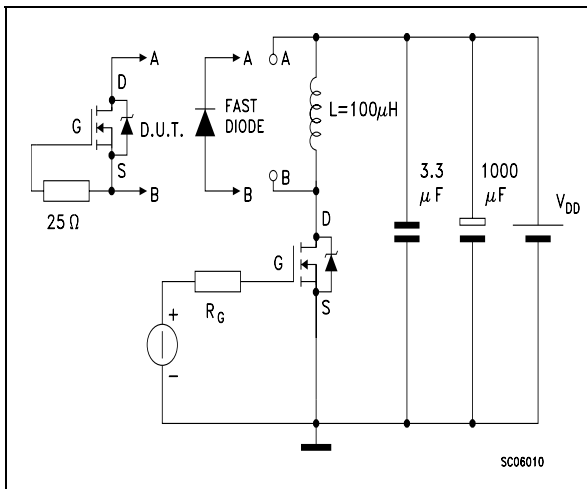


Figure 19: Unclamped Inductive Waferform

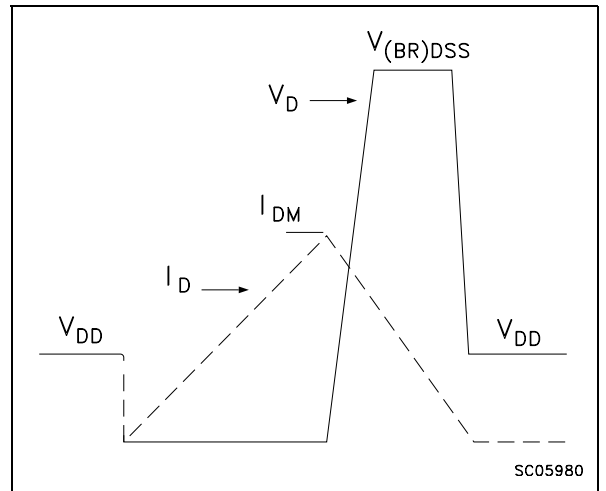
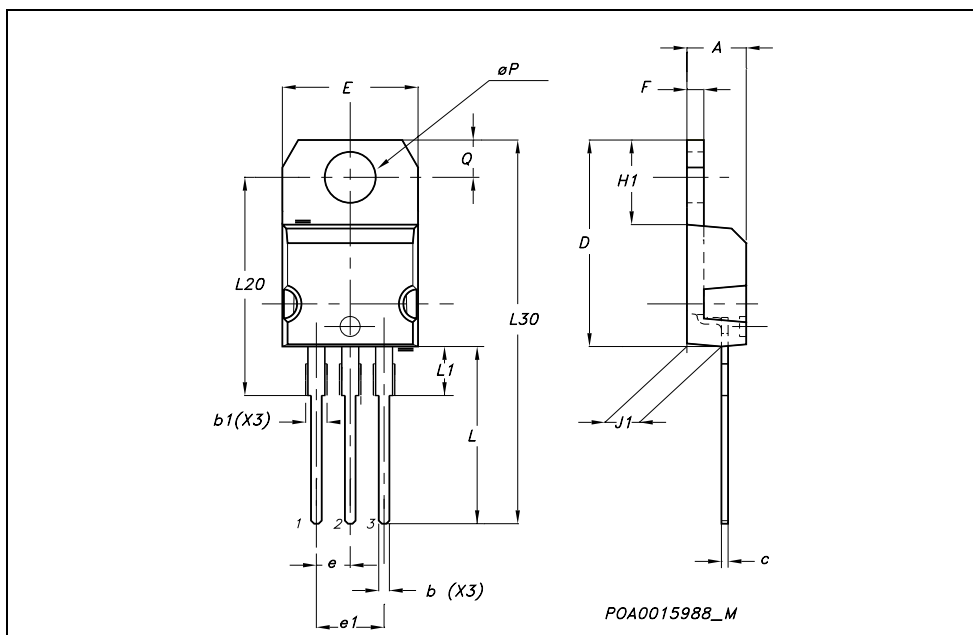


Figure 20: Gate Charge Test Circuit



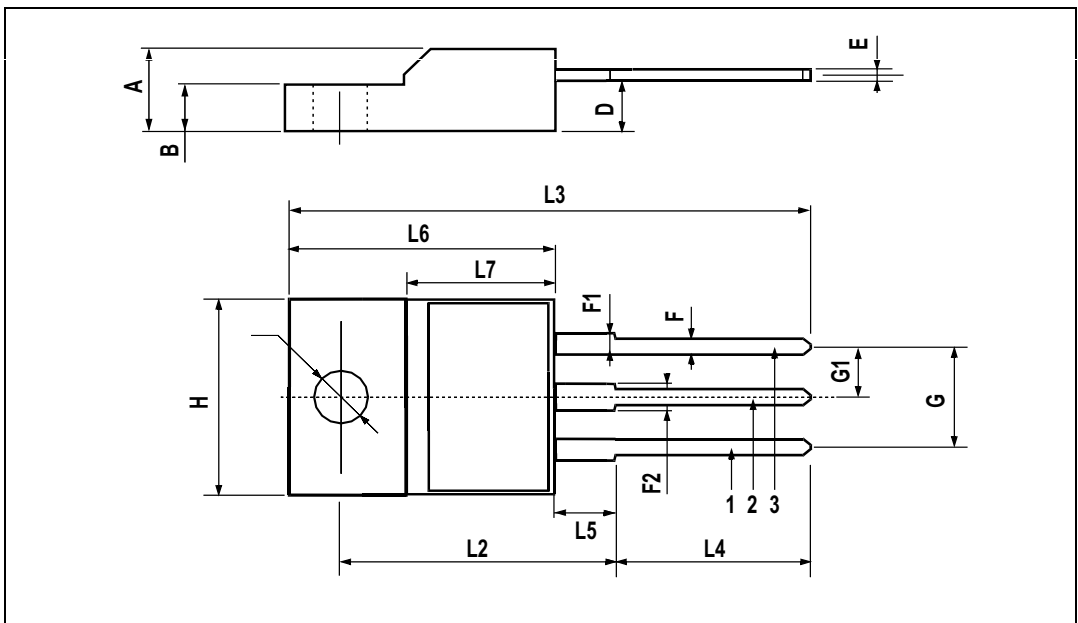
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



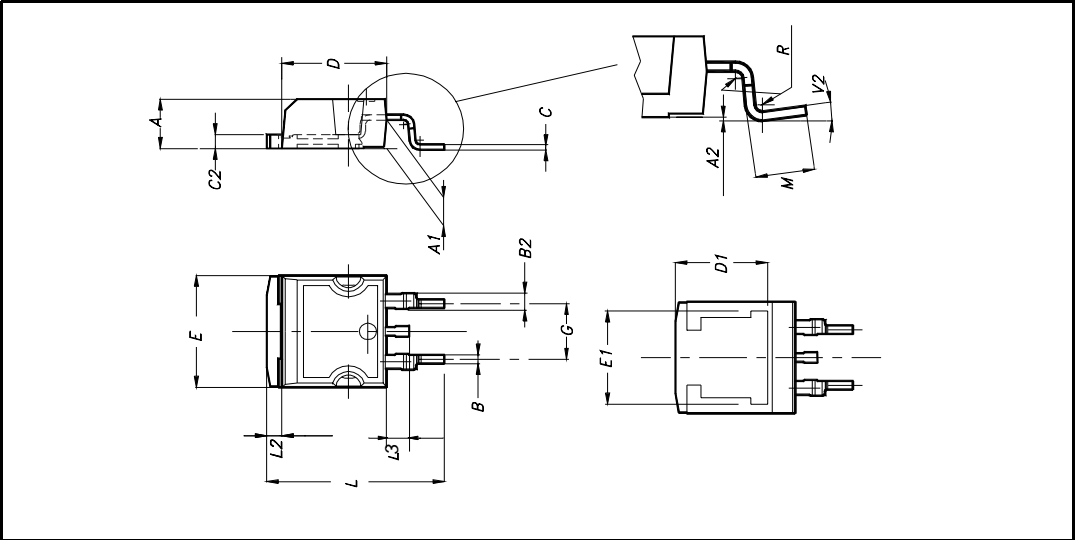
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



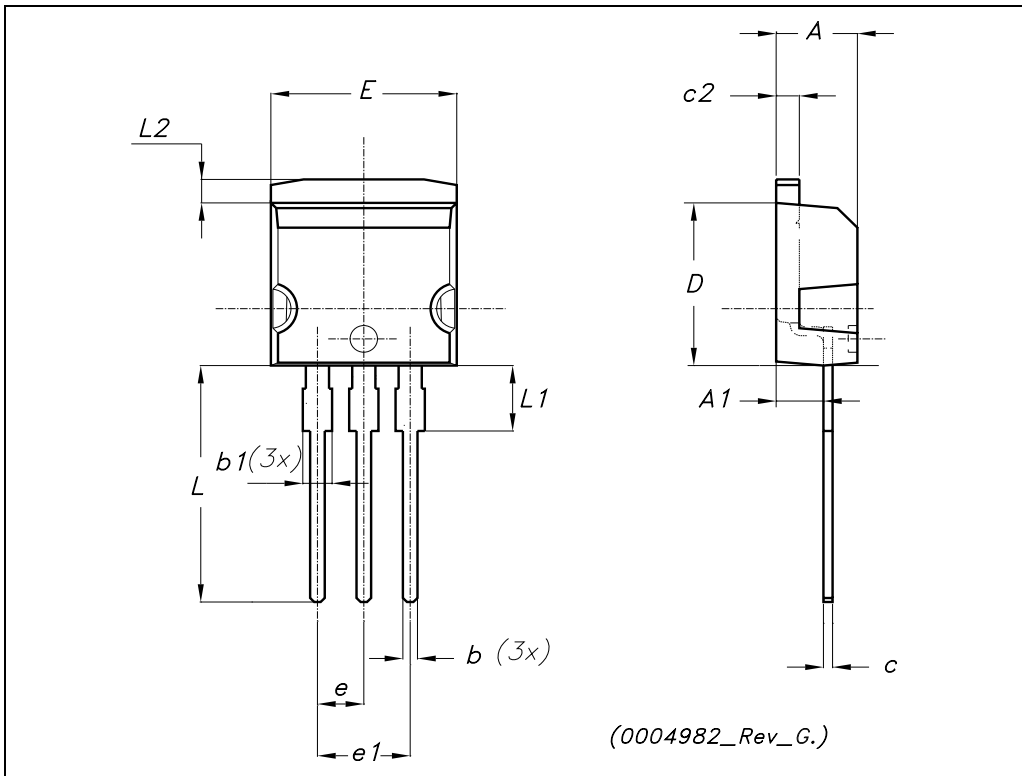
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

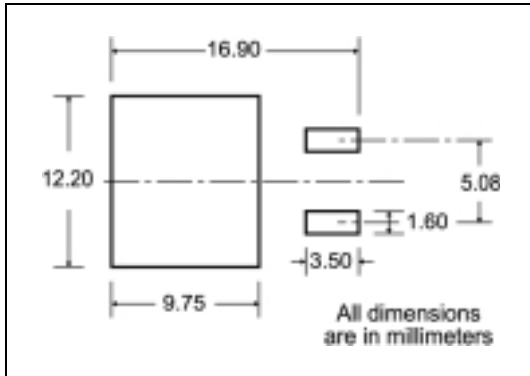


TO-262 (I²PAK) MECHANICAL DATA

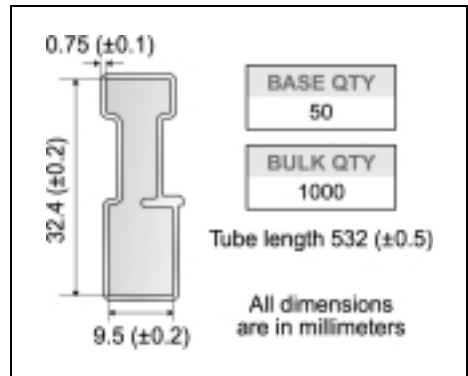
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

Diagram showing the tape mechanical data. It includes a top view of the tape with dimensions A, B, C, D, and G. A 40 mm min. access hole is shown at the slot location. The tape slot in the core has a 2.5 mm min. width. The full radius is also indicated.

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

Diagram showing the reel mechanical data. It includes a top view of the reel with dimensions A₀, B₀, D, D₁, E, F, K₀, P₀, P₁, P₂, R, T, and W. The top cover tape is shown with a 10-pitch cumulative tolerance on tape of ±0.2 mm. The center line of the cavity is also indicated. The user direction of feed and feed direction are shown. The bending radius is R min.

* on sales type

Table 9: Revision History

Date	Revision	Description of Changes
27-Sep-2004	1	Complete version
09-Mar-2005	2	New Stylesheet

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