



STP9NK60ZFD - STP9NK60ZFDFP STB9NK60ZFD

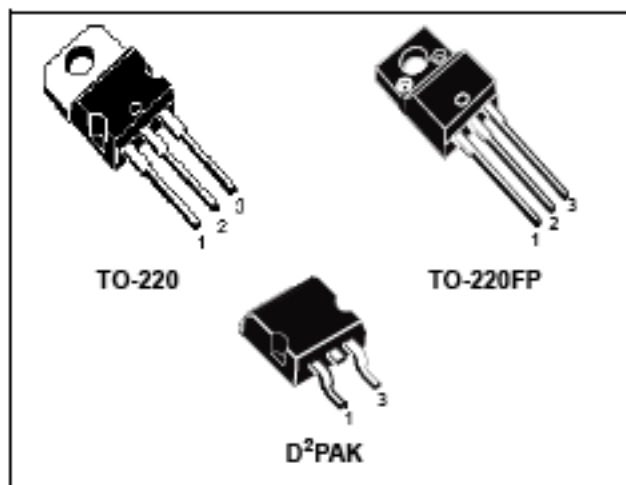
N-CHANNEL 600V - 0.85Ω - 7A TO-220/TO-220FP/D²PAK

Fast Diode SuperMESH™ MOSFET

TARGET DATA

TYPE	V _{DS}	R _{DS(on)}	I _D	P _w
STP9NK60ZFD	600 V	< 0.85 Ω	7 A	104 W
STP9NK60ZFDFP	600 V	< 0.85 Ω	7 A	32 W
STB9NK60ZFD	600 V	< 0.85 Ω	7 A	104 W

- TYPICAL R_{DS(on)} = 0.85 Ω
- HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY
- FAST INTERNAL RECOVERY DIODE



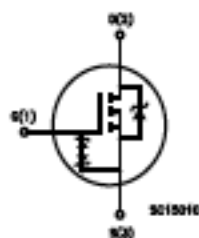
DESCRIPTION

The Fast SuperMESH™ series associates all advantages of reduced on-resistance, zener gate protection and very good dv/dt capability with a Fast body-drain recovery diode. Such series complements the "FDmesh™" Advanced Technology.

APPLICATIONS

- HID BALLAST
- ZVS PHASE-SHIFT FULL BRIDGE CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP9NK60ZFD	P9NK60ZFD	TO-220	TUBE
STP9NK60ZFDFP	P9NK60ZFDFP	TO-220FP	TUBE
STB9NK60ZFDT4	B9NK60ZFD	D ² PAK	TAPE & REEL

ABSOLUTE MAXIM

Symbol		Value		Unit
		TO-220 / D ² PAK	TO-220FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	7	7 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	4.3	4.3 (*)	A
I _{DM} (*)	Drain Current (pulsed)	28	28 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	104	32	W
	Derating Factor	0.83	0.26	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C=100pF, R=1.5KΩ)	4000		V
dw/dt (1)	Peak Diode Recovery voltage slope	TBD		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _J T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		°C

(*) Pulse width limited by safe operating area

(1) I_{SD} ≤ 7A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{DSR(ESS)}, T_J ≤ T_{JMAX}

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 D ² PAK	TO-220FP	Unit
R _{thj-case}	Thermal Resistance Junction-case Max	1.02	3.85	°C/W
R _{thj-pcb}	Thermal Resistance Junction-pcb Max (When mounted on minimum Footprint)	30		°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _J max)	7	A
E _{AS}	Single Pulse Avalanche Energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	280	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} = ± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED)
ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = \text{mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 3.5\text{A}$		0.85	0.95	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15\text{V}$, $I_D = 3.5\text{A}$		5.3		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		1110 135 30		pF pF pF
$C_{oss\text{ eq. (3)}}$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 480\text{V}$		72		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 300\text{V}$, $I_D = 3.5\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Resistive Load see, Figure 3)		19 17		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480\text{V}$, $I_D = 7\text{A}$, $V_{GS} = 10\text{V}$		38 7 21	53	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 300\text{V}$, $I_D = 3.5\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Resistive Load see, Figure 3)		43 15		ns ns
$t_{r(volt)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 480\text{V}$, $I_D = 7\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		11 8 20		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				7 28	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 7\text{A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 30\text{V}$, $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		150 TBD TBD		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Fig. 1: Unclamped Inductive Load Test Circuit

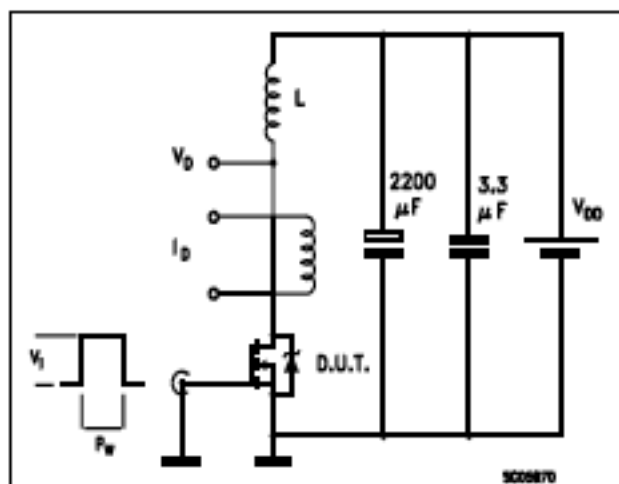


Fig. 2: Unclamped Inductive Waveform

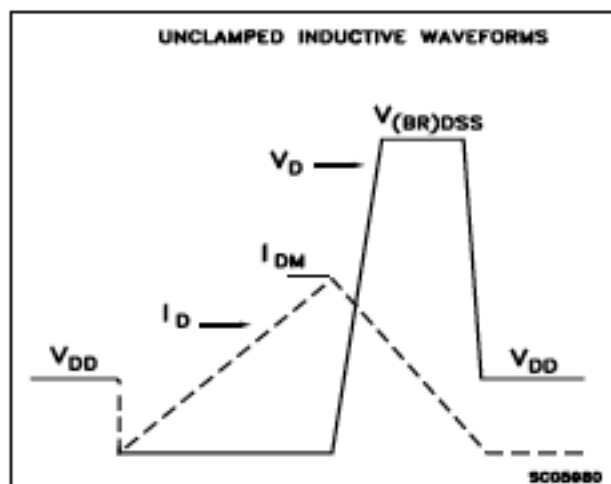


Fig. 3: Switching Times Test Circuit For Resistive Load

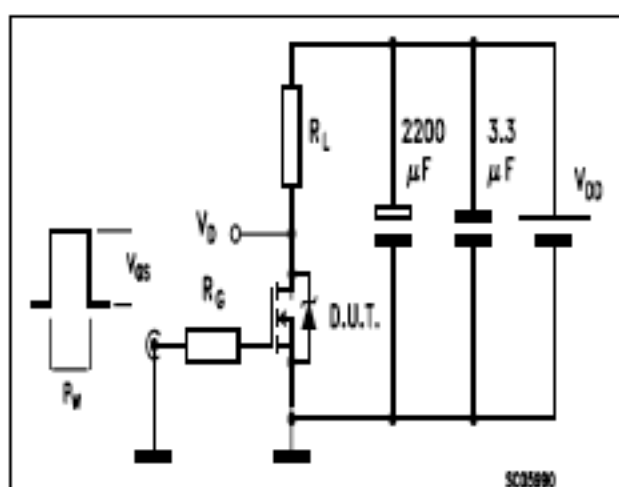


Fig. 4: Gate Charge test Circuit

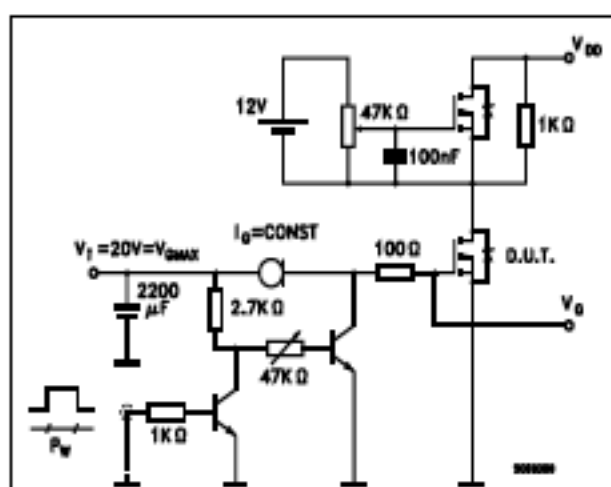
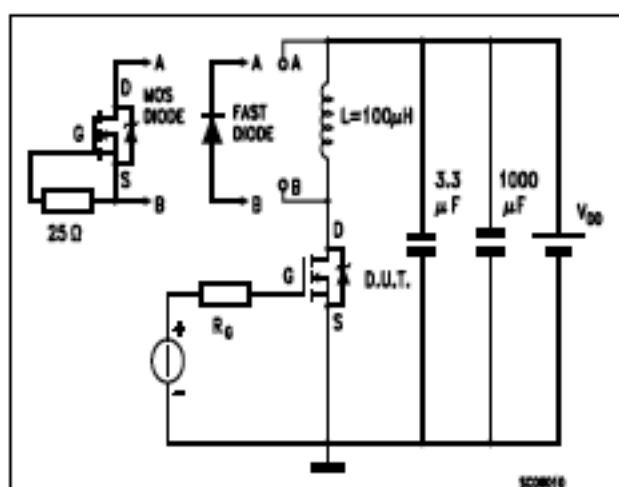
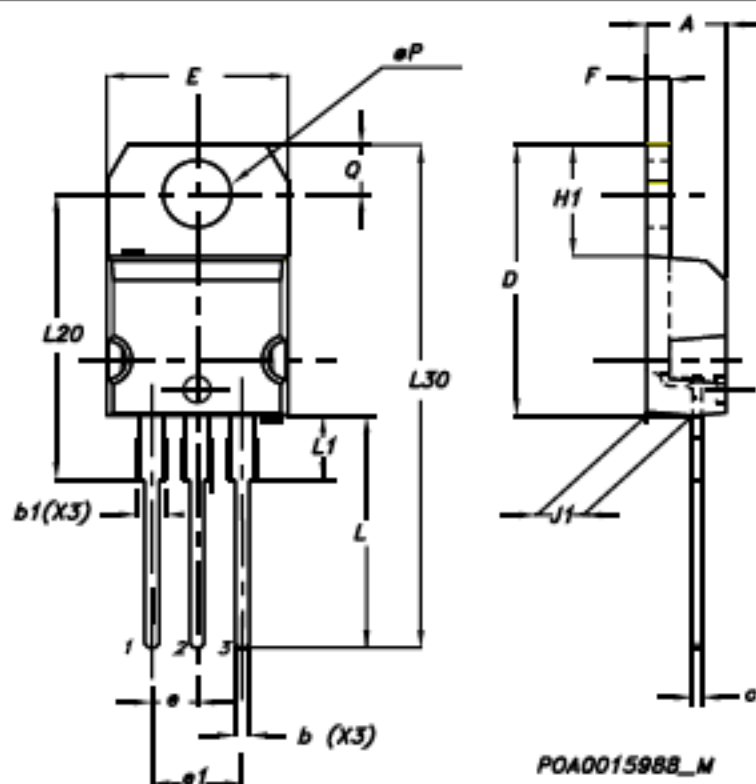


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



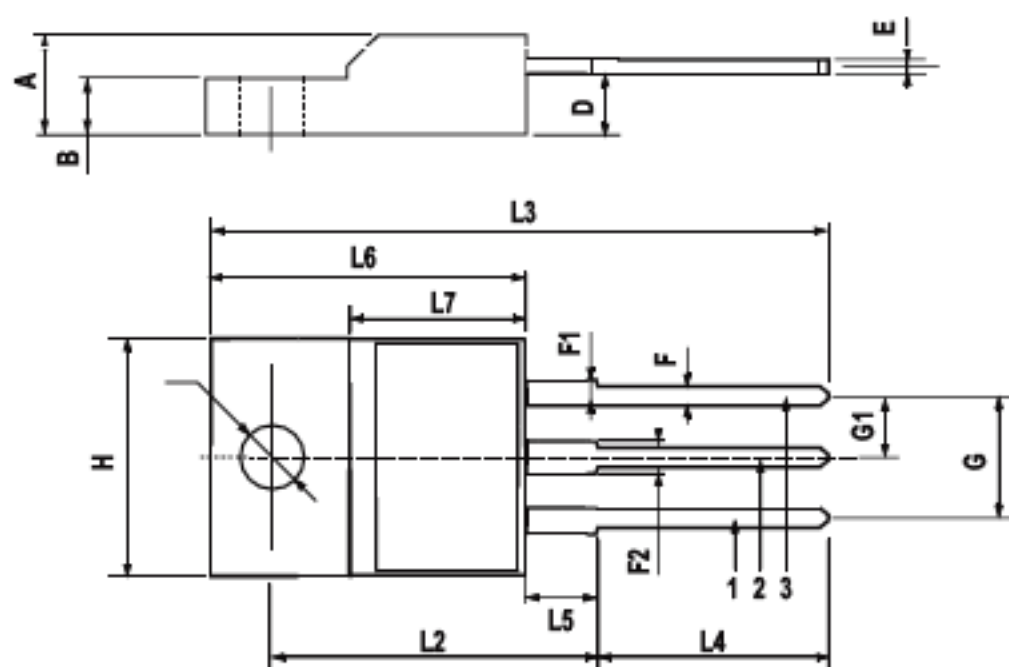
TO-220 MECHANICAL DATA

DIM.	mm.			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



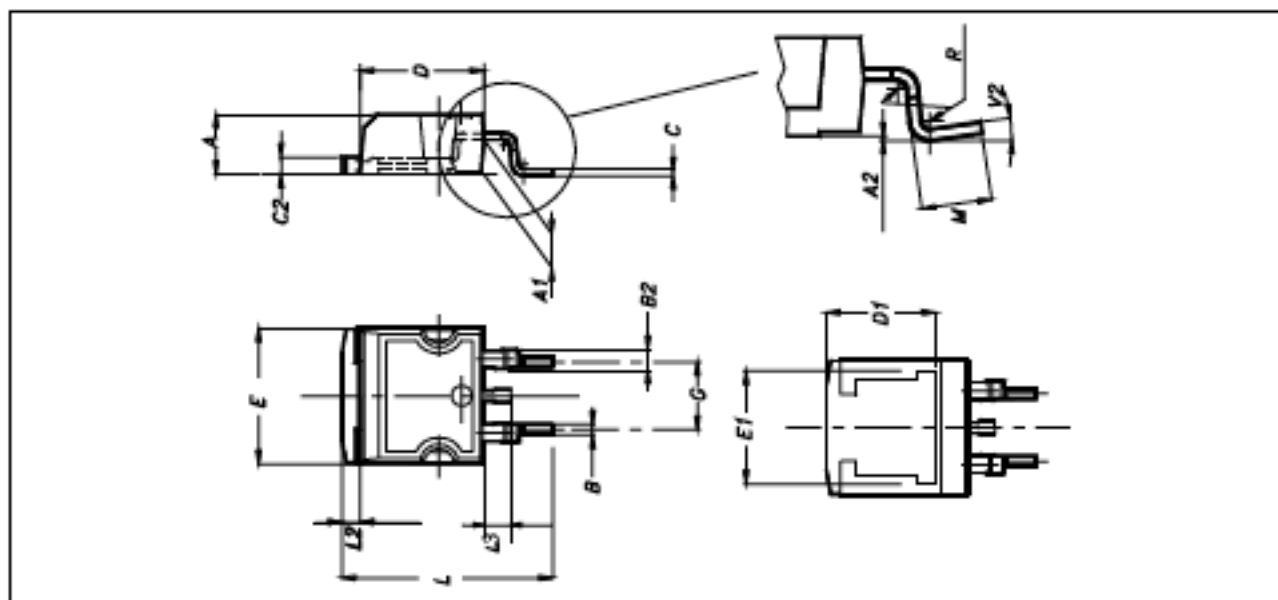
TO-220FP MECHANICAL DATA

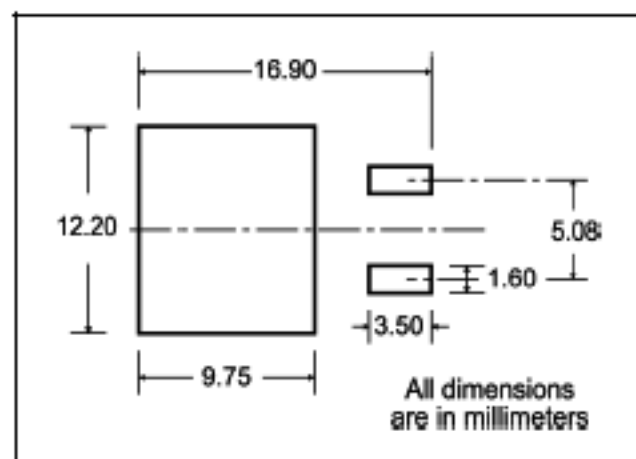
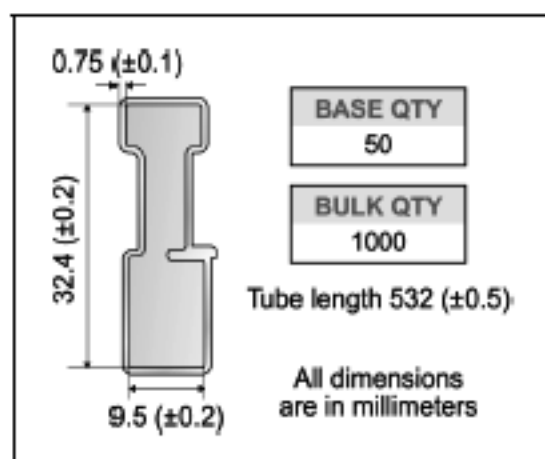
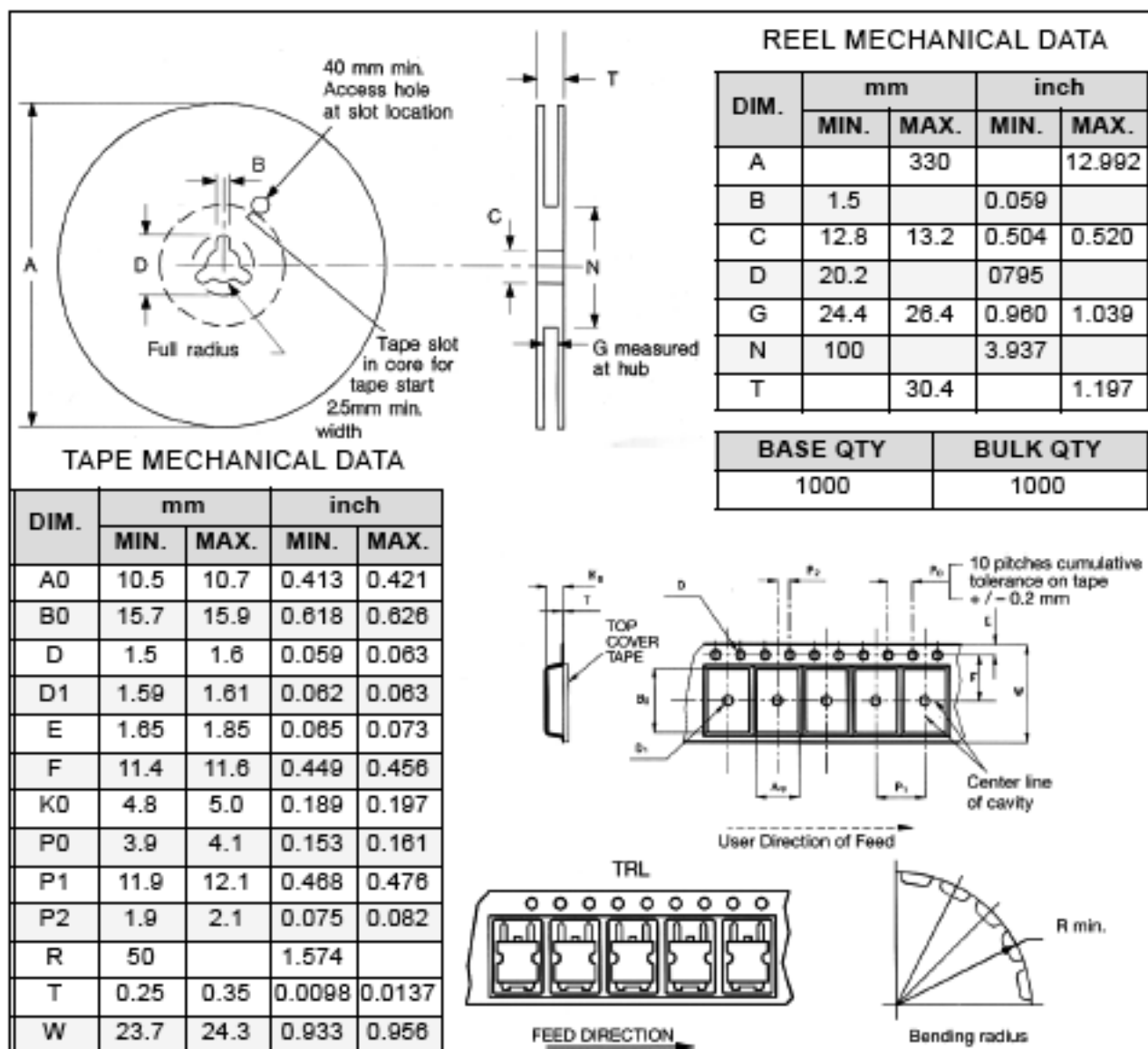
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.38	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



D²PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>