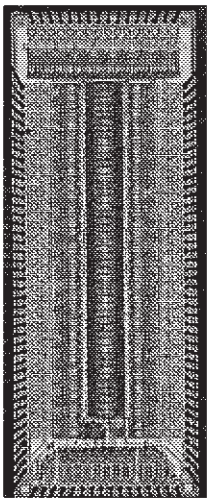
STV7618

PLASMA DISPLAY PANEL DATA DRIVER

FEATURES

- 96 Outputs Plasma Display Driver
- 90V Absolute Maximum Rating
- 3.3V / 5V Compatible Logic
- -40 / 30 mA Source / Sink Output MOS
- 3 or 6 Bit Data Bus (40 MHz)
- BCD Process
- Packaging Adapted to Customer's Request (DICE, COB, COF, TAB).



Die

ORDER CODE: STV7618/WAF (1)
(1)Unsawn tested wafer

DESCRIPTION

STV7618 is a data driver for Plasma Display Panel (PDP) designed in the ST proprietary BCD high voltage technology. Using a 3 or 6 bit wide data bus, it can control 96 high current & high voltage outputs. The STV7618 is supplied with a separated 70V power output supply and a 5V logic supply. All command inputs are CMOS and 3.3V logic levels compatible.

Version 4.2

Revision follow-up

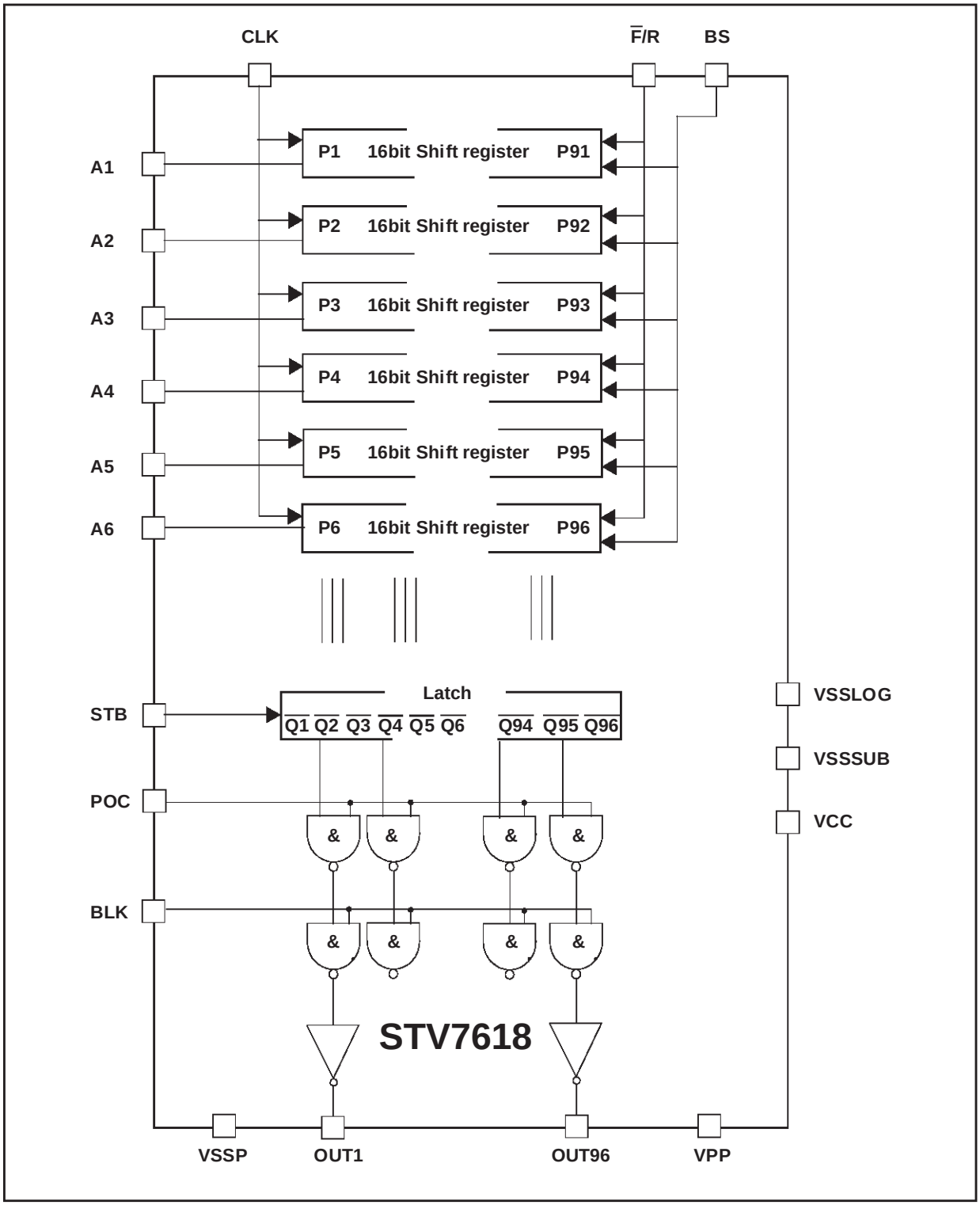
Target specification

05/2000	version 1.1
	document creation
05/2000	version 1.2
	few changes in figures
07/2000	version 1.3
	addition of pads dimensions/coordinates, few changes in figures and electrical characteristics
02/2001	version 1.4
	TBD mentions replaced with values for Vouthl and Voutlh

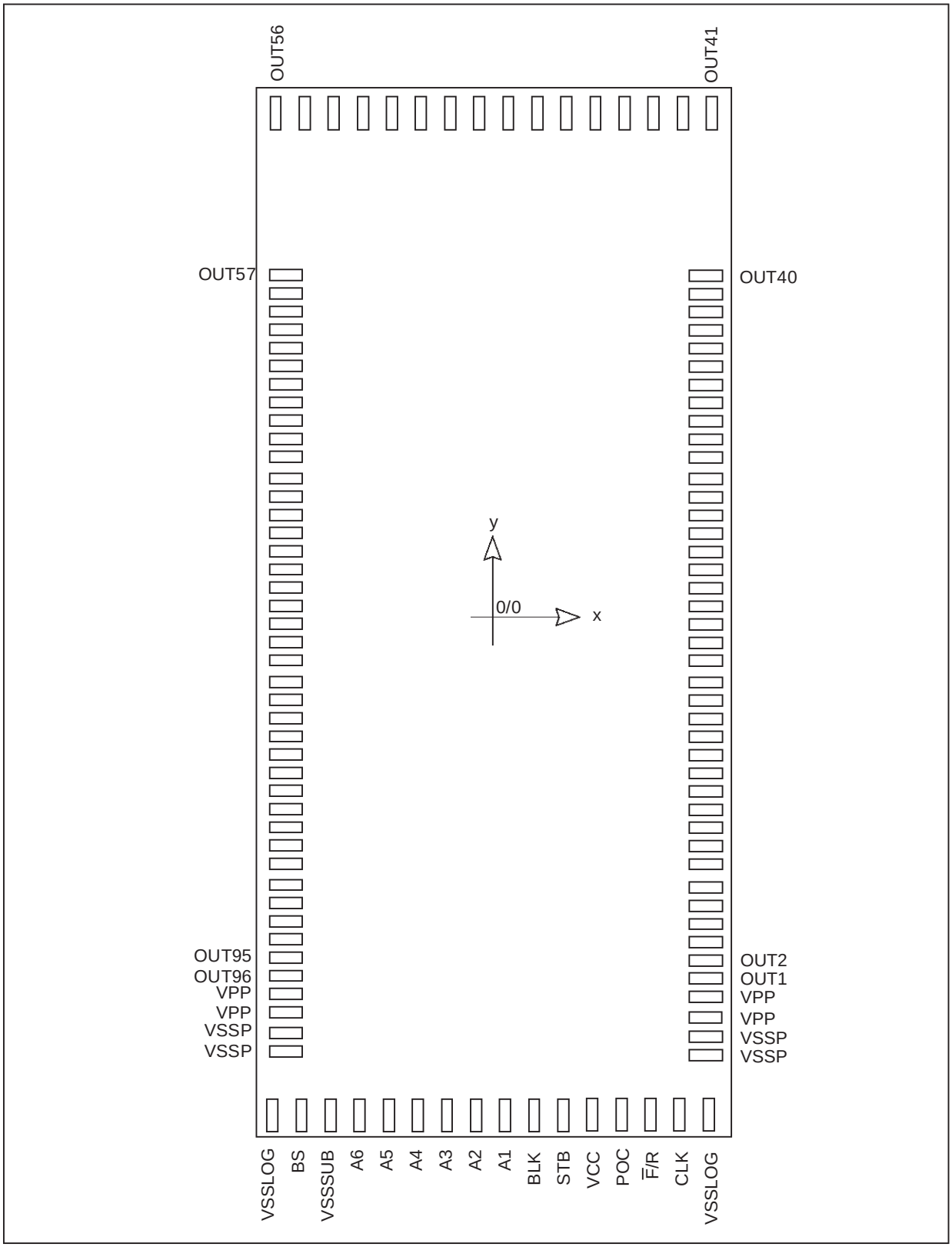
Datasheet

06/2001	version 4.0
	general update
10/2001	version 4.1
	addition of die photo in cover page new pads dimensions
04/2002	version 4.2
	Cover page features related to output diode current deleted New values for Source/sink output MOS: -40/30mA Absolute maximum ratings I_{POUT} values -150/150mA added definition and values for I_{DOUT} -200/300mA Addition of note 4: Transient current. Spike current duration inferior to 300ns. Tested wafer disclaimer chapter added

1 - BLOCK DIAGRAM



2 - DIE PIN OUT / DIE DESCRIPTION



3 - PADS DIMENSIONS (in μm)/ PADS POSITIONS

The reference is the centre of the die (x=0, y=0)

TOP SIDE from left to right

Name	Centre: X	Centre: Y	Size:x	SIze: y
OUT56	-774.478	2700.96	75	90
OUT55	-671.288	2700.96	75	90
OUT54	-568.098	2700.96	75	90
OUT53	-464.907	2700.96	75	90
OUT52	-361.718	2700.96	75	90
OUT51	-258.528	2700.96	75	90
OUT50	-155.338	2700.96	75	90
OUT49	-52.147	2700.96	75	90
OUT48	51.042	2700.96	75	90
OUT47	154.232	2700.96	75	90
OUT46	257.422	2700.96	75	90
OUT45	360.612	2700.96	75	90
OUT44	463.802	2700.96	75	90
OUT43	566.992	2700.96	75	90
OUT42	670.267	2700.96	75	90
OUT41	773.458	2700.96	75	90

BOTTOM SIDE from right to left

Name	Centre: X	Centre:Y	Size:x	SIze: y
VSSLOG	773.542	-2701.045	75	90
CLK	670.352	-2701.045	75	90
F/R	567.162	-2701.045	75	90
POC	463.972	-2701.045	75	90
VCC	360.782	-2701.045	75	90
STB	258.442	-2701.045	75	90
BLK	155.252	-2701.045	75	90
A1	52.062	-2701.045	75	90
A2	-51.128	-2701.045	75	90
A3	-154.318	-2701.045	75	90
A4	-257.508	-2701.045	75	90
A5	-360.698	-2701.045	75	90
A6	-463.888	-2701.045	75	90
VSSSUB	-567.078	-2701.045	75	90
BS	-670.352	-2701.045	75	90
VSSLOG	-773.542	-2701.045	75	90

RIGHT SIDE from top to bottom

Name	Centre: X	Centre:Y	Size:x	SIze: y
OUT40	892.670	1950.792	90	75
OUT39	892.670	1847.602	90	75
OUT38	892.670	1744.327	90	75
OUT37	892.670	1641.138	90	75
OUT36	892.670	1537.947	90	75
OUT35	892.670	1434.757	90	75
OUT34	892.670	1331.568	90	75
OUT33	892.670	1228.378	90	75
OUT32	892.670	1125.188	90	75
OUT31	892.670	1021.998	90	75
OUT30	892.670	918.807	90	75
OUT29	892.670	815.618	90	75
OUT28	892.670	712.428	90	75
OUT27	892.670	609.238	90	75
OUT26	892.670	506.048	90	75
OUT25	892.670	402.857	90	75
OUT24	892.670	299.668	90	75
OUT23	892.670	196.478	90	75
OUT22	892.670	93.288	90	75
OUT21	892.670	-9.902	90	75
OUT20	892.670	-113.092	90	75
OUT19	892.670	-216.282	90	75
OUT18	892.670	-319.472	90	75
OUT17	892.670	-422.662	90	75
OUT16	892.670	-525.852	90	75
OUT15	892.670	-629.042	90	75
OUT14	892.670	-732.232	90	75
OUT13	892.670	-835.422	90	75
OUT12	892.670	-938.612	90	75
OUT11	892.670	-1041.802	90	75
OUT10	892.670	-1144.992	90	75
OUT9	892.670	-1248.182	90	75
OUT8	892.670	-1351.372	90	75
OUT7	892.670	-1454.562	90	75
OUT6	892.670	-1557.752	90	75
OUT5	892.670	-1660.942	90	75
OUT4	892.670	-1764.132	90	75
OUT3	892.670	-1867.322	90	75
OUT2	892.670	-1970.512	90	75
OUT1	892.670	-2073.702	90	75

LEFT SIDE from bottom to top

Name	Centre: X	Centre:Y	Size:x	SIze: y
VSSP	-892.670	-2486.208	90	75
VSSP	-892.670	-2383.018	90	75
VPP	-892.670	-2279.912	90	75
VPP	-892.670	-2176.722	90	75
OUT96	-892.670	-2073.702	90	75
OUT95	-892.670	-1970.512	90	75
OUT94	-892.670	-1867.322	90	75
OUT93	-892.670	-1764.132	90	75
OUT92	-892.670	-1660.942	90	75
OUT91	-892.670	-1557.752	90	75
OUT90	-892.670	-1454.562	90	75
OUT89	-892.670	-1351.372	90	75
OUT88	-892.670	-1248.182	90	75
OUT87	-892.670	-1144.992	90	75
OUT86	-892.670	-1041.802	90	75
OUT85	-892.670	-938.612	90	75
OUT84	-892.670	-835.422	90	75
OUT83	-892.670	-732.232	90	75
OUT82	-892.670	-629.042	90	75
OUT81	-892.670	-525.852	90	75
OUT80	-892.670	-422.662	90	75
OUT79	-892.670	-319.472	90	75
OUT78	-892.670	-216.282	90	75
OUT77	-892.670	-113.092	90	75
OUT76	-892.670	-9.902	90	75
OUT75	-892.670	93.288	90	75
OUT74	-892.670	196.478	90	75
OUT73	-892.670	299.668	90	75
OUT72	-892.670	402.857	90	75
OUT71	-892.670	506.048	90	75
OUT70	-892.670	609.238	90	75
OUT69	-892.670	712.428	90	75
OUT68	-892.670	815.618	90	75
OUT67	-892.670	918.807	90	75
OUT66	-892.670	1021.998	90	75
OUT65	-892.670	1125.188	90	75
OUT64	-892.670	1228.378	90	75
OUT63	-892.670	1331.568	90	75
OUT62	-892.670	1434.757	90	75
OUT61	-892.670	1537.947	90	75

Name	Centre: X	Centre:Y	Size:x	SIze: y
VPP	892.670	-2176.722	90	75
VPP	892.670	-2279.912	90	75
VSSP	892.670	-2383.018	90	75
VSSP	892.670	-2486.208	90	75

Name	Centre: X	Centre:Y	Size:x	SIze: y
OUT60	-892.670	1641.138	90	75
OUT59	-892.670	1744.327	90	75
OUT58	-892.670	1847.602	90	75
OUT57	-892.670	1950.792	90	75

4 - DATA BUS CONFIGURATION

BS	$\overline{F}$/R	Input	Data Shift														
			CLK	**01**	**02**	**03**	**04**	**05**	**06**	**...**	**11**	**12**	**13**	**14**	**15**	**16**	
L	L	A1	Out	01	07	13	19	25	31		61	67	73	79	85	91	Forward Shift
		A2	Out	02	08	14	20	26	32		62	68	74	80	86	92	
		A3	Out	03	09	15	21	27	33		63	69	75	81	87	93	
		A4	Out	04	10	16	22	28	34		64	70	76	82	88	94	
		A5	Out	05	11	17	23	29	35		65	71	77	83	89	95	
		A6	Out	06	12	18	24	30	36		66	72	78	84	90	96	
L	H	A1	Out	91	85	79	73	67	61		31	25	19	13	07	01	Reverse Shift
		A2	Out	92	86	80	74	68	62		32	26	20	14	08	02	
		A3	Out	93	87	81	75	69	63		33	27	21	15	09	03	
		A4	Out	94	88	82	76	70	64		34	28	22	16	10	04	
		A5	Out	95	89	83	77	71	65		35	29	23	17	11	05	
		A6	Out	96	90	84	78	72	66		36	30	24	18	12	06	
			CLK	**01**	**02**	**03**	**04**	**05**	**06**	**...**	**27**	**28**	**29**	**30**	**31**	**32**	
H	L	A1	Out	01	04	07	10	13	16		79	82	85	88	91	94	Forward
		A2	Out	02	05	08	11	14	17		80	83	86	89	92	95	
		A3	Out	03	06	09	12	15	18		81	84	87	90	93	96	
H	H	A1	Out	94	91	88	85	82	79		16	13	10	07	04	01	Reverse
		A2	Out	95	92	89	86	83	80		17	14	11	08	05	02	
		A3	Out	96	93	90	87	84	81		18	15	12	09	06	03	

This table describes the position of the first data sampled by the first rising edge of the CLK signal. For the first configuration described in the above table, (BS = “L” and $\overline{F}$/R= “L”), data on A1 bus sampled by the 1st clock pulse is applied on Output1. After 16 clock pulses this data will be shifted to Output 91.

5 - PIN DESCRIPTION

Symbol	Function	Description
OUT(01-96)	Output	Power output
VSSP	Ground	Ground of power outputs
VPP	Supply	High voltage supply of power outputs
BLK	Input	Blanking input
POC	Input	Power output control input
$\overline{F}$/R	Input	Selection of shift direction
BS	Input	Selection of 3/6 bits shift register
VCC	Supply	5V logic supply
VSSLOG	Ground	Logic ground
VSSSUB	Ground	Substrate ground
CLK	Input	Clock of data shift register
STB	Input	Latch of data to outputs
IN (A1-A6)	Input	Shift register input for BS = “L”
IN (A1-A3)	Input	Shift register input for BS = “H”

6 - CIRCUIT DESCRIPTION

STV7618 includes all the logic and power circuits necessary to drive column electrodes of a Plasma Display Panel (P. D. P.). Binary values of each pixel of the displayed line are loaded into the shift register by a 6 bits wide (A1 - A6) or 3 bits wide (A1 - A3) data bus depending on the configuration of the BS input pin. Data is shifted at each low to high transition of the CLK clock.

The forward /reverse ($\overline{F}$/R) input is used to select the direction of the shift register.

The BS input is used to configure the shift register either in 3 x 32 bits or in 6 x 16 bits.

In case of a 3bits arrangement, A1, A2 and A3 data bus input pins are used. The 3 shift registers are loaded with 32 clock pulses. A4, A5 and A6 data bus input pins are at high impedance status.

The maximum frequency of the shift clock is 40MHz. This leads to an equivalent 240 MHz serial shift register for a 6 x 16 bits arrangement.

When the STB signal is Low, data are transferred from the shift register to the latch and power output stages.

All the output data are kept memorised and held in the latch stage when the latch input STB is pulled high.

Vsssub and Vsslog must be connected as close as possible to the logical reference ground of the application.

STV7618 is supplied with a 5 volt power supply. All the logic inputs can be driven either by 5V CMOS logic, or by 3.3V CMOS logic.

Table 1: Shift register truth table

	Input		Shift register function
BS	$\overline{F}$/R	CLK	Output Q
X	L	rise	Forward shift
X	L	H or L	Steady
X	H	rise	Reverse shift
X	H	H or L	Steady
H	X	X	3 bits shift register
L	X	X	6 bits shift register

Table 2: Power output truth table

Qn	STB	BLK	POC	Driver Output	Comments
X	X	L	X	all L	Output at low level
X	X	H	L	all H	Output at high level
X	H	H	H	Qn	Data latched
L	L	H	H	L	Data copied
H	L	H	H	H	Data copied

Qn+1 = A1, Qn+2 = A2, Qn+3 = A3, Qn+4 = A4, Qn+5 = A5, Qn+6 = A6, n = [0,6,12,18,...,90] and BS = “L”

7 - ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Logic supply range	-0.3, +7	V
Vpp	Driver supply range	-0.3, +90	V
Vin	Logic input voltage range	-0.3, Vcc+0.3	V
Ipout	Driver Output Current (Note 1) (Note 3) (Note 4)	-150 / +150	mA
Idout	Diode Output Current (Note 2) (Note 3) (Note 4)	-200 / +300	mA
Tjmax	Maximum junction temperature	125	°C
Tstg	Storage temperature range	-50, +150	°C
Toper	Operating ambient temperature	-20, +85	°C
Vout	Output power voltage range	-0.3, +90	V

Note 1 Through one power output (all power outputs).

Note 2 Through one power output for all power outputs (see Test Diagram) with Junction temperature lower or equal than $T_j$max.

Note 3 These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

Note 4 Transient current. Spike current duration inferior to 300ns.

ELECTRICAL CHARACTERISTICS

(Vcc = 5V, Vpp = 70V, Vssp = 0V, Vss = 0V, Tamb = 25°C, FCLK = 40 MHz, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
SUPPLY					
Vcc	Logic supply voltage	4.50	5	5.5	V
Icc	Logic supply current (Note 5)	-		100	µA
Iccl	Logic Dynamic Supply Current (FCLK=20Mhz) (Note 6)	-	20	-	mA
Icc	Logic Supply Current (Vih=2.0V)		500	750	µA
Vpp	Power output supply voltage - DC mode	15		70	V
Vpp	Power output supply voltage - AC mode	15		75	V
Ipph	Power output supply current (steady outputs)	-	-	100	µA
OUTPUT					
OUT1-OUT96					
Vpouth	Power output high level (voltage drop versus Vpp) @Ipouth = - 25mA and Vpp = 70V	-	11	16	V
Vpoutl	Power output low level @ Ipoutl = + 25mA	-	8	13	V
Vdouth	Output diode voltage drop @ Idouth = + 30mA (Note 7)	-	1	2	V
Vdoutl	Output diode voltage drop @ Idoutl = - 30mA (Note 7)	-2	-1	-	V
INPUT					
CLK, $\overline{F}$/R, STB, POC, BLK, BS, A1-A6					
Vih	Input high level	2.0	-	-	V
Vil	Input low level	-	-	0.9	V
Iih	High level input current (Vih >=2.0V)	-	-	5	µA
Iil	Low level input current (Vil = 0v)	-	-	5	µA
Cin	Input capacitance (Note 8)			15	pF

Note 5: Logic input levels compatible with 5V CMOS logic

Note 6: All data inputs are commuted at 10MHz

Note 7: see Figure 2.Test configuration page15

Note 8: This parameter is measured during ST's internal qualification which includes temperature characterization on standard and corner batches of the process. This parameter is not tested on the part.

AC TIMING REQUIREMENTS

(Vcc = 4.5v to 5.5v, T amb = -20 to +85°C, input signals max leading edge & trailing edge (tr,tf) = 5ns)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	Data clock period	25	-	-	ns
t_{WHCLK}	Duration of CLK pulse at high level	10	-	-	ns
t_{WLCLK}	Duration of CLK pulse at low level	10	-	-	ns
t_{SDAT}	Set-up time of data input before low to high clock transition	5	-	-	ns
t_{HDAT}	Hold-time of data input after low to high clock transition	5	-	-	ns
t_{HSTB}	Hold-time of STB after low to high clock transition	5	-	-	ns
t_{STB}	STB low level pulse duration	10	-	-	ns
t_{SSTB}	STB set-up time before CLK rise	5			ns

AC TIMING CHARACTERISTICS

(Vcc = 5V, Vpp = 70V, Vssp = 0V, Vsssub = 0V, Vsslog = 0V, Tamb = 25°C, FCLK = 40MHz,)
(Vilmax = 0.2Vcc, Vihmin = 0.8Vcc)

Symbol	Parameter	Min	Typ	Max	Unit
t_{PHL1} t_{PLH1}	Delay of power output change after CLK transition - high to low - low to high	 - -	 35 30	 100 100	 ns ns
t_{PHL2} t_{PLH2}	Delay of power output change after STB transition - high to low - low to high	 -	 30 25	 95 95	 ns ns
t_{PHL3} t_{PLH3}	Delay of power output change after BLK, POC transition - high to low - low to high	 -	 25 20	 90 90	 ns ns
$t_{R\ OUT}$	Power output rise time (Note 9)	50	90	200	ns
$t_{F\ OUT}$	Power output fall time (Note 9)	50	120	200	ns

Note 9: one output among 96, loading capacitor CL = 50pF, other outputs at low level

Figure 1. AC Characteristics Waveform

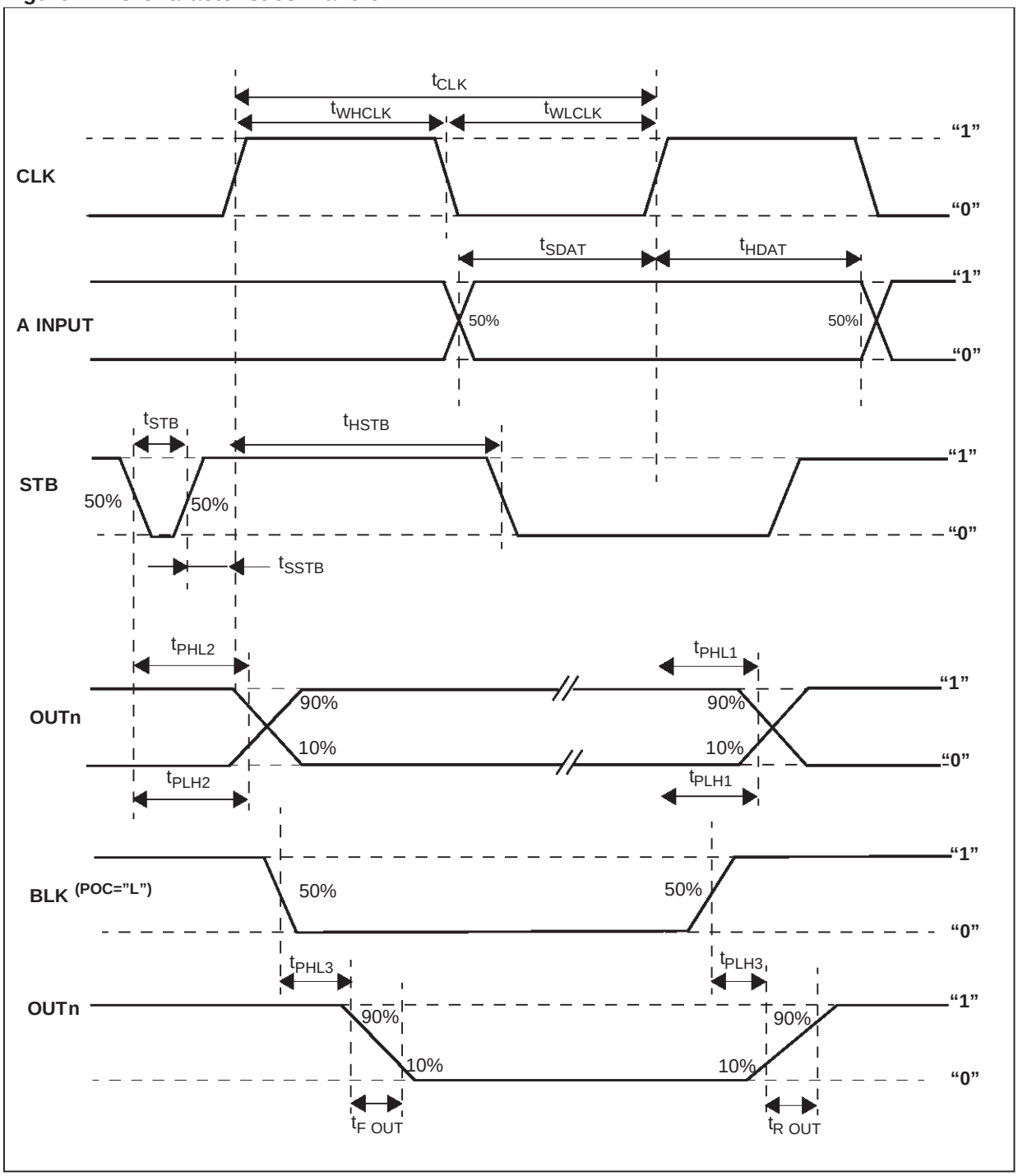
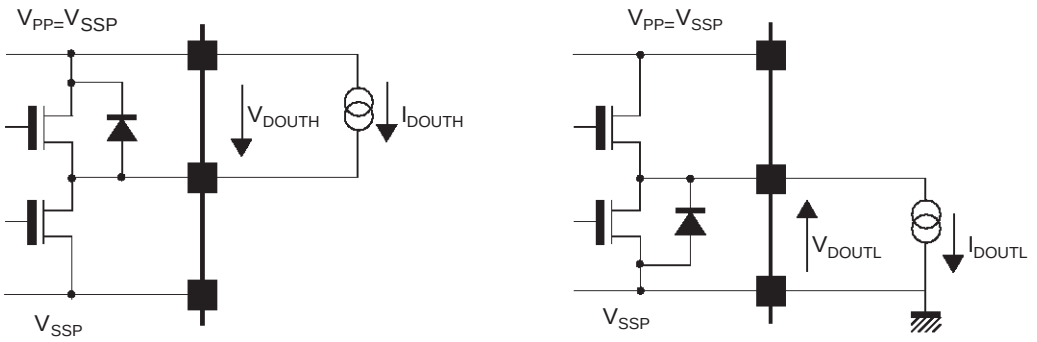


Figure 2. Test configuration



Output sinking current as positive value, sourcing current as negative value

8 - TESTED WAFER DISCLAIMER

All wafers are tested and guaranteed to comply with all datasheet limits up to the point of wafer sawing for a period of ninety (90) days from the delivery date.

We remind you that it is the customer's responsibility to test and qualify their application in which the die is used. ST Microelectronics is ready to support the customer when qualifying the product.

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