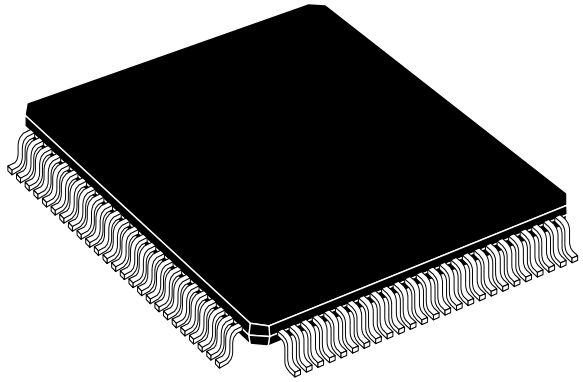
STV7619DU

Scan Driver for Plasma Display Panels

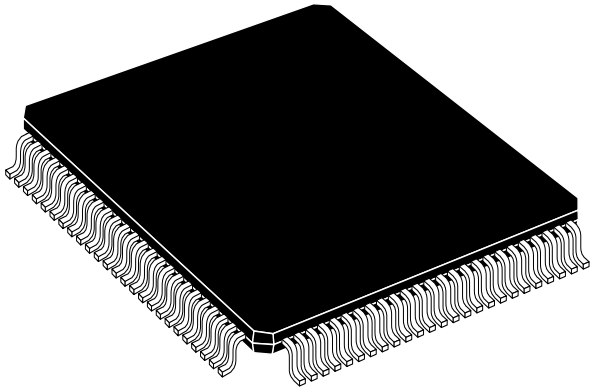
Main Features

- **64-output Scan Driver**
- **120 V Absolute Maximum Supply**
- **5 V Logic Supply**
- **Optional 12 V Supply for driving the output stage**
- **150mA/1A Source/Sink Output**
- **1 A Source/Sink Output Diode**
- **64-bit Bi-directional Shift Register (8 MHz)**
- **BCD Technology**
- **100-pin TQFP package with integrated heatsink**



TQFP100 (14 x 14 x 1.4 mm Slug-down)
(Thin Plastic Quad Flat Pack)

ORDER CODE: STV7619D



TQFP100 (14 x 14 x 1.4 mm)
(Thin Plastic Quad Flat Pack)

ORDER CODE: STV7619

Description

The STV7619 is a scan driver for plasma display panels (PDP) implemented in ST's proprietary BCD (Bi-polar CMOS DMOS) technology. Using a 64-bit cascadable 8 MHz shift register, it drives 64 high-current and high-voltage outputs.

By connecting several STV7619 devices in series, any vertical pixel definition can be performed. The STV7619 is supplied with separate 110V power output and 5 V logic supplies. The logic section of the output stage is supplied either externally by a 5V or 12V supply or internally by a charge pump cell. The choice of the supply value is related to the PDP size. All command inputs are CMOS compatible.

The STV7619 package is a 100-pin TQFP with integrated heatsink located on the bottom (STV7619D) of the package. It is also available without heatsink (STV7619).

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1 Pin Allocation and Descriptions

1.1 Pinout Diagrams

Figure 1: STV7619 and STV7619D (TQFP100)

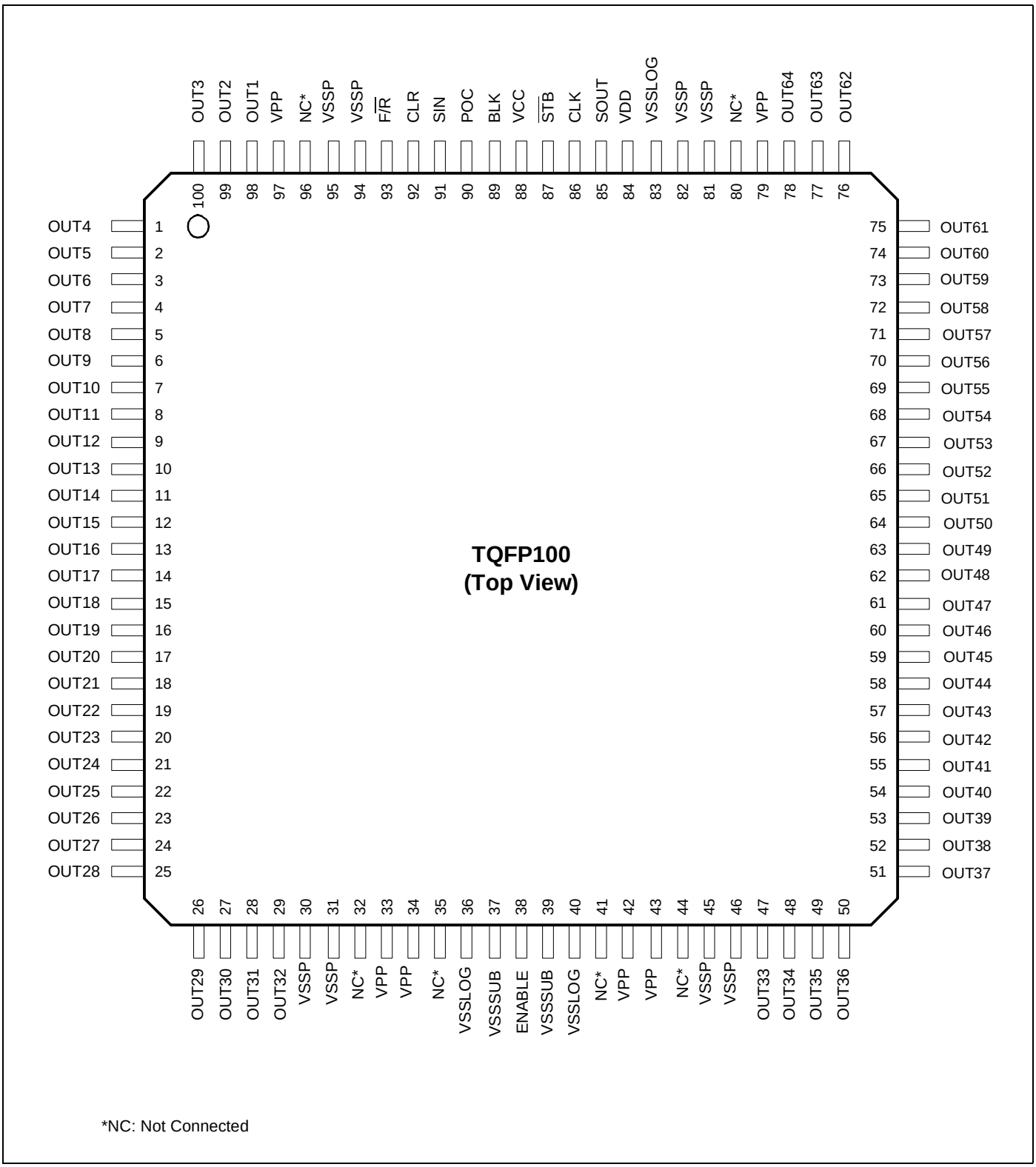


Table 1: Supply Pins

Pin No.	Pin Name	Pin Description
88	VCC	5V Logic Supply
84	VDD	5/12V Internal/External Logic Supply
33	VPP	High Voltage Supply for Power Outputs
34	VPP	High Voltage Supply for Power Outputs
42	VPP	High Voltage Supply for Power Outputs
43	VPP	High Voltage Supply for Power Outputs
79	VPP	High Voltage Supply for Power Outputs
97	VPP	High Voltage Supply for Power Outputs
36	VSSLOG	Logic Ground
40	VSSLOG	Logic Ground
83	VSSLOG	Logic Ground
30	VSSP	Ground for Power Outputs
31	VSSP	Ground for Power Outputs
45	VSSP	Ground for Power Outputs
46	VSSP	Ground for Power Outputs
81	VSSP	Ground for Power Outputs
82	VSSP	Ground for Power Outputs
94	VSSP	Ground for Power Outputs
95	VSSP	Ground for Power Outputs
37	VSSSUB	Substrate Ground
39	VSSSUB	Substrate Ground

Table 2: Shift Register and Input Pins

Pin No.	Pin Name	Pin Description
38	ENABLE	Enable Charge Pump mode
85	SOUT	Shift Register Data Output
86	CLK	Clock for Shift Register Data
87	$\overline{STB}$	Latch for Shift Register Data (Strobe Input)
89	BLK	Blanking Control for Power Outputs
90	POC	Polarity Output Control
91	SIN	Shift Register Data Input
92	CLR	Clear for Shift Register Data
93	F/$\overline{R}$	Foward/Reserve modes for selecting Shift Register

Table 3: Power Output Pins

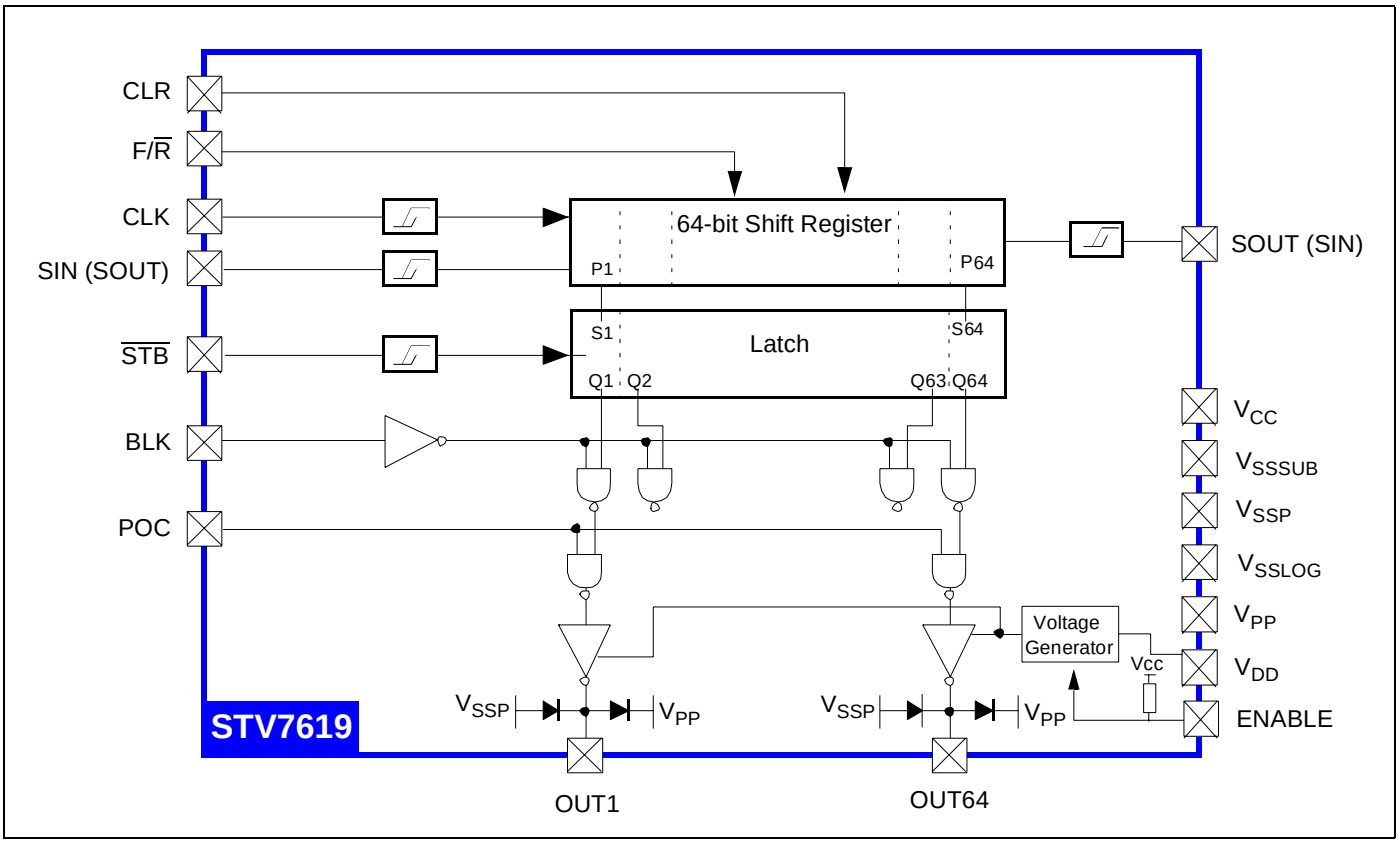
Pin No.	Pin Name	Pin Description	Pin No.	Pin Name	Pin Description
98	OUT1	Power Output 1	47	OUT33	Power Output 33
99	OUT2	Power Output 2	48	OUT34	Power Output 34
100	OUT3	Power Output 3	49	OUT35	Power Output 35
1	OUT4	Power Output 4	50	OUT36	Power Output 36
2	OUT5	Power Output 5	51	OUT37	Power Output 37
3	OUT6	Power Output 6	52	OUT38	Power Output 38
4	OUT7	Power Output 7	53	OUT39	Power Output 39
5	OUT8	Power Output 8	54	OUT40	Power Output 40
6	OUT9	Power Output 9	55	OUT41	Power Output 41
7	OUT10	Power Output 10	56	OUT42	Power Output 42
8	OUT11	Power Output 11	57	OUT43	Power Output 43
9	OUT12	Power Output 12	58	OUT44	Power Output 44
10	OUT13	Power Output 13	59	OUT45	Power Output 45
11	OUT14	Power Output 14	60	OUT46	Power Output 46
12	OUT15	Power Output 15	61	OUT47	Power Output 47
13	OUT16	Power Output 16	62	OUT48	Power Output 48
14	OUT17	Power Output 17	63	OUT49	Power Output 49
15	OUT18	Power Output 18	64	OUT50	Power Output 50
16	OUT19	Power Output 19	65	OUT51	Power Output 51
17	OUT20	Power Output 20	66	OUT52	Power Output 52
18	OUT21	Power Output 21	67	OUT53	Power Output 53
19	OUT22	Power Output 22	68	OUT54	Power Output 54
20	OUT23	Power Output 23	69	OUT55	Power Output 55
21	OUT24	Power Output 24	70	OUT56	Power Output 56
22	OUT25	Power Output 25	71	OUT57	Power Output 57
23	OUT26	Power Output 26	72	OUT58	Power Output 58
24	OUT27	Power Output 27	73	OUT59	Power Output 59
25	OUT28	Power Output 28	74	OUT60	Power Output 60
26	OUT29	Power Output 29	75	OUT61	Power Output 61
27	OUT30	Power Output 30	76	OUT62	Power Output 62
28	OUT31	Power Output 31	77	OUT63	Power Output 63
29	OUT32	Power Output 32	78	OUT64	Power Output 64

Table 4: Miscellaneous Pins

Pin No.	Pin Name	Pin Description
32	NC	Not connected
35	NC	Not connected
41	NC	Not connected
44	NC	Not connected
80	NC	Not connected
96	NC	Not connected

2 Circuit Description

Figure 2: Block Diagram



The STV7619 includes all the necessary logic and power circuits to drive the rows of electrodes of a plasma display panel (PDP). Data is shifted at each low to high transition of the (CLK) shift clock. After 64 shifts, the first bit presented at the serial input (SIN) is available at the serial output (SOUT). This output is used to cascade several drivers to perform any vertical resolution (Table 5). CLK, STB, SIN and SOUT inputs are Schmitt trigger inputs.

Table 5: Shift Register Truth Table

F/$\overline{R}$	CLK	SIN	SOUT	Comments
H	Rise	In	Out	Forward Shift
H	L or H	In	Out	Steady
L	Rise	Out	In	Reverse Shift
L	L or H	Out	In	Steady

In reverse mode (F/$\overline{R}$ = low), data is input on the SOUT pin and output on the SIN pin.

The clear signal (CLR) sets the shift register data to low.

Shift register outputs (P1, ... P64) are transferred from the shift register to the latch stage when the latch input (STB) is at low level.

All the data is kept memorized in the latch stage when the strobe input (STB) is pulled high.

Driver outputs can be simultaneously polarized at high or low level depending on the biasing of the POC input signal (Table 6).

Table 6: Output State Configuration

$\overline{STB}$	CLR	POC	BLK	Comments
*	*	L	*	All at low level
*	*	H	H	All at high level
L	H	H	L	All at high level
L	L	H	L	Inverted copy of input data
H	*	H	L	Inverted copy of latched data

The STV7619 integrates a charge pump cell to manage the current drive capabilities of the output sink transistor, as explained in Table 7. More details are given in Chapter 3.

Table 7: Voltage Generator Table

ENABLE	VDD	Output Performances
L	External Power Supply (V_{DD} = 5V)	Minimum Sink Current mode
	External Power Supply (V_{DD} = 12V)	Maximum Sink Current mode
H	Internal Power Supply (Charge Pump mode) V_{DD} connected to an external capacitance (C_{VDD} = 100nF (20V))	Medium Sink Current mode

3 Application Hints: Charge Pump Function

3.1 Power Supply

The STV7619 is designed to drive panels up to 42” with low voltage logic supplies (pins VCC and VDD). In this case, pin VDD must be connected to pin VCC. The driving of large panels (50”, 60”) requires a 100 nF capacitor connected between pin VDD and the ground. An internal charge pump provides a higher driving voltage for the low stage. If requested, higher performances are obtained when a 12V power supply is directly connected to pin VDD.

The logic supply management of the output stage mainly depends on the write current value of the plasma cells. The write current is related to the size of the PDP. The following figures illustrate the different possibilities to supply the STV7619 according to the current drive performances requested by the plasma panel.

Figure 3: External Power Supply (Small-size PDP)

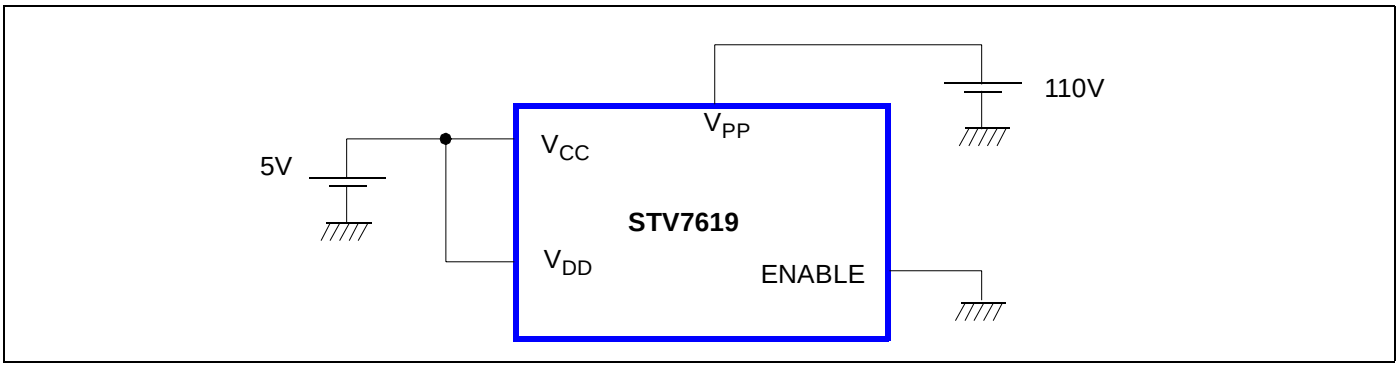


Figure 4: External Power Supply (Large-size PDP)

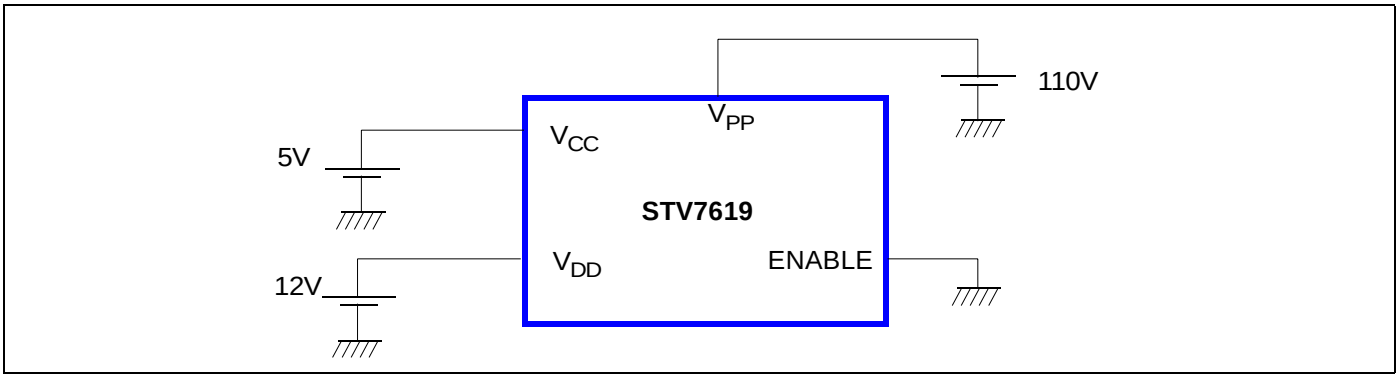
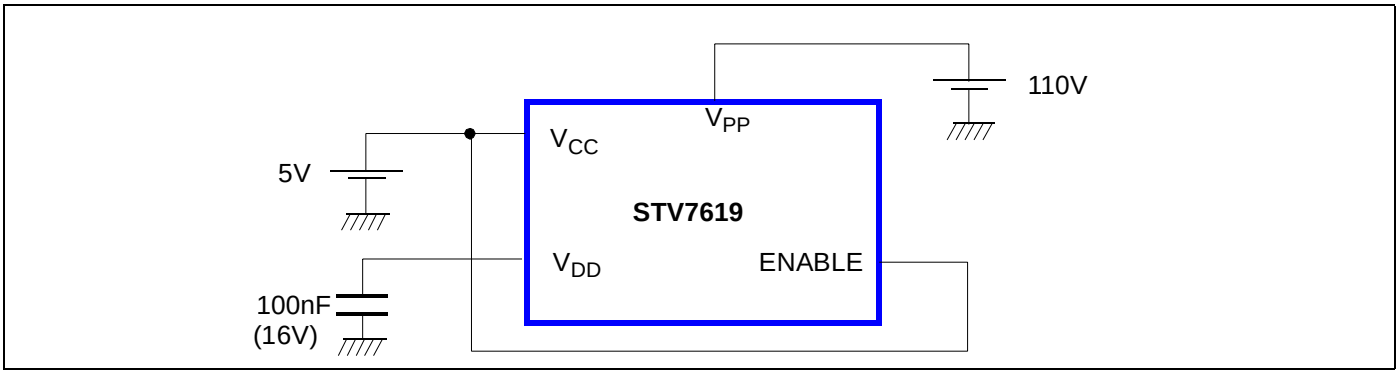
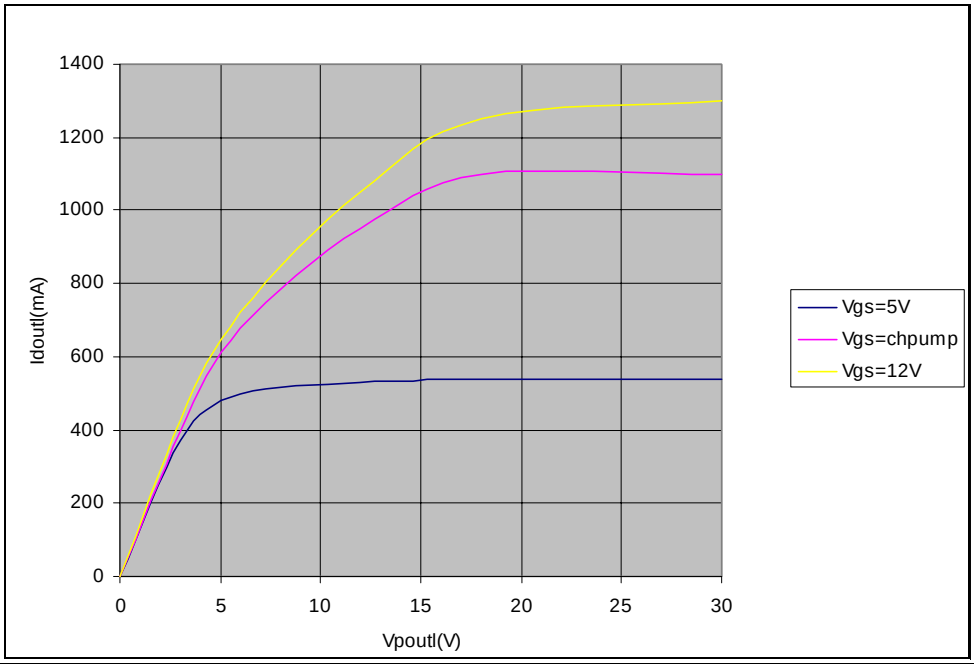


Figure 5: Internal Power Supply, Charge Pump mode (Medium- or Large-size PDP)



3.2 Sink Current Characteristics

Figure 6: Typical Sink Stage Characteristics (Peak current and T_{AMB} = 25 °C)



3.3 Recommendations

The Sustain current must not be sunk in the power outputs to VPP when the power supply is applied. VSSSUB and VSSLOG must be connected close to the logical reference ground of the logic control signal buffers.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Logic Supply	-0.3, +7	V
V_{DD}	Logic supply of power part	-0.3, +14	V
OUTi	Output Pins	-0.3, +120	V
V_{IN}	Logic Input Voltage	-0.3, V_{CC} +0.3	V
V_{OUT}	Logic Output Voltage	-0.3, V_{CC} + 0.3	V
V_{POUT}	Driver Output Voltage (scanning mode)	-0.3, +120	V
V_{ESD}	ESD Susceptibility (Human Body model: 100 pF capacitor discharged through 1.5 kΩ serial resistor) (See Note 1)	±2200	V
I_{POUT}	Driver Output Current (See Note 2, Note 5 and Note 6)	-150 mA/+1.2	A
I_{DOUT1}	Diode Output Current (See Note 3 and Note 5)	±1	A
I_{DOUT2}	Diode Output Current (See Note 4 and Note 5)	±700	mA
T_{JMAX}	Junction Temperature	+150	°C
T_{OPER}	Operating Temperature	-20, +85	°C
T_{STG}	Storage Temperature	-20, +150	°C

Note:1. All pins in relation to V_{CC} = -1500V

2. Through one power output.

3. Through one diode

4. Through all power outputs (see test diagram): with power dissipation lower than or equal to Ptot and Junction temperature lower than or equal to T_{jmax} and V_{PP} = V_{SSP}.

5. These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

6. For V_{DD} = 9 V, I_{POUT} = 1.0 A, for V_{DD} = 5 V, I_{POUT} = 0.5 A

4.2 Thermal Data

Symbol	Parameter	Value	Units
T_{JOPER}	Maximum Operating Junction	125	°C
R_{thJA}	Junction-ambient Thermal Resistance (See Note 1)	20	°C/W
R_{thJA}	Junction-ambient Thermal Resistance (See Note 2)	40	°C/W
R_{thJA}	Junction-ambient Thermal Resistance (See Note 3)	29	°C/W

Note:1. For TQFP100 packaging with slug soldered on printed circuit board.

2. TQFP soldered on 4-layer printed circuit board.

3. For TQFP100 packaging with slug not soldered on printed circuit board.

4.3 Supply Characteristics

(V_{SSP} = 0 V, V_{SSLOG} = 0 V, V_{SSSUB} = 0 V, T_{AMB} = 25°C and f_{CLK} = 8 MHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
V_{DD}	Logic Supply Voltage for Output Stage		V_{CC}		13	V
V_{PP}	Power Output Supply Voltage		20		110	V
I_{CCH}	Logic Supply Current	with V_{DD}=5 or 12 V (ENABLE=L) with pump charge capacitor (ENABLE=H)		 0.3	100 2	µA mA
I_{CCL}	Dynamic Logic Supply Current	f_{CLK} = 8 MHz		TBD		mA
I_{PPH}	Power Output Supply Current (steady outputs)				100	µA

4.4 Power Output Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{POUTH}	Power Output High Level (Voltage drop versus V_{PP})	I_{POUTH} = - 60 mA	TBD	4.2		V
V_{POUTL}	Power Output Low Level voltage drop I_{POUTL}= +400 mA	V_{DD}=12V (ENABLE = L)		2.5	TBD	V
		V_{DD}=5V (ENABLE = L)		3.4	TBD	V
		pump charge capacitor on V_{DD} (ENABLE = H)		2.8	TBD	V
I_{POULP}	Power Output Low Level Peak current V_{POUTL}=12 V (See Note 1) (Pulse ≤ 500ns)	V_{DD}=12 V (ENABLE = L)	TBD	1100		mA
		V_{DD}= 5V (ENABLE= L)	TBD	530		mA
		pump charge capacitor on V_{DD} (ENABLE = H)	TBD	1000		mA
V_{DOUTH}	Output Diode High Level (See Note 2 and Note 3)	I_{DOUTH} = +400 mA		1.8	3.0	V
V_{DOUTL}	Output Diode Low Level (See Note 2 and Note 3)	I_{DOUTL} = - 400 mA		-1.25	-3.00	V

Note:1. Peak current - Pulse mode 720 Hz - 0.2%. Duty cycle.

2. Compatible with power dissipation and $T_{JOPER} \leq 125°C$.

3. See Figure 8: Test Configuration on page 17*.*

4.5 SOUT Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Logic Output High Level	I_{OH} = -1 mA	4.2	4.6		V
V_{OL}	Logic Output Low Level	I_{OL} = +1 mA		0.1	0.4	V

4.6 Input (CLK, $\overline{STB}$, BLK, POC, SIN, CLR, F/$\overline{R}$ and ENABLE) Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Level		0.8 V_{CC}			V
V_{IL}	Input Low Level				0.2V_{CC}	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$			±10	µA
I_{IL}	Low Level Input Current for pins CLK, SIN, $\overline{STB}$, CLR, BLK and POC	V_{IL} = 0 V			±10	µA
I_{IL}	Low Level Input Current for ENABLE pin	V_{IL} = 0 V		-25		µA

4.7 AC Timing Requirements

V_{CC} = 4.5 V to 5.5 V, T_{AMB} = -20 to +85°C, max. leading/trailing edge for input signals (t_r, t_f) = 10 ns

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WHCLK}	Duration of clock (CLK) pulse at high level	40			ns
t_{WLCLK}	Duration of clock (CLK) pulse at low level	40			ns
t_{SDAT}	Set-up Time of data input before clock (low to high) transition	10			ns
t_{HDAT}	Hold Time of data input after clock (low to high) transition	20			ns
t_{DSTB}	Minimum Delay to latch $\overline{STB}$ after clock (low to high) transition	25			ns
t_{SSTB}	Set-up Time $\overline{STB}$ before clock (low to high) transition	10			ns
t_{STB}	Latch $\overline{STB}$ Low Level Pulse Duration	20			ns
t_{BLK}	Blanking (BLK) Pulse Duration	100			ns

4.8 AC Timing Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CLK}	Data Clock Period	125			
t_{RDAT}	Logical Data Output Rise Time		25		
t_{FDAT}	Logical Data Output Fall Time		15		
t_{PHL1}	Delay of logic data output (high to low transition) after clock (CLK) transition (CL=10pF)		45		
t_{PLH1}	Delay of logic data output (low to high transition) after clock (CLK) transition (CL=10 pF)		50		ns
t_{PHL2}	Delay of power output change (high to low transition) after clock (CLK) transition		TBD	180	ns
t_{PLH2}	Delay of power output change (low to high transition) after clock (CLK) transition		TBD	180	ns
t_{PHL3}	Delay of power output change (high to low transition) after Latch ($\overline{STB}$) transition		TBD	165	ns
t_{PLH3}	Delay of power output change (low to high transition) after Latch ($\overline{STB}$) transition		TBD	165	ns
t_{PHL4}	Delay of power output change (high to low transition) to POC transition		105	160	ns
t_{PLH4}	Delay of power output change (low to high transition) to POC transition		100	160	ns
t_{ROUT}	Power Output Rise Time (See Note 1)		100		ns
t_{FOUT}	Power Output Fall Time (See Note 1)		30		ns

Note:1. One output among 64, loading capacitor C_{OUT} = 200 pF, other outputs at low or high level.

Figure 7: AC Characteristics Waveform

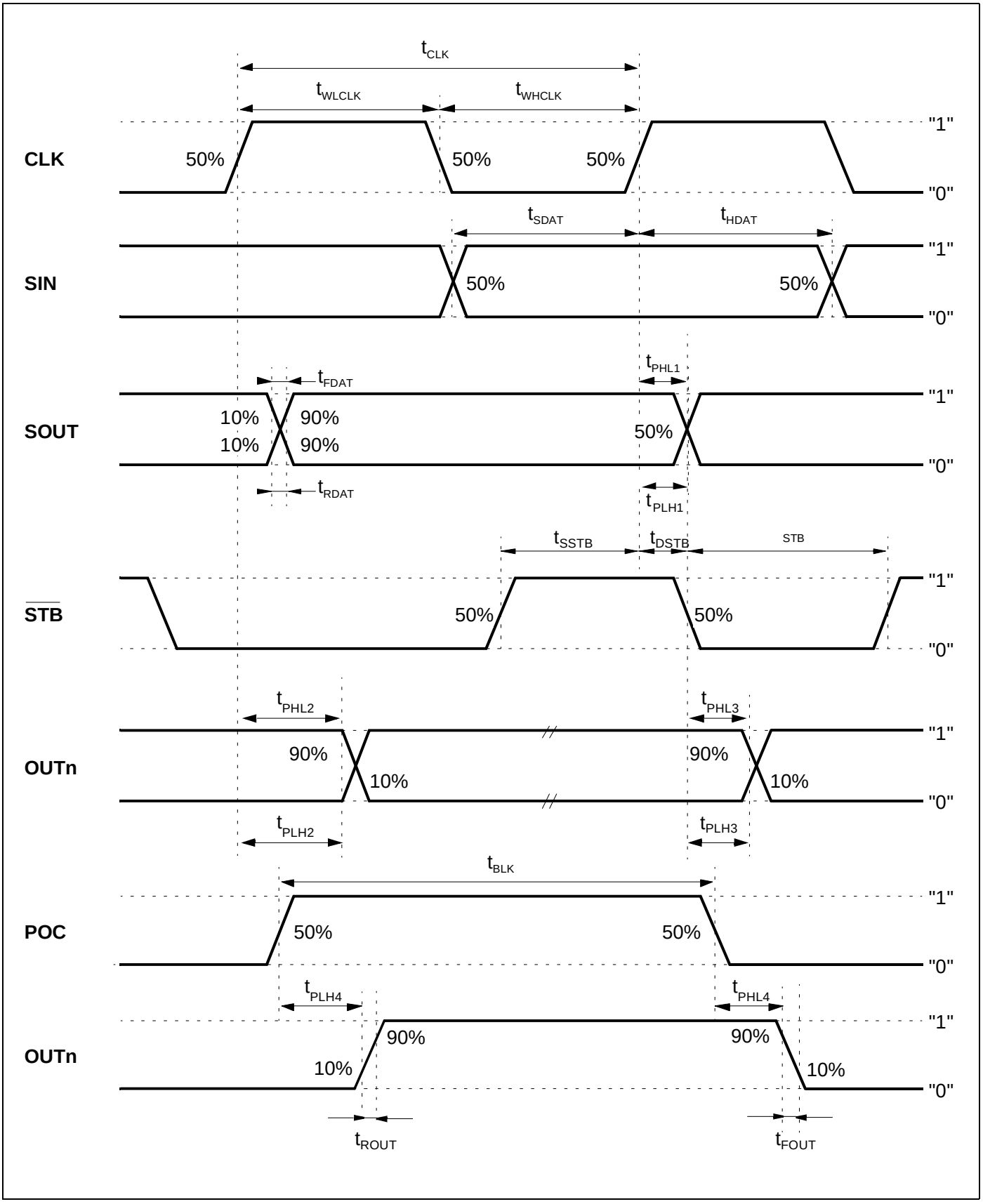
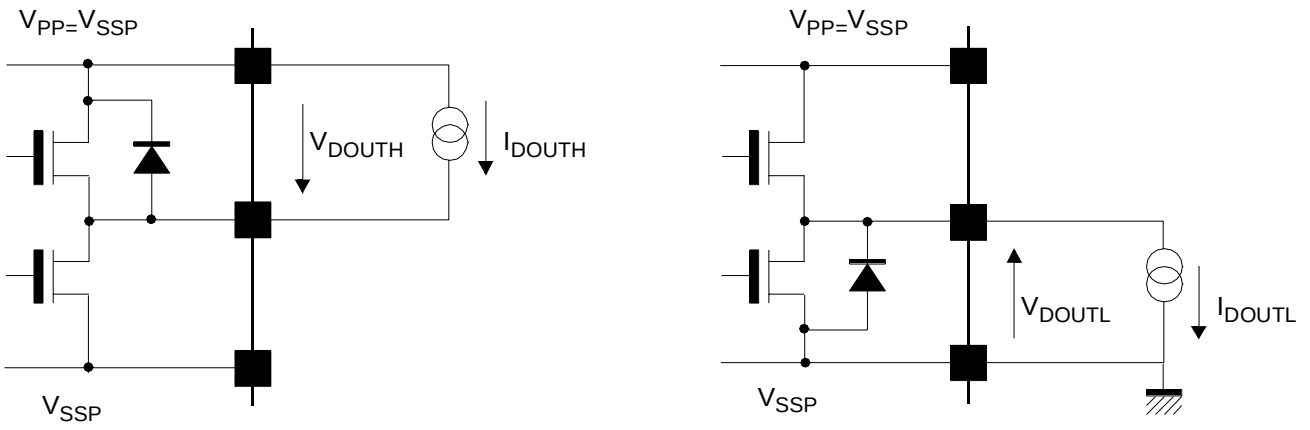


Figure 8: Test Configuration



Output sinking current as positive value, sourcing current as negative value.

5 Input/Output Schematic Diagrams

Figure 9: ENABLE Input

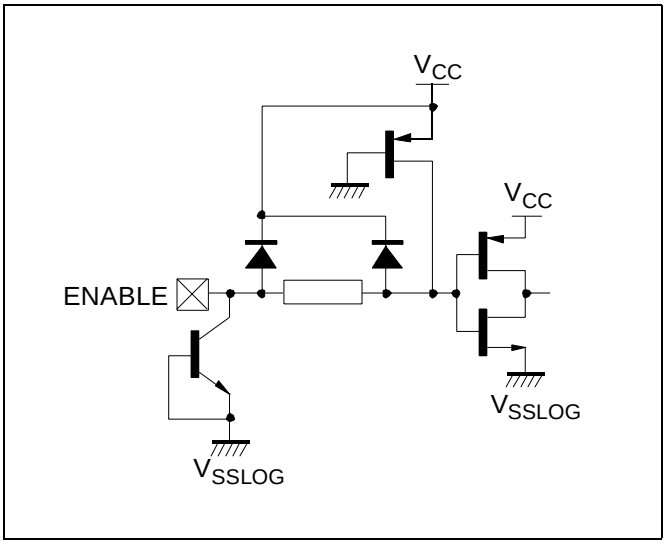


Figure 10: F/$\overline{R}$, CLR, CLK, $\overline{STB}$, BLK and POC Inputs

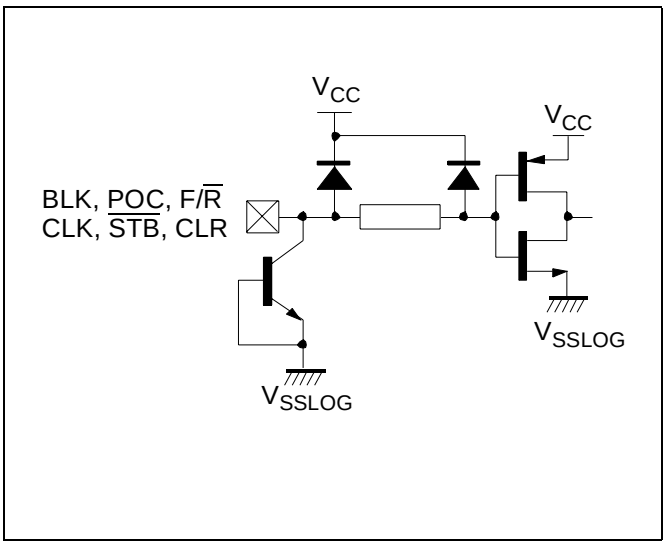


Figure 11: SIN, SOUT Input

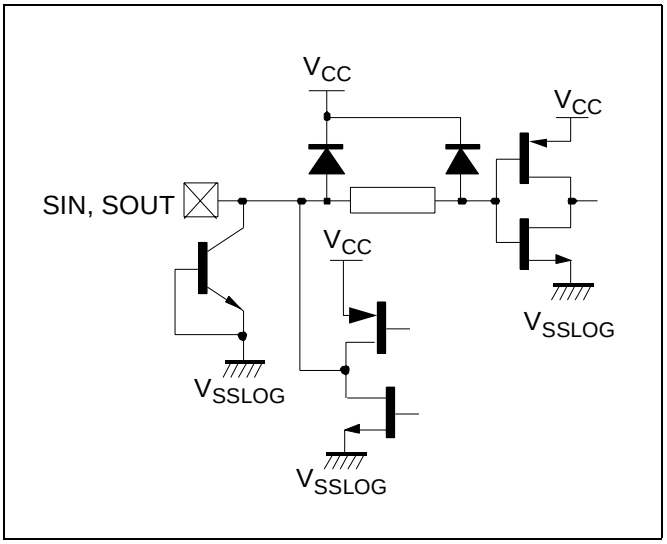
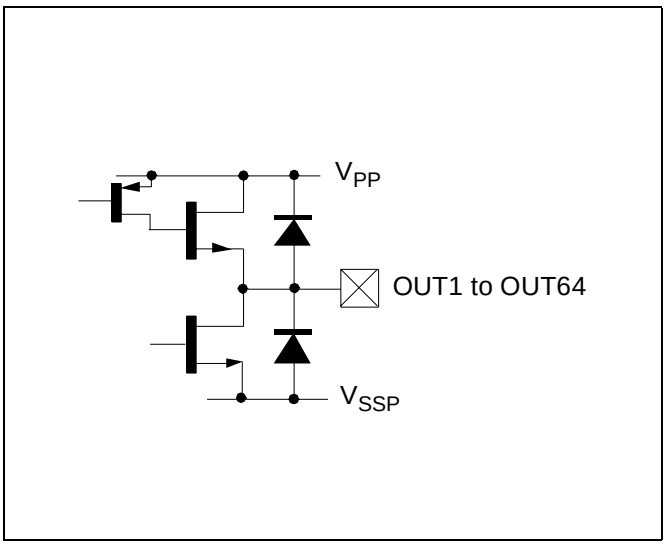
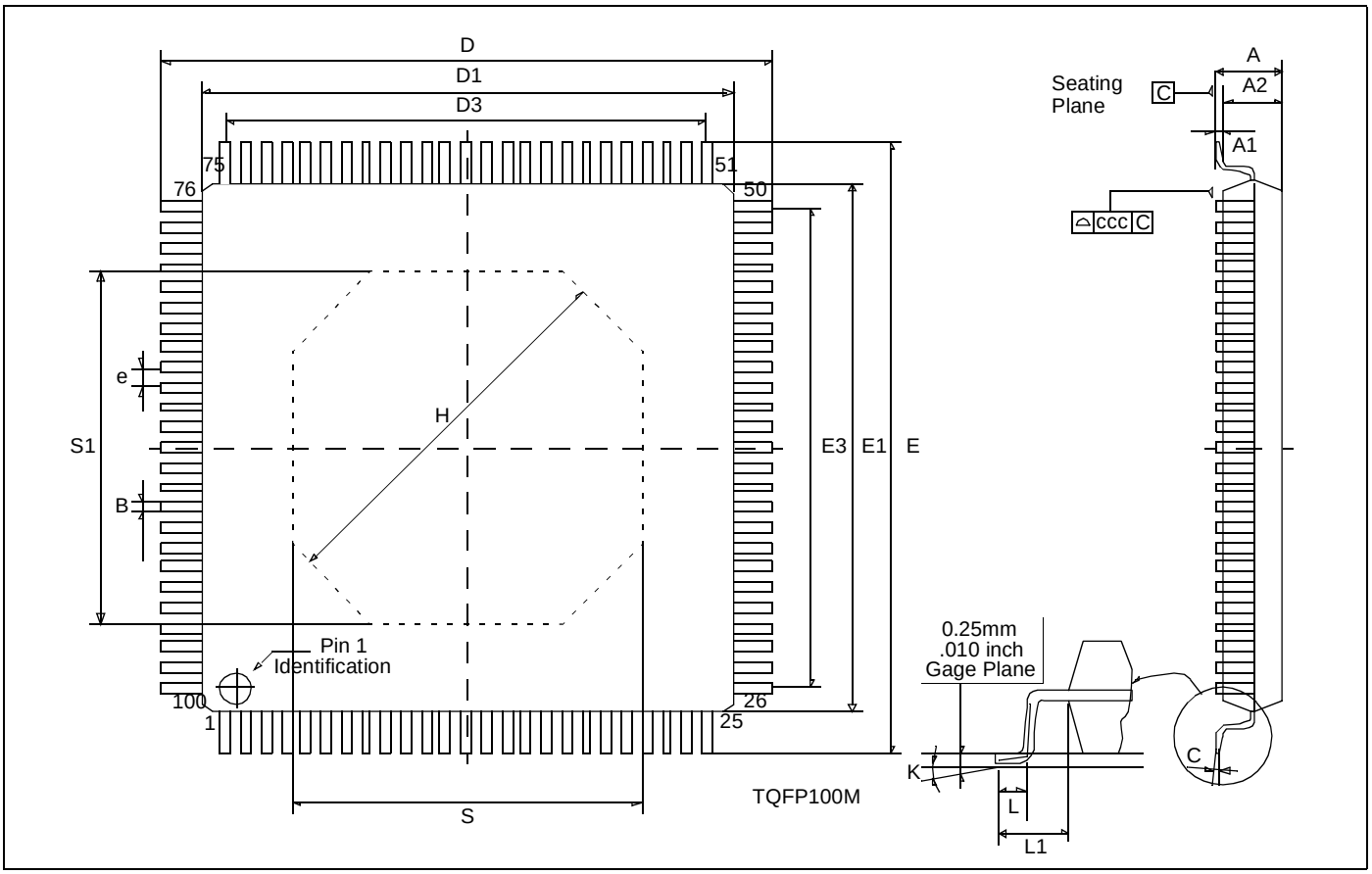


Figure 12: Power Outputs



6 Package Mechanical Data

Figure 13: TQFP100 Package



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.20	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (Min.), 7° (Max.)					
Slug Dimension For L/Frame Pad Size 10.00 x 10.00 mm						
H		9.85			0.388	
S	8.80			0.346		
S1	8.80			0.346		

7 Revision History

Table 8: Summary of Modifications

Version	Date	Description
Target Specification		
1.0	April 2001	First version issued
1.1	April 2001	Corrections from the design
1.2	May 2001	Corrections in Table 1 and text added in Circuit description
1.3	May 2001	Inversion of BLK and POC pinsin block diagram and Table 1.
Product Preview		
2.0	September 2001	Pin connections - pins 30 to 50 corrected, Pin assignements: completed, Block diagram: voltage generator added, Circuit description: text modified, Application hints chapter added, Electrical characteristics: few precisions, Input/output schematics: corrections
2.1	October 2001	Pin connections - pins 38 added to pin description, Electrical characteristics: I_{IH} and $I_{IL,}$ typical value is ±10, AC timing characteristics: t_{PHL4} and t_{PLH4}: (BLK) replaced with (POC), Figure 5: AC characteristics waveform: STB and OUTn waveforms replaced, BLK renamed with POC.
2.2	November 2001	Page 10 - C_{VDD} value replaced with 100 nF (1 previously), Page 11 - figure 3 - C_{VDD} value replaced with 100 nF, Page 12 - Figure 4 replaced. Sentence modified in subsection 7.3 recommendations: the logical reference ground "*of the application"* replaced with "*of the logic control signal buffers*". Page 13 - absolute maximum ratings - Ioutput value replaced with -150mA/ +1.2A. Note removed. Page 14- Electrical characteristics: values replaced. Page 15 - AC timing charactersitics: values replaced
2.3	January 2002	Electrical characteristics: First sentence: Vpp and Vdd removed, in the table: Vpp moved after Vdd.
Preliminary Data		
2.4	24 July 2002	Reformatted datasheet. Deletion of STV7619U (Slug-up) device and related information. Modification of values in Note 6 on page 11. Addition of Note 3 on page 12. Update of typical values in Section 4.
2.5	13 January 2003	Addition of V_{ESD} information in Section 4.1: Absolute Maximum Ratings on page 11.
Datasheet		
3.0	August 2003	Published on internet.