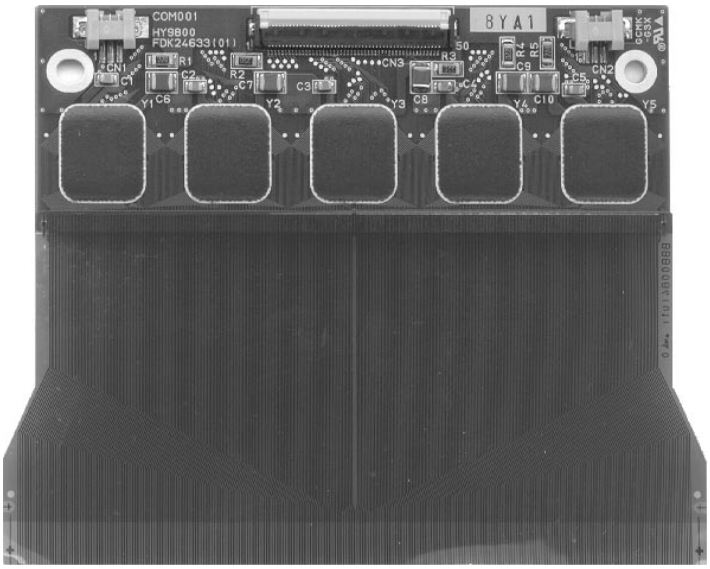
CM17699

COLOR PDP DRIVER MODULE

PRODUCT PREVIEW



CM17699.TIF

The CM17699 is plasma Display Panel (PDP) data driver board implementing 5 data drivers referenced STV7699.

This module addresses 320 column electrodes of a plasma panel. The monoblock structure of this module and the output Flexible Printed Circuit (FPC) realizes a high density package for data drivers ICs. This module is adapted to standard definition large size PDPs. The bidirectional feature of this module allows its implementation on the top side and/or bottom side of the panel without any modification in the data bit stream.

1 - CM17699 MAIN FEATURES

- Equiped with five STV7699 devices - 4 x 16-bit bidirectional shift register
- Mounted connectors/capacitors
- Configurable for AC/DC power supply
- FPC compatible with narrow pitches of column electrodes
- Compatible with custom designs.

Output Count	320
Output Pitch	320mm
Logic Power Supply	4.5V to 5.5V
Power Supply Voltage	30V to 160V
Power Output Current	±40mA
Clock Frequency	20MHz
Dimension	COB - 92 x 33 FPC - 101.4 x 50

2 - CM17699 CONNECTORS DEFINITION

2.1 - Signal Connector

Input signal connector is a 50 nodes high density connector defined as follow :

1	A14
2	A13
3	A12
4	A11
5	B11
6	B12
7	B13
8	B14
9	A24
10	A23
11	A22
12	A21
13	B21
14	B22
15	B23
16	B24
17	A34
18	A33
19	A32
20	A31
21	B31
22	B32
23	B33
24	B34
25	BLK
26	VSS
27	POL
28	VSS
29	F/R
30	VSS
31	STB
32	VSS
33	CLK
34	VSS
35	A44
36	A43
37	A42
38	A41
39	B41
40	B42
41	B43
42	B44
43	A54
44	A53
45	A52
46	A51
47	B51
48	B53
49	B53
50	B54

2.2 - Power Supply Connector

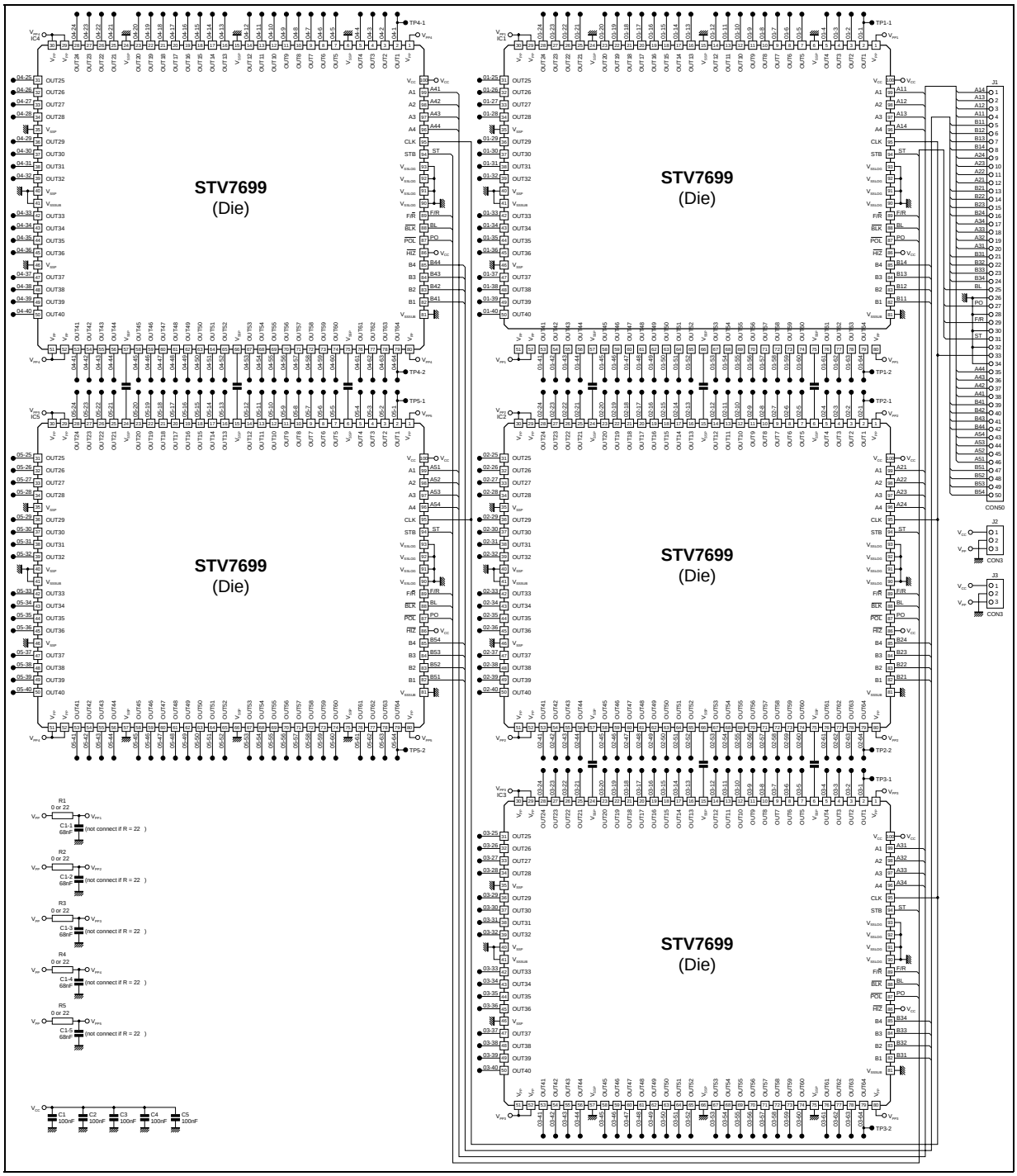
Power supplies come from 2 connectors of 3 nodes each (V_{PP}, V_{DD}, V_{SS}). The use of both connectors is not necessary as all the supplies are connected together on the board. The use of both connectors spread the currents on the PC borad and reduce the EMI radiations.

Depending on the application, the data module can be configured either for DC supplies or for AC supplies of the data drivers by the implementation of surface mounted devices.

3 - CM17699 SCHEMATIC

Decoupling capacitors must be located as close as possible to the drivers. If the damping and protection resistor in V_{PP} line of each driver is different to 0Ω, the decoupling capacitor should not be mounted.

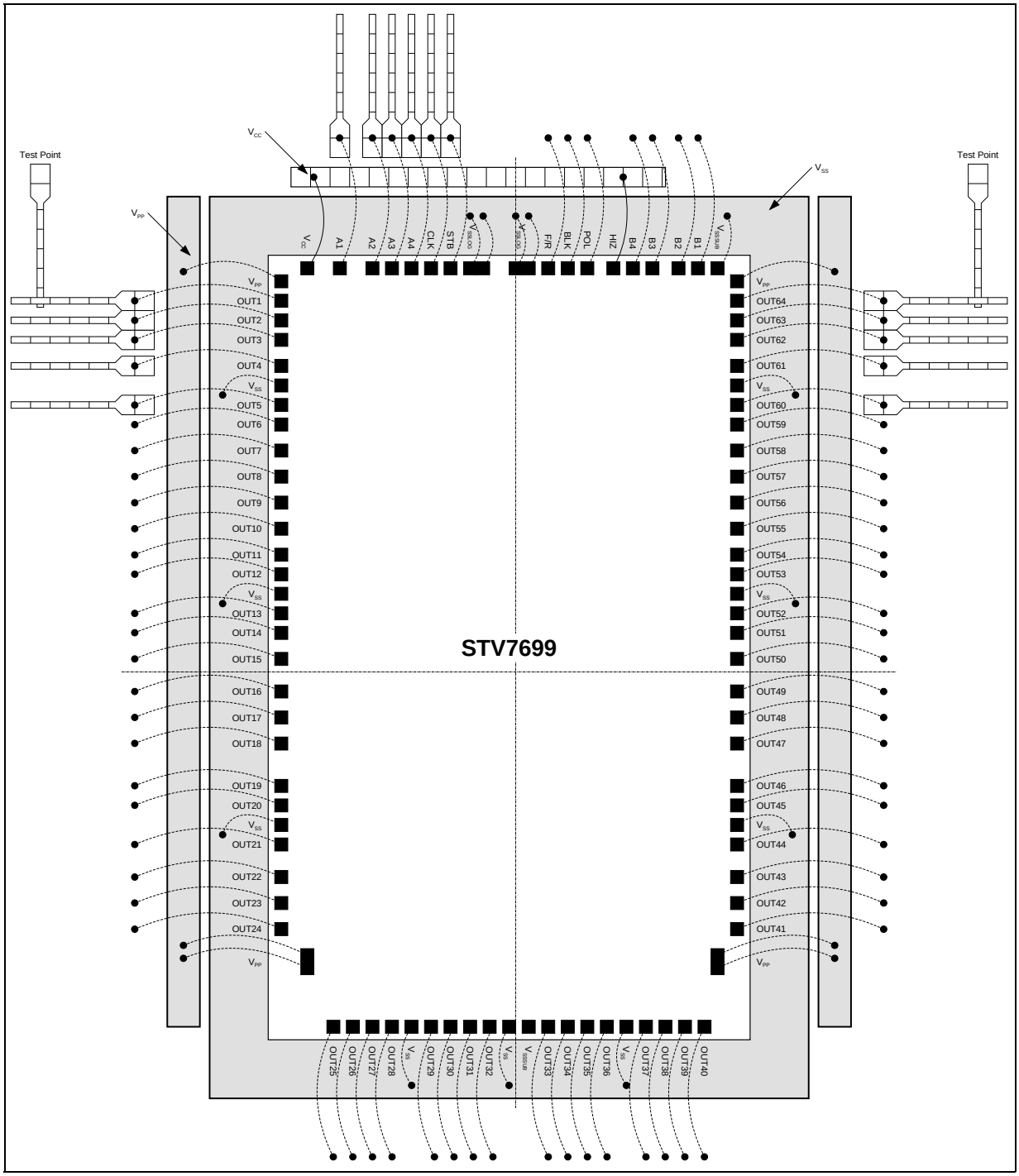
Figure 1



3 - CM17699 SCHEMATIC (continued)

3.1 - Details of Die Bonding

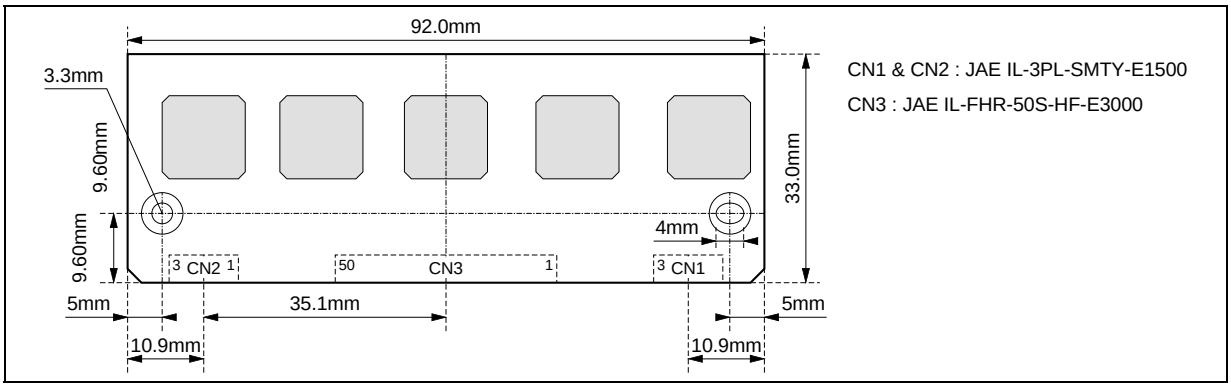
Figure 2



4 - PCB MECHANICAL SPECIFICATIONS

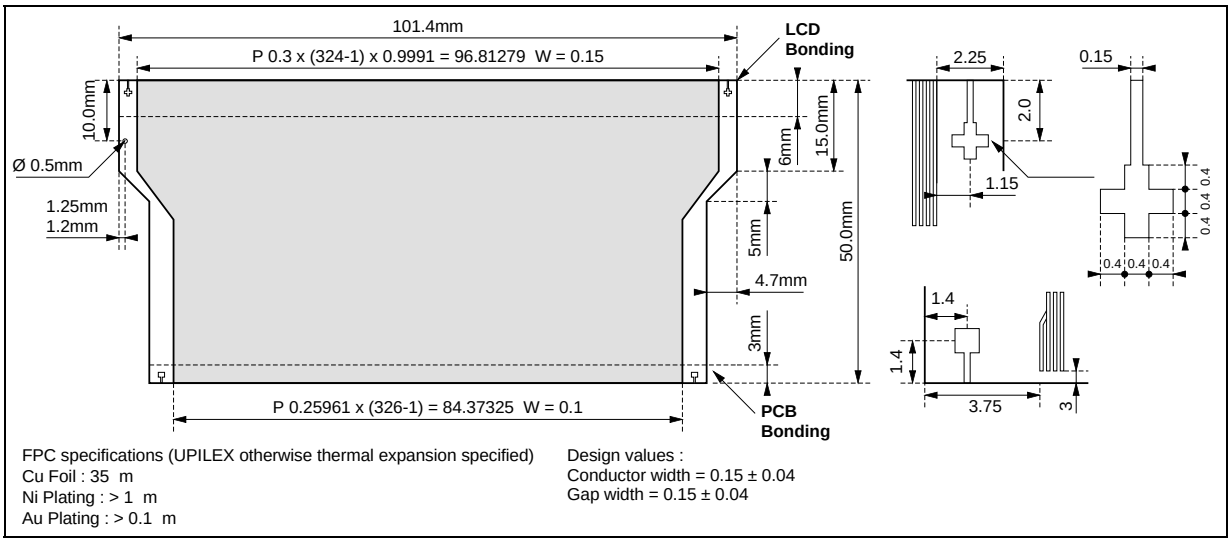
The rigid board is 92mm long by 30mm wide.
The rigid board can be mounted on the mechanical chassis of the plasma panel or on a heat sinker by clips and/or screws.
The recommended size of the heat sinker depends on the final application if data drivers are powered with a DC or an AC supply.
Power supplies (V_{PP}, V_{SS}) are dispatched by large copper surface in order to spread the current on the board and reduce voltage drops and EMI.

Figure 3



5 - FPC MECHANICAL SPECIFICATIONS

Figure 4



6 - STV7699 SPECIFICATIONS

6.1 - Features

- 64 outputs plasma display driver
- 170V absolute maximum supply
- 5V supply for logic
- 50/40mA source / sink output
- 60/60mA source / sink output diode
- 64-bit shift register (20MHz)
- BLK, polarity and HIZ control
- BCD technology

6.2 - General Description

The STV7699 is a Plasma Display Panel (PDP) data driver implemented in ST's proprietary BCD technology. Using a 4-bit wide cascadable shift register, it drives 64 high current & high voltage outputs. By serialy connecting several STV7699, any horizontal pixel definition can be performed. The 20MHz shift clock gives an equivalent 80MHz shift register. The STV7699 is supplied with a separated 170V power output supply and a 5V logic supply. All command inputs are CMOS compatible.

6 - STV7699 SPECIFICATIONS (continued)

6.3 - Pad Dimensions (in µm)

The reference is the center of the die (x = 0, y = 0).

LEFT SIDE from top to bottom

Name	Center : X	Center : Y	Size : x	Size : y
V_{PP}	-1738.0	2867.5	90.0	75.0
OUT1	-1738.0	2703.0	90.0	75.0
OUT2	-1738.0	2570.5	90.0	75.0
OUT3	-1738.0	2411.0	90.0	75.0
OUT4	-1738.0	2228.5	90.0	75.0
V_{SSP}	-1738.0	2093.0	90.0	75.0
OUT5	-1738.0	1952.0	90.0	75.0
OUT6	-1738.0	1813.5	90.0	75.0
OUT7	-1738.0	1631.0	90.0	75.0
OUT8	-1738.0	1453.0	90.0	75.0
OUT9	-1738.0	1235.5	90.0	75.0
OUT10	-1738.0	1046.5	90.0	75.0
OUT11	-1738.0	862.0	90.0	75.0
OUT12	-1738.0	712.5	90.0	75.0
V_{SSP}	-1738.0	566.0	90.0	75.0
OUT13	-1738.0	431.0	90.0	75.0
OUT14	-1738.0	293.0	90.0	75.0
OUT15	-1738.0	82.5	90.0	75.0
OUT16	-1738.0	-109.5	90.0	75.0
OUT17	-1738.0	-277.0	90.0	75.0
OUT18	-1738.0	-471.0	90.0	75.0
OUT19	-1738.0	-691.5	90.0	75.0
OUT20	-1738.0	-822.5	90.0	75.0
V_{SSP}	-1738.0	-953.0	90.0	75.0
OUT21	-1738.0	-1096.0	90.0	75.0
OUT22	-1738.0	-1335.5	90.0	75.0
OUT23	-1738.0	-1569.0	90.0	75.0
OUT24	-1738.0	-1697.5	90.0	75.0
V_{PP}	-1715.0	-2045.0	90.0	200.0

Right SIDE from bottom to top

Name	Center : X	Center : Y	Size : x	Size : y
V_{PP}	1600.5	-2087.0	90.0	200.0
OUT41	1737.5	-1646.0	90.0	75.0
OUT42	1737.5	-1507.0	90.0	75.0
OUT43	1737.5	-1328.0	90.0	75.0
OUT44	1737.5	-1096.0	90.0	75.0
V_{SSP}	1737.5	-953.0	90.0	75.0
OUT45	1737.5	-822.5	90.0	75.0
OUT46	1737.5	-691.5	90.0	75.0
OUT47	1737.5	-471.0	90.0	75.0
OUT48	1737.5	-277.0	90.0	75.0
OUT49	1737.5	-109.5	90.0	75.0
OUT50	1737.5	82.5	90.0	75.0
OUT51	1737.5	293.0	90.0	75.0
OUT52	1737.5	431.0	90.0	75.0
VSSP	1737.5	566.0	90.0	75.0
OUT53	1737.5	712.5	90.0	75.0
OUT54	1737.5	862.0	90.0	75.0
OUT55	1737.5	1046.5	90.0	75.0
OUT56	1737.5	1235.5	90.0	75.0
OUT57	1737.5	1453.0	90.0	75.0
OUT58	1737.5	1631.0	90.0	75.0
OUT59	1737.5	1813.5	90.0	75.0
OUT60	1737.5	1952.0	90.0	75.0
V_{SSP}	1737.5	2093.0	90.0	75.0
OUT61	1737.5	2228.5	90.0	75.0
OUT62	1737.5	2411.0	90.0	75.0
OUT63	1737.5	2570.5	90.0	75.0
OUT64	1737.5	2703.0	90.0	75.0
V_{PP}	1737.5	2873.5	90.0	75.0

BOTTOM SIDE from left to right

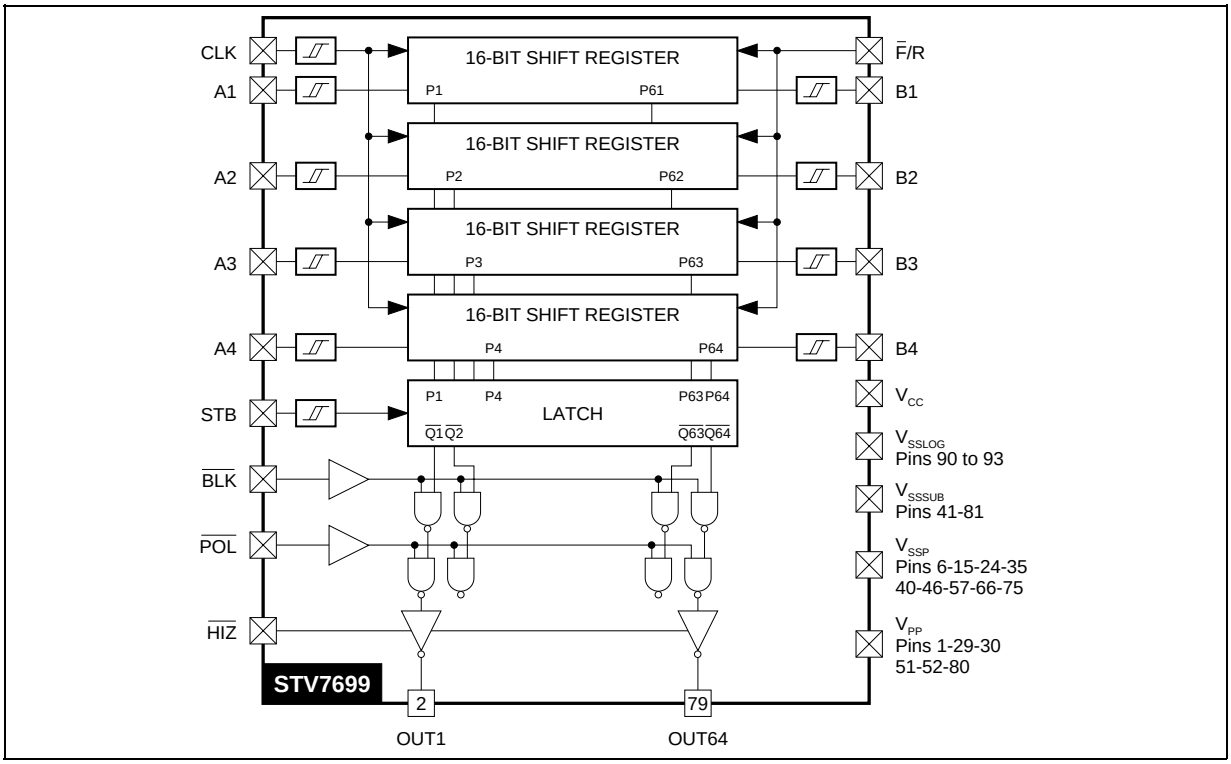
Name	Center : X	Center : Y	Size : x	Size : y
OUT25	-1443.5	-3077.0	75.0	90.0
OUT26	-1249.0	-3077.0	75.0	90.0
OUT27	-1049.5	-3077.0	75.0	90.0
OUT28	-889.0	-3077.0	5.0	90.0
V_{SSP}	-753.0	-3077.0	75.0	90.0
OUT29	-614.0	-3077.0	75.0	90.0
OUT30	-467.5	-3077.0	75.0	90.0
OUT31	-332.0	-3077.0	75.0	90.0
OUT32	-186.5	-3077.0	75.0	90.0
V_{SSP}	-54.0	-3077.0	75.0	90.0
V_{SSSUB}	78.0	-3077.0	75.0	90.0
OUT33	209.5	-3077.0	75.0	90.0
OUT34	342.5	-3077.0	75.0	90.0
OUT35	467.5	-3077.0	75.0	90.0
OUT36	607.5	-3077.0	75.0	90.0
V_{SSP}	752.0	-3077.0	75.0	90.0
OUT37	892.5	-3077.0	75.0	90.0
OUT38	1045.5	-3077.0	75.0	90.0
OUT39	1252.0	-3077.0	75.0	90.0
OUT40	1433.5	-3077.0	75.0	90.0

TOP SIDE from right to left

Name	Center : X	Center : Y	Size : x	Size : y
V_{SSSUB}	1628.5	3073.5	75.0	90.0
B1	1478.5	3073.5	75.0	90.0
B2	1228.5	3077.0	75.0	90.0
B3	978.5	3077.0	75.0	90.0
B4	847.5	3077.0	75.0	90.0
HIZ	716.5	3077.0	75.0	90.0
$\overline{POL}$	486.5	3077.0	75.0	90.0
$\overline{BLK}$	355.5	3077.0	75.0	90.0
$\overline{F/R}$	224.5	3077.0	75.0	90.0
V_{SSLOG}	31.0	3077.0	200.0	90.0
V_{SSLOG}	-354.5	3077.0	200.0	90.0
STB	-582.0	3077.0	75.0	90.0
CLK	-713.0	3077.0	75.0	90.0
A4	-844.0	3077.0	75.0	90.0
A3	-975.0	3077.0	75.0	90.0
A2	-1106.0	3077.0	75.0	90.0
A1	-1471.5	3077.0	75.0	90.0
V_{CC}	-1629.0	3077.0	75.0	90.0

6 - STV7699 SPECIFICATIONS (continued)

6.4 - Block Diagram



6.5 - Circuit Description

STV7699 contains all the logic and the power circuits necessary to drive the colums of a Plasma Display Panel (P.D.P.). Data are shifted at each low to high transition of the (CLK) shift clock. Data are input in a 4-bit wide data bus to A1 - A4 input (case of forward shift mode ; F/R = low). After 16 shifts, the first nibble is available at the serial outputs B1 - B4. These outputs can be used to cascade several drivers to perform any horizontal resolution. CLK, Ai and Bi inputs are Smith trigger inputs to improve the noise margin.

The Forward/Reverse (F/R) input is used to select the direction of the shift register.

The maximum frequency of the shift clock is 20MHz.

All the output data are held and memorized into the latch stage when the Latch input (STB) is high. When it is at low level, data are transferred from the shift register to the latch and to the output power stage.

Output state can be forced to high impedance by pulling low HIZ input.

When BLK is Low, all the outputs are forced to low level or high level according to POL signal value.

Output state copy data that was input, with the same polarity, when BLK, HIZ and POL are High.

V_{SSLOG}, V_{SSSUB} and V_{SSP} are not internally connected.

V_{SSLOG} and V_{SSSUB} must be connected as close as possible to the logical reference ground of the application.

Table 1 : Power Output Truth Table

Data	STB	POL	BLK	HIZ	Driver Output	Comments
x	x	x	x	L	HIZ	High impedance
x	x	L	x	H	L	Forced to low
x	x	H	L	H	H	Forced to high
x	H	H	H	H	Qn (1)	Latched data
L	L	H	H	H	L	Copy data
H	L	H	H	H	H	Copy data

Note 1 : Qn is the value memorised in the latch stage ; it is the value of the parallel shift register output stage after n Clock pulses.

A data loaded in the shift register is read on the output power stage without inversion of its polarity.

Table 2 : Control Table

F/R	Ai	Bi	Comments
L	Input	Output	Forward shift
H	Output	Input	Reverse shift

6 - STV7699 SPECIFICATIONS (continued)

6.6 - Characteristics

6.6.1 - Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply	-0.3, +7	V
V_{IN}	Logic Input Voltage	-0.3, V_{CC} + 0.3	V
V_{OUT}	Logic Output Voltage	-0.3, V_{CC} + 0.3	V
V_{POUT}	Driver Output Voltage	-0.3, +170	V
V_{PP}	Driver Power Supply	-0.3, +170	V
I_{POUT}	Driver Output Current (1)	±60	mA
I_{DOUT}	Diode Output Current (1)	+40/-50	mA
T_{jmax}	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	-20, +85	°C
T_{stg}	Storage Temperature	-50, +150	°C

Note : 1. Through all power outputs : with power dissipation lower or equal than P_{tot} and junction temperature lower or equal than T_{jmax}.

6.6.2 - Electrical Characteristics

(V_{CC} = 5V, V_{PP} = 160V, V_{SSP} = 0V, V_{SSLOG} = 0V, V_{SSSUB} = 0V, T_{amb} = 25°C, f_{CLK} = 20MHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current		-	-	100	µA
I_{CCL}	Logic Supply Current	f_{CLK} = 20MHz	-	12	TBD	mA
V_{PP}	Power Output Supply Voltage		-	-	160	V
I_{PPH}	Power Output Supply Current (steady outputs)		-	-	100	µA
OUTPUT						
OUT1-OUT64						
V_{POUTH}	Power Output High Level	I_{POUTH} = - 10mA, V_{PP} = 65V I_{POUTH} = - 40mA, V_{PP} = 65V	55 TBD	60 -	- -	V V
V_{POUTL}	Power Output Low Level	I_{POUTL} = + 10mA I_{POUTL} = + 30mA	- -	2 12	5 TBD	V V
V_{DOUTH}	Output Diode High Level	I_{DOUTH} = + 25mA (2)(3)	-	-	3	V
V_{DOUTL}	Output Diode Low Level	I_{DOUTL} = - 25mA (2)(3)	-	-	-3	V
I_{OUTHIZ}	Output Stage Leakage Current on $\overline{HIZ}$ State		-	-	±10	µA
SHIFT REGISTER OUTPUT (Ai or Bi according to $\overline{F}$/R Status)						
V_{OH}	Logic Output High Level	I_{OH} = - 0.5mA	4	-	-	V
V_{OL}	Logic Output Low Level	I_{OL} = + 0.5mA	-	0.1	0.3	V
INPUT (CLK, STB, $\overline{BLK}$, $\overline{HIZ}$, Ai, Bi)						
V_{IH}	Input High Level		0.8 V_{CC}	-	-	V
V_{IL}	Input Low Level		-	-	0.2 V_{CC}	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	-	-	1	µA
I_{IL}	Low Level Input Current	V_{IL} = 0V	-	-	-1	µA

Notes : 2. Compatible with power dissipation and $T_{joper} \leq 125°C$.
3. See test diagram.

6 - STV7699 SPECIFICATIONS (continued)

6.6.3 - AC Timings Requirements

(V_{CC} = 4.5V to 5.5V, T_{amb} = -20 to +85°C, input signals max leading edge & trailing edge (t_R, t_F) = 10ns)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	50	-	-	ns
t_{WHCLK}	Duration of clock (CLK) pulse at high level	15	-	-	ns
t_{WLCLK}	Duration of clock (CLK) pulse at low level	15	-	-	ns
t_{SDAT}	Set-up Time of data input before clock (low to high) transition	0	-	-	ns
t_{HDAT}	Hold Time of data input after clock (low to high) transition	15	-	-	ns
t_{DSTB}	Minimum Delay to latch (STB) after clock (low to high) transition	20	-	-	ns
t_{STB}	Latch (STB) Low Level Pulse Duration	10	-	-	ns
t_{BLK}	Blanking ($\overline{BLK}$) Pulse Duration	100	-	-	ns
t_{POL}	Polarity ($\overline{POL}$) Pulse Duration	100	-	-	ns
t_{HIZ}	High Impedance ($\overline{HIZ}$) Pulse Duration	100	-	-	ns
t_{SFR}	Set-up Time of $\overline{Forward}$/Reverse Signal before Clock (low to high) transition	100	-	-	ns

6.6.4 - AC Timings Characteristics

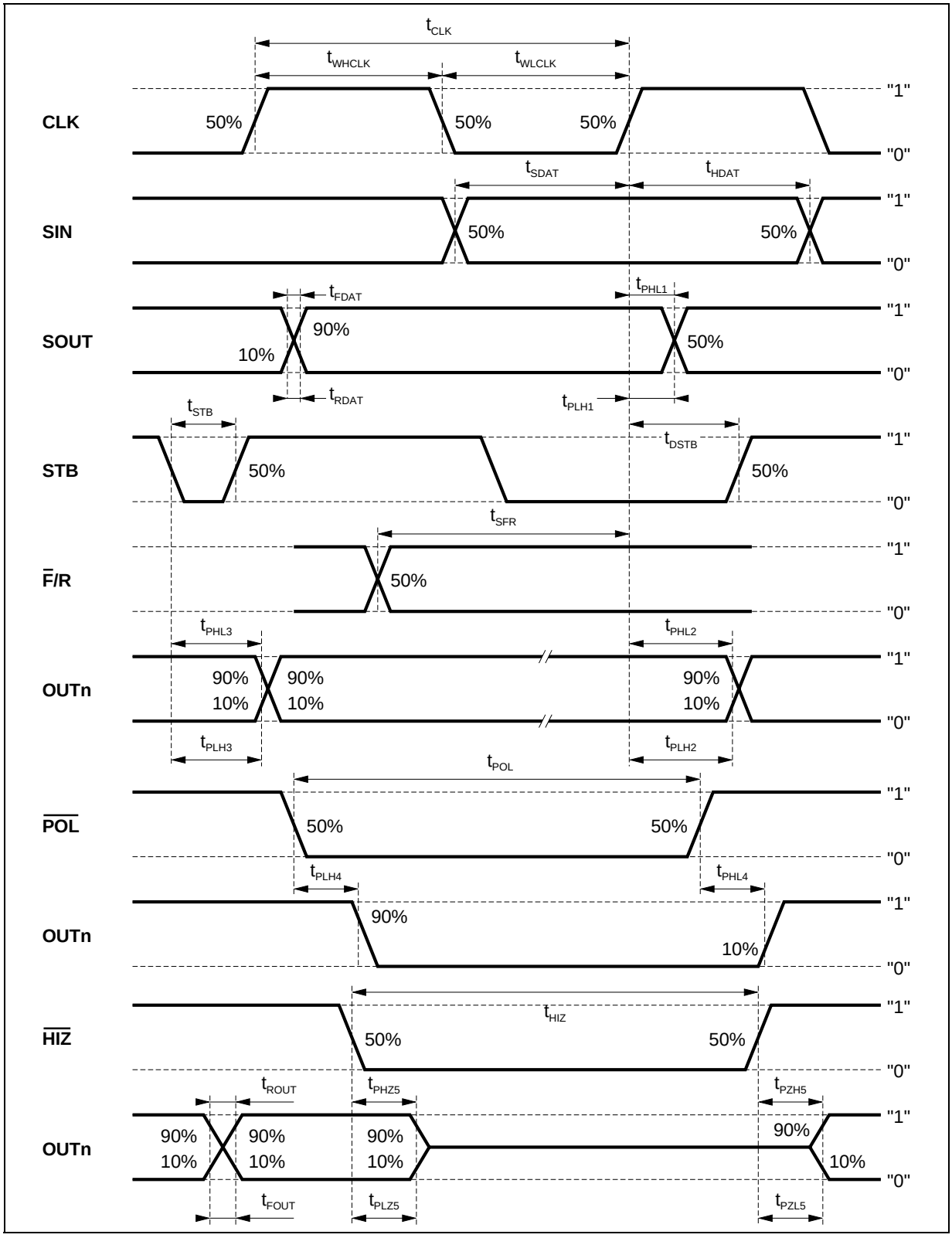
(V_{CC} = 5V, V_{PP} = 65V, V_{SSP} = 0V, V_{SSLOG} = 0V, V_{SSSUB} = 0V, T_{amb} = 25°C, $V_{ILMax.}$ = 0.2V_{CC}, $V_{IHMin.}$ = 0.8V_{CC}, V_{OH} = 4.0V, V_{OL} = 0.4V, C_L = 10pF, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	50	-	-	ns
t_{RDAT}	Logical Data Output Rise Time	-	TBD	30	ns
t_{FDAT}	Logical Data Output Fall Time	-	TBD	30	ns
t_{PHL1} t_{PLH1}	Delay of logic data output (high to low transition) after clock (CLK) transition Delay of logic data output (low to high transition) after clock (CLK) transition	- -	40 40	TBD TBD	ns ns
t_{PHL2} t_{PLH2}	Delay of power output change (high to low transition) after clock (CLK) transition Delay of power output change (low to high transition) after clock (CLK) transition	- -	TBD TBD	120 120	ns ns
t_{PHL3} t_{PLH3}	Delay of power output change (high to low transition) after Latch (STB) transition Delay of power output change (low to high transition) after Latch (STB) transition	- -	TBD TBD	110 110	ns ns
t_{PHL4} t_{PLH4}	Delay of power output change (high to low transition) to Blank ($\overline{BLK}$) or Polarity (POL) transition Delay of power output change (low to high transition) to Blank ($\overline{BLK}$) or Polarity (POL) transition	- -	TBD TBD	100 100	ns ns
t_{PHZ5} t_{PLZ5}	Delay of power output change (high to Hi-Z transition) after high impedance ($\overline{HIZ}$) (5) Delay of power output change (low to Hi-Z transition) after high impedance (HIZ) (5)	- -	TBD TBD	100 100	ns ns
t_{PZH5} t_{PZL5}	Delay of power output change (Hi-Z to high transition) after high impedance ($\overline{HIZ}$) (5) Delay of power output change (Hi-Z to low transition) after high impedance (HIZ) (5)	- -	TBD TBD	100 100	ns ns
t_{ROUT}	Power Output Rise Time (6)	-	-	150	ns
t_{FOUT}	Power Output Fall Time (6)	-	-	150	ns

Notes : 5. See test diagram.
6. One output among 64, loading capacitor C_{OUT} = 50pF, other outputs at low level.

6 - STV7699 SPECIFICATIONS (continued)

Figure 5 : AC Characteristics Waveform



6 - STV7699 SPECIFICATIONS (continued)

6.7 - Input/output Schematics

Figure 6 : $\overline{F}$/R, $\overline{BLK}$, $\overline{POL}$, $\overline{HIZ}$

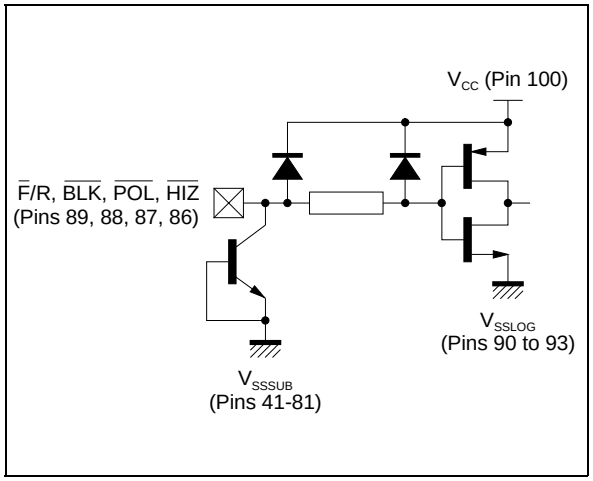


Figure 7 : CLK, STB

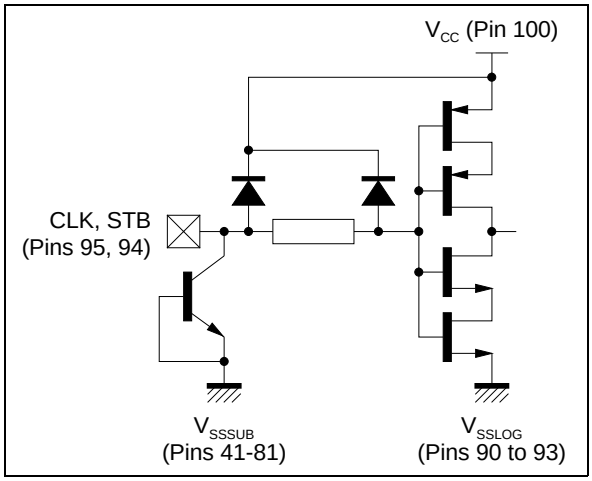


Figure 8 : Ai, Bi

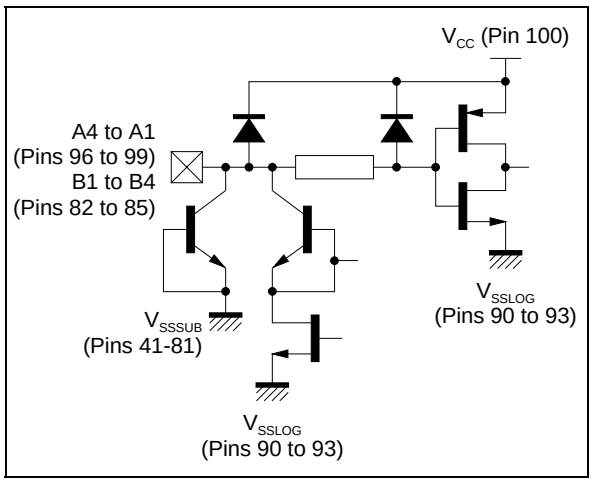


Figure 9 : Power Output