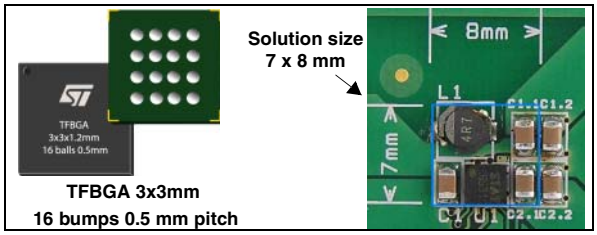
STw4141

Single Coil Dual Output Step Down DC/DC Converter for Digital Base Band and Multimedia Processor Supply

PRELIMINARY DATA

Features

- Single coil dual output switching converter for digital core supply & digital I/Os supply
  - Digital I/O supply:V_{OUT1} @ 200 mA
  - CPU CORE supply:V_{OUT2} @ 400 mA
- Wide range of fixed output voltage configurations available
- High efficiency synchronous step down converter with up to 92 % for the entire device
- Size and cost optimized application board (7x8 mm, height 1.2mm) three capacitors and only one inductor necessary for both outputs
- 2.7 V to 5.5 V battery input range
- ±100mV output voltage accuracy full range in PWM (Including Line and Load Transients)
- 900 kHz fixed frequency PWM operation
- PFM mode operation at light load current
- PWM/PFM switch can be done automatically or forced by setting external pins (AUTO and MODE/SYNC)
- MODE/SYNC input pin for external clock synchronization from 600 kHz to 1.5 MHz
- VSEL input pin for V_{OUT2}/$V_{OUT2(red.)}$ selection
- Ultra low shutdown current (Iq<1 µA)
- Short circuit and thermal shutdown protections



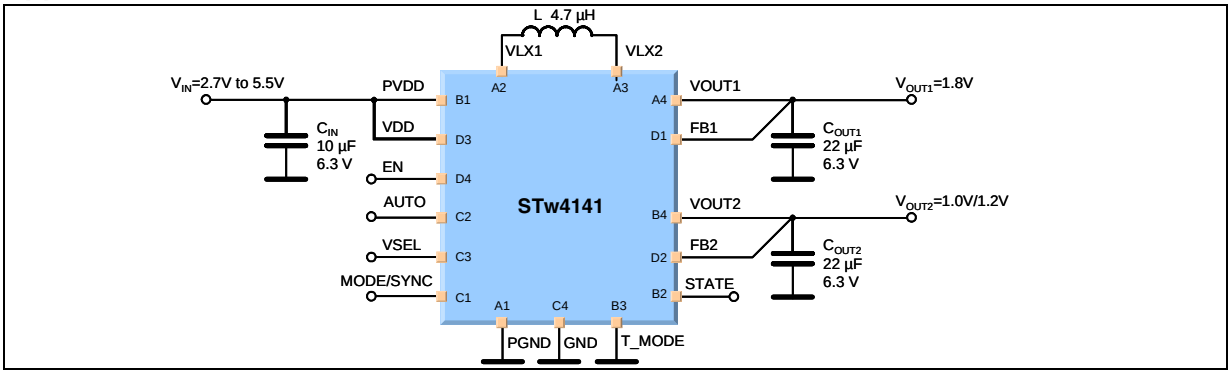
Applications

- Mobile phones
- PDAs and hand held terminals
- Portable media players
- Digital still camera
- WLAN and Bluetooth applications

Description

The STw4141 is a single coil dual output synchronous step down DC/DC converter that requires only four standard external components. It operates at a fixed 900 kHz switching frequency in PWM mode. The device can operate in PFM mode to maintain high efficiency over the full range of output currents.
The STw4141 application requires a very small PCB area and offers a very efficient, accurate, space and cost saving solution to fulfill the requirements of digital baseband or multimedia processor supply (CORE & I/O).

Application Test Circuit



Order Codes

Table 1. STw4141 ordering information

Part number	Package type	Package marking	Output voltage options[1]			Supplied as
			V_{OUT1}[2] (I/O)	V_{OUT2} (CORE)	$V_{OUT2reduced}$ (CORE)	
STw41411	TFBGA 3x3x1.2 16 balls	STA1	1.8 V	1.2 V	1.0 V	Tray
STw41411/T		STA1	1.8 V	1.2 V	1.0 V	Tapes/Reels
STw41412		STA2	1.8 V	1.3 V	1.0 V	Tray
STw41412/T		STA2	1.8 V	1.3 V	1.0 V	Tapes/Reels
STw41413		STA3	1.5 V	1.3 V	1.0 V	Tray
STw41413/T		STA3	1.5 V	1.3 V	1.0 V	Tapes/Reels
STw41414		STA4	1.8 V	1.5 V	1.3 V	Tray
STw41414/T		STA4	1.8 V	1.5 V	1.3 V	Tapes/Reels
STw41415		STA5	1.8 V	1.35 V	1.0 V	Tray
STw41415/T		STA5	1.8 V	1.35 V	1.0 V	Tapes/Reels
STw41416		STA6	1.8 V	1.25 V	1.0 V	Tray
STw41416/T		STA6	1.8 V	1.25 V	1.0 V	Tapes/Reels

1. The output configuration which will be introduced in production will be only those related to customer design-in.
2. $VOUT1 \geq VOUT2$ **THIS CONDITION MUST BE ALWAYS VALID.**

Contents

1 STw4141 Pinout

Figure 1. Pin assignment in TFBGA 3x3 mm - 16 bumps 0.5 mm pitch

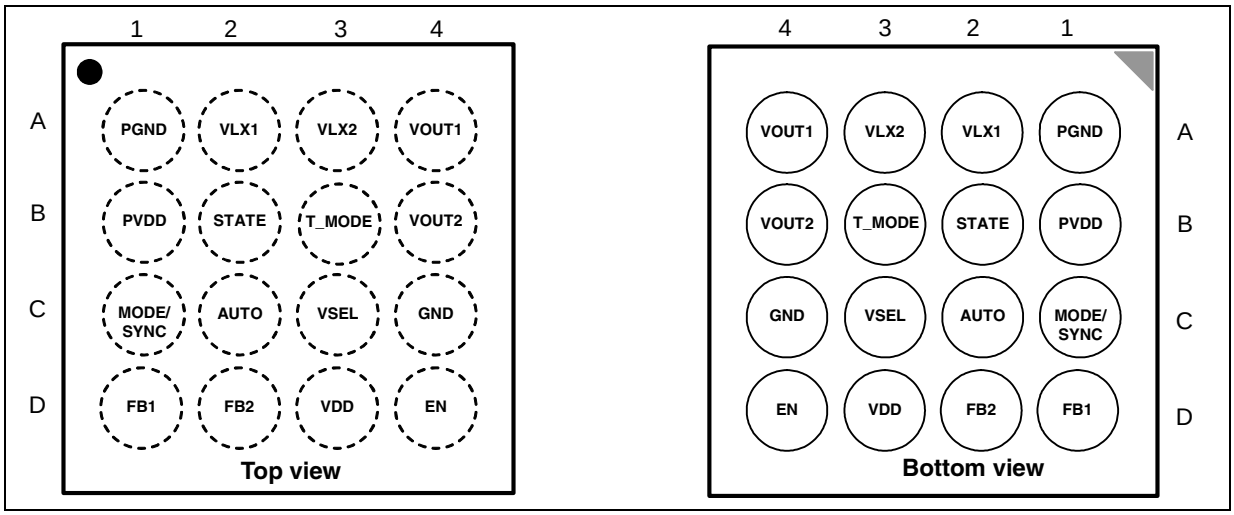


Table 2. STw4141 pin description

Pin	Symbol	Description
A1	PGND	Power ground
B1	PVDD	Power supply voltage
C1	MODE/SYNC	MODE/SYNC = High to forced PWM mode MODE/SYNC = Low to forced PFM mode MODE/SYNC = 600 kHz - 1.5 MHz external clock synchronization in PWM
D1	FB1	Feedback 1
A2	VLX1	External inductor connection pin 1
B2	STATE	Output STATE pin allow the user to monitor operation mode of the product STATE = High - PFM mode STATE = Low - PWM mode If not used must be left unconnected.
C2	AUTO	PWM/PFM automatic switch control pin AUTO = High - PWM/PFM mode automatic switch ENABLED AUTO = Low - PWM/PFM mode automatic switch DISABLED PWM/PFM mode controlled by MODE/SYNC pin)
D2	FB2	Feedback 2
A3	VLX2	External inductor connection pin 2
B3	T_MODE	Input signal for test mode selection. This pin must be connected to GND.
C3	VSEL	Voltage selection input VSEL = High - VOUT1 = 1.8V, VOUT2 = 1.2V (valid for STA1) VSEL = Low - VOUT1 = 1.8V, VOUT2 = 1.0V (valid for STA1) (For other voltage options see *Table 1: STw4141 ordering information*)
D3	VDD	Signal supply voltage
A4	VOUT1	Output voltage 1

Table 2. STw4141 pin description

Pin	Symbol	Description
B4	VOUT2	Output voltage 2
C4	GND	Signal ground
D4	EN	Enable Input: EN = Low - Device in shutdown mode, EN = High - Enable device This pin must be connected either to VDD or GND.

PGND pin This is the ground pin related to power signal. This pin should be connected to the board ground plane by short and wide track or multiply vias to reduce impedance and EMI.

GND pins This is the ground pin related to analog signal.

PVDD pin This pin is designed to provide power to the device. This path leads high currents. It should be wide and short to minimize track impedance to reduce losses and EMI.

VDD pin This pin is designed to provide signal supply voltage to the device. There is no specific requirement for its related track design.

VLX1/VLX2 pins External coil is connected on those pins. It should be placed as closed as possible to the device in order minimize resistances which cause looses. These paths lead high currents.

VOUT1 pin3 It is the first output voltage of this device. This path leads high currents. It should be wide and short to minimize track impedance to reduce losses and EMI.

VOUT2 pin It is the second output voltage of this device. This path leads high currents. It should be wide and short to minimize track impedance to reduce losses and EMI.

FB1 pin Intended to measure VOUT1 voltage in order to ensure the regulation of this output.

FB2 pin Intended to measure VOUT2 voltage in order to ensure the regulation of this output.

ENABLE pin This is the enable pin of the device. Pulling this pin to ground, forces the device into shutdown mode. Pulling this pin to VDD enables the device. This pin must be terminated.

MODE/SYNC pin The MODE/SYNC pin is a multipurpose pin which provides mode selection and frequency synchronization.
The device can also be synchronized to an external clock signal from 600 kHz to 1.5 MHz by the MODE/SYNC pin. During synchronization, the mode is forced to PWM mode and the top switch turn-on is synchronized to the rising edge of the external clock.

AUTO pin This pin allows the device to automatically switch from PWM to PFM mode following load on both 2 outputs.

STATE pin This output pin informs user in which state the device is working: PWM or PFM mode.

VSEL pin This pin is used to reduce V_{OUT2} (CORE) output voltage in order to reduce the processor power consumption when entering into sleep mode.

2 Electrical Characteristics

2.1 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PV_{DD}	Power Supply Voltage	-0.3 to 6	V
V_{DD}	Signal Supply Voltage	-0.3 to 6	V
V_{EN}	Enable Input	-0.3 to V_{DD}	V
V_{SEL}	Voltage Selection	-0.3 to V_{DD}	V
$V_{MODE/SYNC}$	Operating Mode Selection/Synchronization Input	-0.3 to V_{DD}	V
V_{AUTO}	PWM/PFM automatic switch selection	-0.3 to V_{DD}	V
V_{T_MODE}	Test mode selection	-0.3 to V_{DD}	V
V_{STATE}	Operating mode information	-0.3 to V_{OUT1}	V
V_{OUT1},FB_1	Output Voltage 1, Feedback 1	-0.3 to 3.3	V
$V_{OUT2,}$ FB_2	Output Voltage 2, Feedback 2	-0.3 to 3.3	V
VLX_1	External Inductor Connection Pin 1	-0.3 to V_{DD}	V
VLX_2	External Inductor Connection Pin 2	-0.3 to 3.3	V
T_A	Operating Temperature Range	-40 to 85	°C
T_J	Maximum Operating Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance Junction-Ambient TFBGA 3x3 mm – 16 bumps - 0.5 mm pitch	150	°C/W

2.3 DC electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise is noted. All typical values are referred to T_A = 25°C, PVDD = 3.6V, VDD = 3.6V.

Table 5. DC electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
PVDD	Power supply voltage		2.7		5.5	V
I_{LIM}	Peak current limit			1.6		A
V_{OUT1}(1)	Output voltage 1(2)		-3		+3	%
V_{OUT2}	Output voltage 2(2)	VSEL = VDD, MODE/SYNC = VDD	-3		+3	%
	Output voltage 2(2)	VSEL = GND, MODE/SYNC = VDD	-3		+3	%
I_{OUT1}	Output current 1				200	mA
I_{OUT2}	Output current 2				400	mA
I_q	Quiescent Current (PWM)	I_{OUT1} = 0 mA, I_{OUT2} = 0 mA EN = VDD, VSEL = VDD MODE/SYNC = VDD, AUTO = GND		600		µA
	Quiescent Current (PFM)	I_{OUT1} = 0 mA, I_{OUT2} = 0 mA EN = VDD, VSEL = VDD MODE/SYNC = GND, AUTO = GND		90		µA
	Shutdown Current	EN = GND, VSEL = GND MODE/SYNC = GND, AUTO = GND		1	5	µA
Enable functions						
$V_{EN}H$	Enable Threshold High		0.9			V
$V_{EN}L$	Enable Threshold Low				0.4	V
Mode/sync functions						
$V_{M/S}H$	MODE/SYNC Threshold High		0.9			V
$V_{M/S}L$	MODE/SYNC Threshold Low				0.4	V
VSEL functions						
$V_{SEL}H$	Voltage Selection Threshold High		0.9			V
$V_{SEL}L$	Voltage Selection Threshold Low				0.4	V

Table 5. DC electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Auto functions						
$V_{AUTO}H$	Voltage Selection Threshold High		0.9			V
$V_{AUTO}L$	Voltage Selection Threshold Low				0.4	V
State functions						
$V_{STATE}H$	Voltage Selection Threshold High	R_{Lmax} = 100k, C_{Lmax} = 10pF	$0.7V_{OUT1}$			V
$V_{STATE}L$	Voltage Selection Threshold Low	R_{Lmax} = 100k, C_{Lmax} = 10pF			$0.3\ V_{OUT1}$	V

1. $VOUT1 \geq VOUT2$. This condition must always be valid.
2. Output voltage accuracy excludes line and load transients

2.4 Dynamic electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise is noted. All typical values are referred to T_A = 25°C, PVDD = 3.6V, VDD = 3.6V.

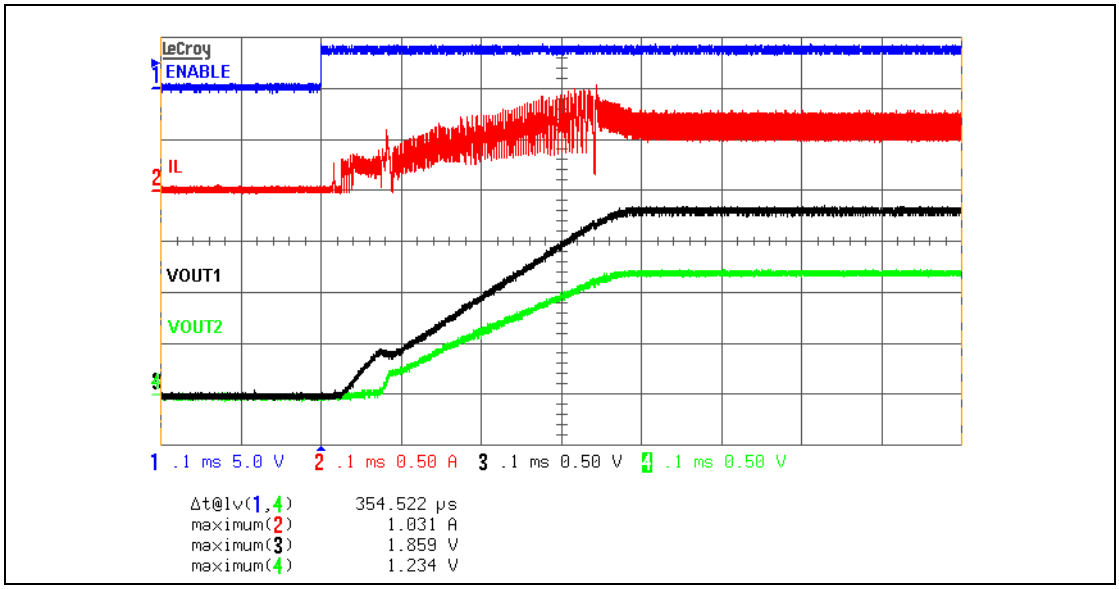
Table 6. Dynamic electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
f_{SW}	Switching frequency			900		kHz
f_{SYNC}	Sync mode frequency		600		1500	kHz
Ts	Settling time (soft start)			400		µs
TS2	Settling time V_{OUT2} (reduced)/V_{OUT2}	VSEL change from GND to VDD		80		µs

2.5 Soft start

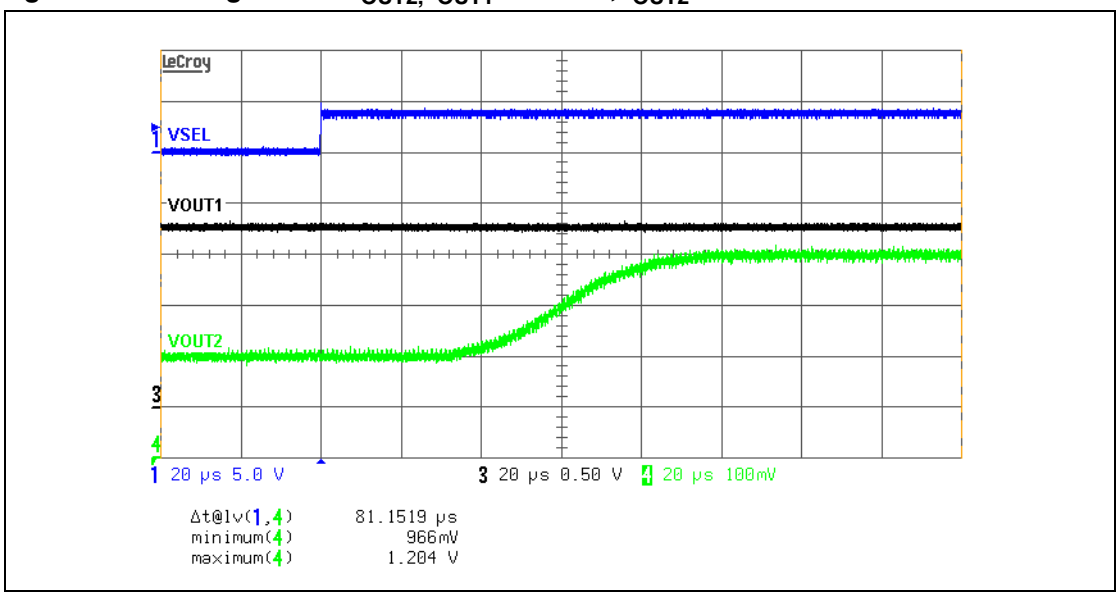
To avoid spikes on battery during STw4141 start-up sequence, a smooth start-up is implemented. Reference voltage grows up less than 600 µs until it achieves is final target. Therefore, STw4141 start up is smooth and secure for the overall mobile phone.

Figure 2. Smooth start-up sequence V_{IN} = 3.6V, V_{OUT1} = 1.8V@ 200mA, V_{OUT2} =1.2V@400mA



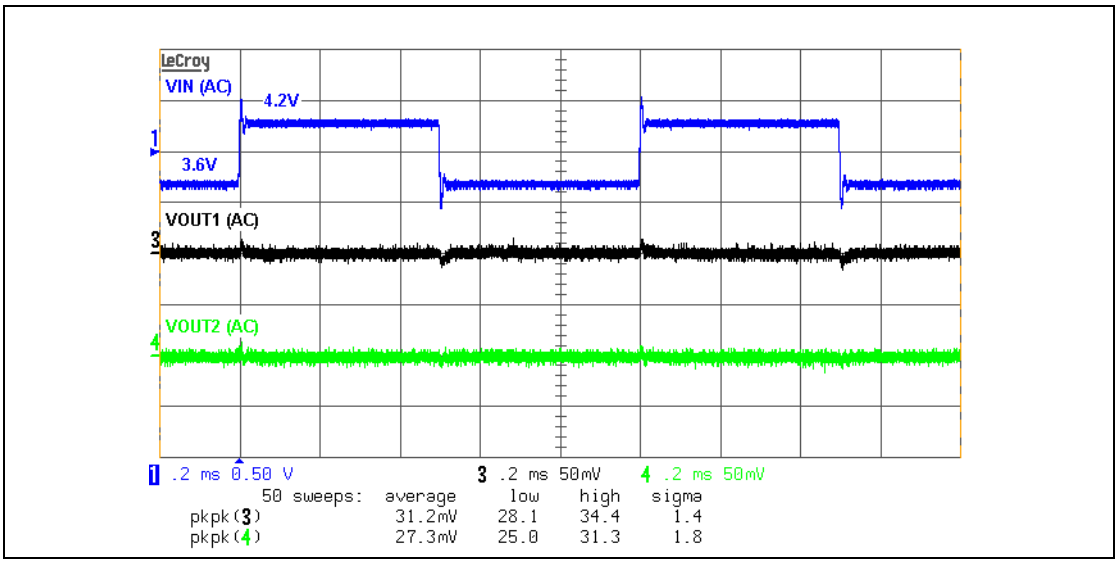
2.6 Settling time of V_{OUT2}

Figure 3. Settling time of V_{OUT2}, I_{OUT1} = 200mA, I_{OUT2} = 400mA



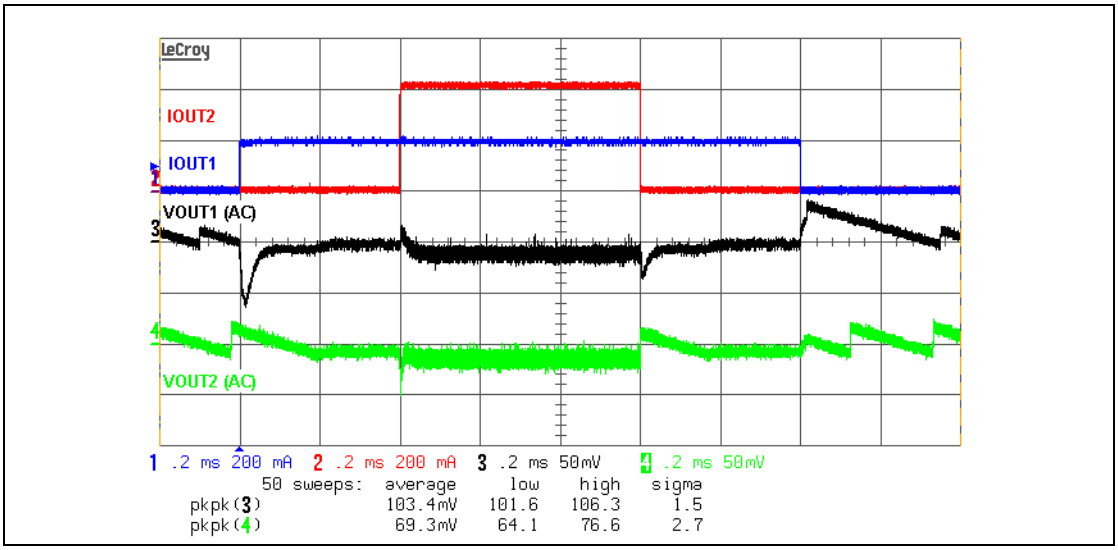
2.7 Line transients

Figure 4. Line transient, V_{OUT1} = 1.8V @ 100mA, V_{OUT2} = 1.2V @ 100mA



2.8 Load transients in AUTO mode

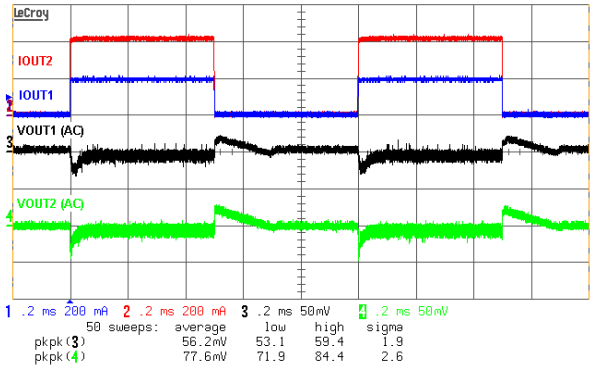
Figure 5. Load transient in AUTO mode V_{IN} = 3.6V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V



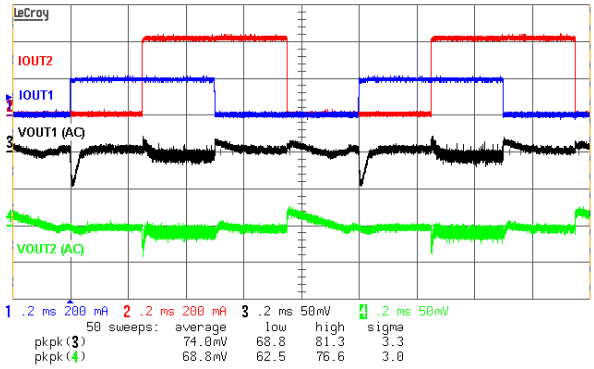
2.9 Load transients in PWM mode

Figure 6: Load transient in PWM mode, I_{OUT1} = 1mA to 200mA, I_{OUT2} = 1mA to 400mA

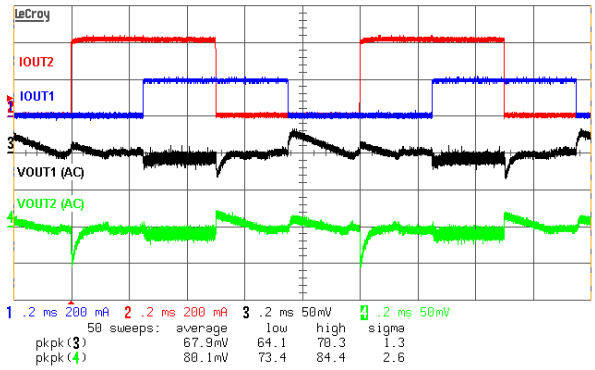
Load transient related to in-phase switching
V_{IN} = 3.6V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V



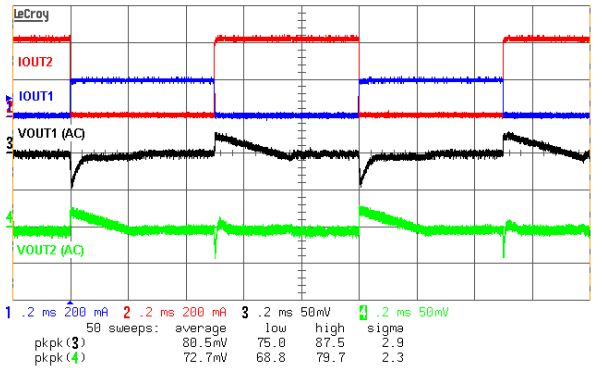
Load transient output 1 leading output 2
V_{IN} = 3.6V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V



Load transient output 2 leading output 1
V_{IN} = 3.6V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V



Load transient related to anti-phase switching
V_{IN} = 3.6V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V



2.10 Switching between PFM and PWM in FORCED MODE

Figure 7. Switching between PFM to PWM operation modes V_{IN} = 3.6V, I_{OUT1} = 10mA, I_{OUT2} = 10mA

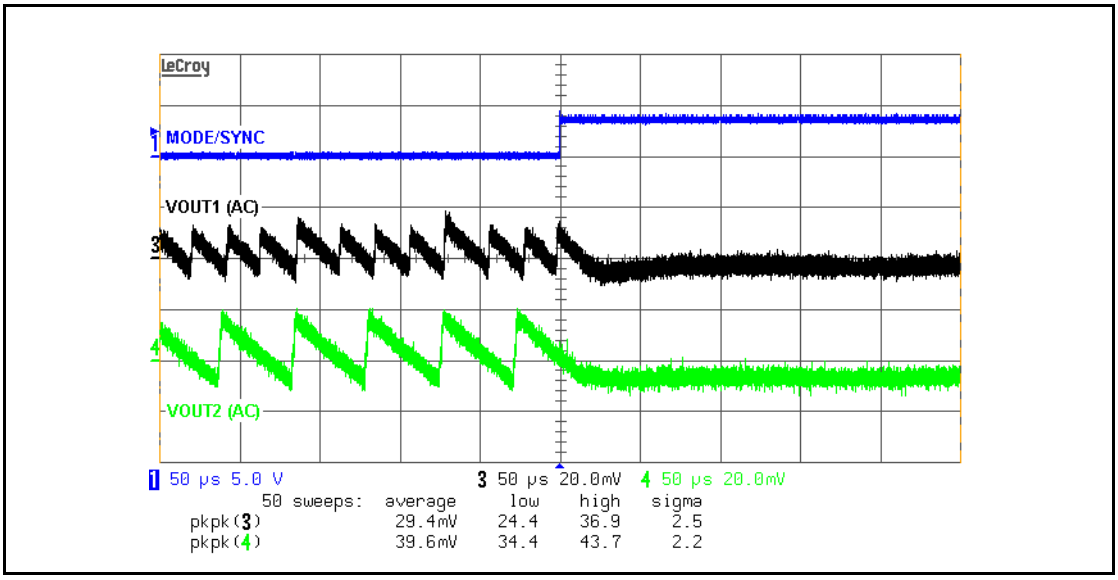
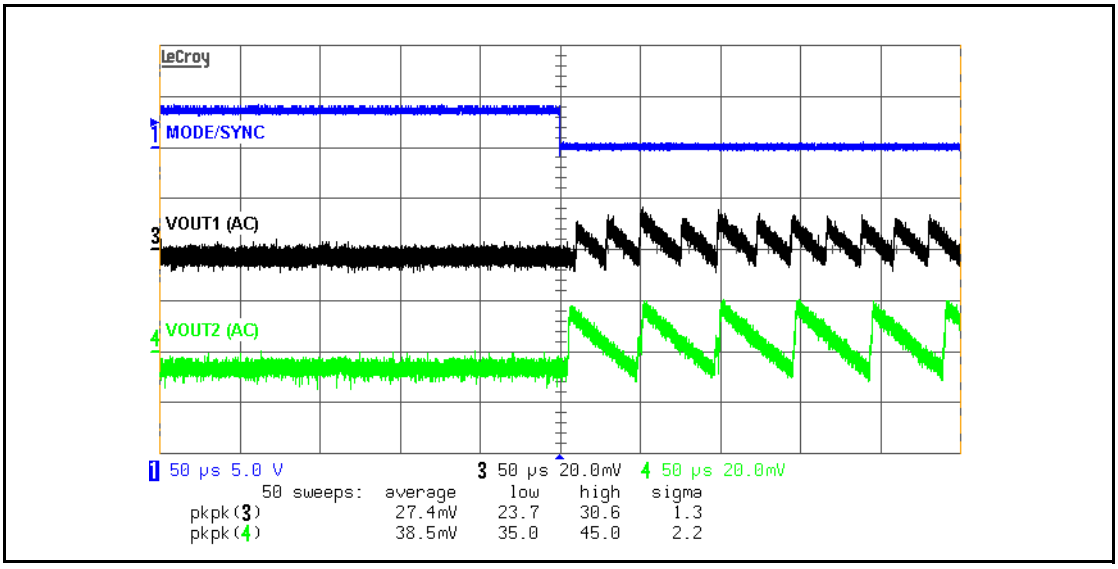


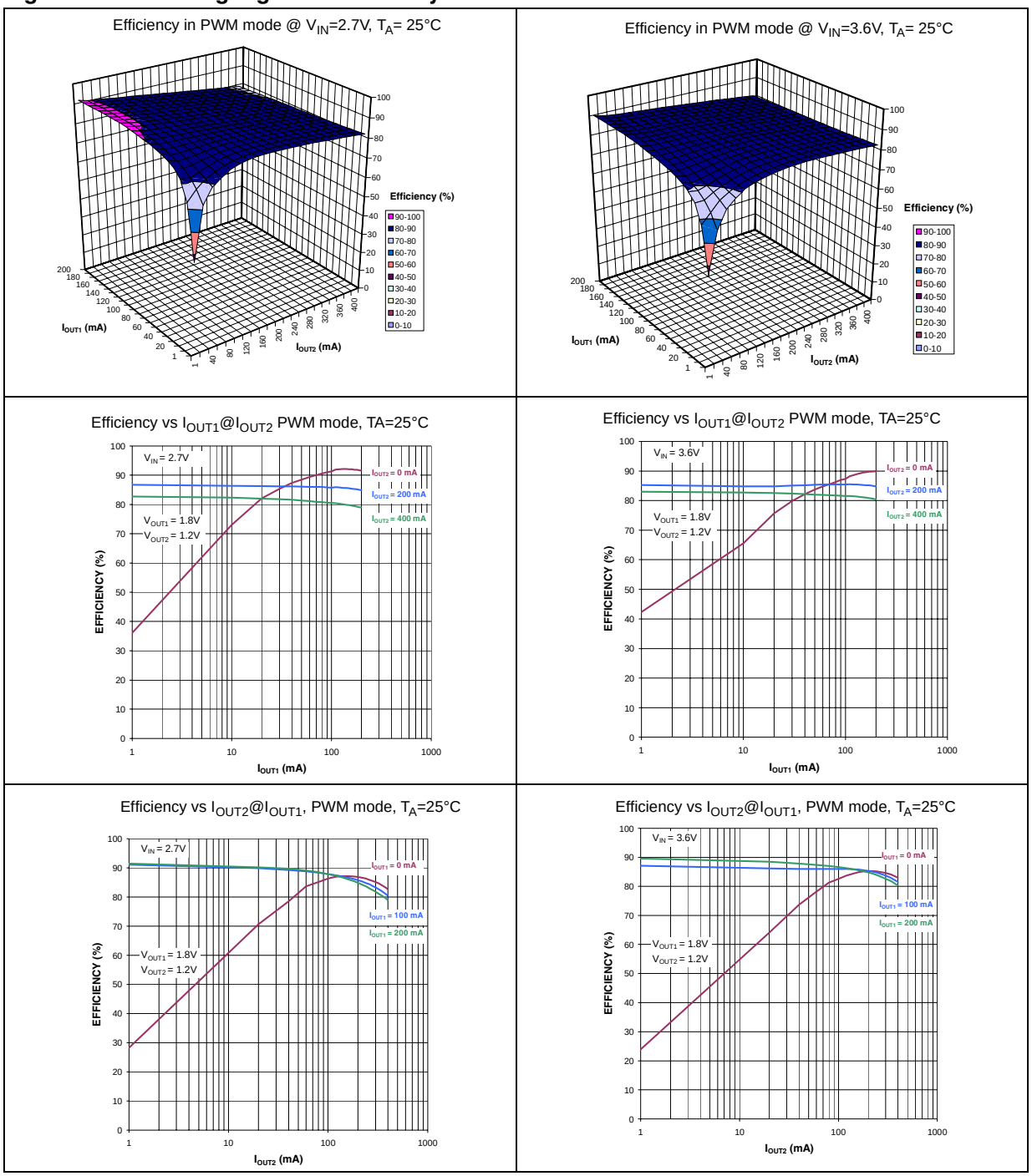
Figure 8. Switching between PWM to PFM operation modes V_{IN} = 3.6V, I_{OUT1} = 10mA, I_{OUT2} = 10mA



2.11 Efficiency in PWM

The efficiency of a switching regulator is equal to the total output power divided by the input. STw4141 has high efficiency up to 92% (for the 2 outputs). Efficiency curve is flat over the output current range.

Figure 9. Switching regulator efficiency in PWM mode

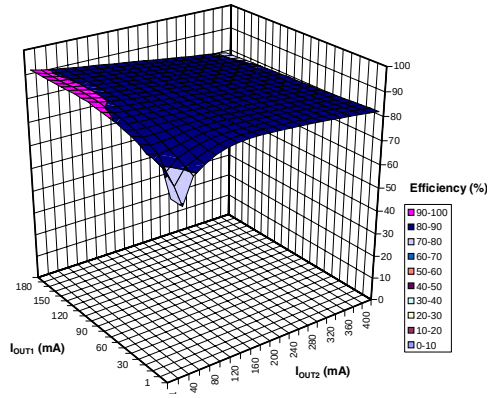


2.12 Efficiency in AUTO

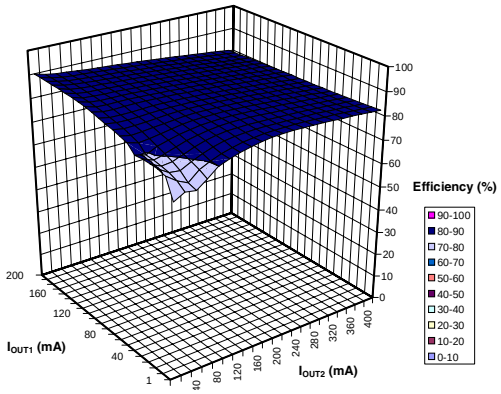
The efficiency of a switching regulator is equal to the total output power divided by the input. STw4141 has high efficiency up to 92% (both outputs) and always higher than 70% for output currents higher than 1mA.

Figure 10. Switching regulator efficiency in auto mode

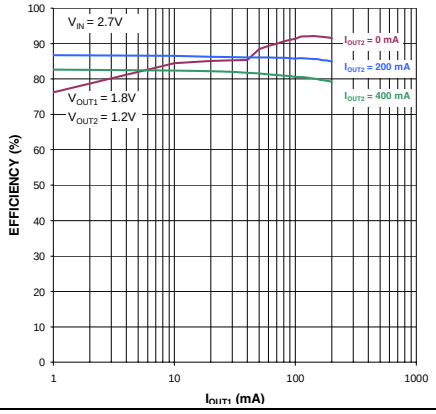
Efficiency VS output currents I_{OUT1} and I_{OUT2}, V_{IN} = 2.7V, AUTO mode



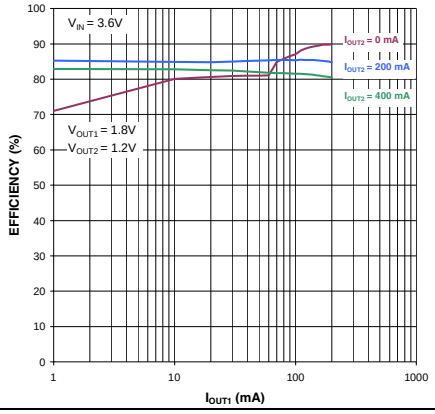
Efficiency VS output currents I_{OUT1} and I_{OUT2}, V_{IN} = 3.6V, AUTO mode



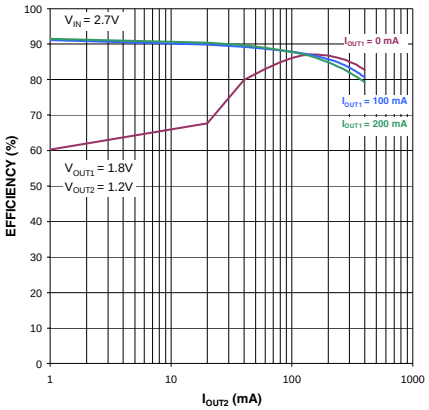
Efficiency VS I_{OUT1}@I_{OUT2}, AUTO mode, T_A = 25°C



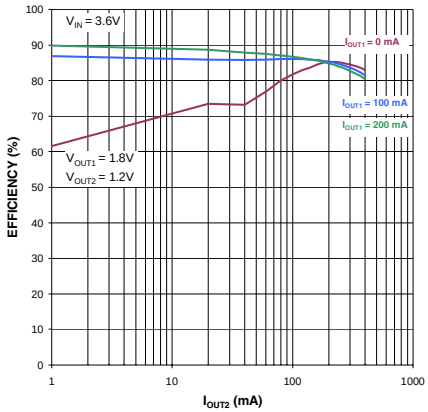
Efficiency VS IOUT1@I_{OUT2}, AUTO mode, T_A = 25°C



Efficiency VS I_{OUT2}@I_{OUT1}, AUTO mode, T_A = 25°C

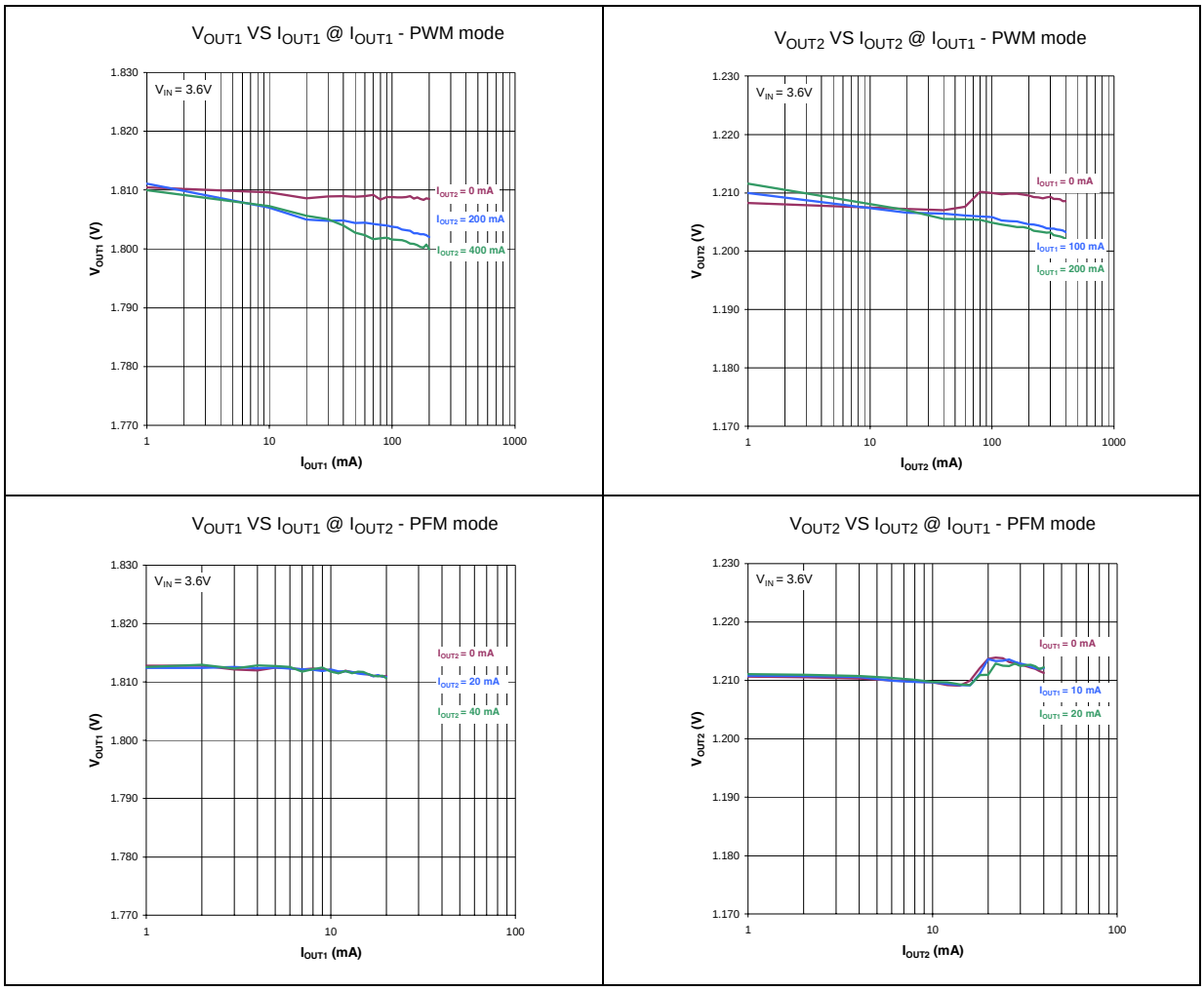


Efficiency VS I_{OUT2}@I_{OUT1}, AUTO mode, T_A = 25°C



2.13 Output voltages versus output currents in PWM and PFM

Figure 11. Output voltages versus output currents in PWM and PFM



3 Functional Description

3.1 Introduction

The STw4141 is an easy to use, single coil dual outputs step down DC/DC converter optimized to supply low-voltage to CPUs or DSPs in cell phones and other miniature devices powered by single cell lithium-ion or 3 cell NiMH/NiCd batteries. It provides two different output voltages with high efficiency operation in a wide range of output currents. The device offers high DC voltage regulation accuracy and load transient response to satisfy demanding processor core supply. The converter is based on voltage mode buck architecture using PWM and PFM operation modes.

At light load currents, the device can operate in PFM mode to maintain high efficiency over the entire load current range. Switching between PWM and PFM modes can be done automatically or can be forced by external pins (AUTO and MODE/SYNC). Externally synchronized or fixed frequency (internal oscillator) PWM mode offers full output current capability while minimizing interference to sensitive RF and data acquisition circuits.

3.2 PWM and PFM mode operation

PWM (Pulse Width Modulation) mode is intended for normal load to high load currents. Energy is delivered to the load with an accurate and defined frequency of 900 kHz.
PFM (Pulse Frequency Modulation) mode is intended for low load currents to maintain high efficiency conversion.

Forced mode: When AUTO pin is LOW, the operating mode is selectable by the user itself. It means that system controls the behavior of the STw4141 according to processor needs. STw4141 is switched from PWM to PFM mode using MODE/SYNC pin (refer to *User mode details*" section).

Automatic PWM / PFM switch: When AUTO pin is HIGH, the operating mode is directly controlled by internal digital circuit according to processor needs. The device switches from PWM to PFM by itself if sum of output currents is lower than approximately 100 mA during at least 16 clock cycles. The device can be forced to PWM mode connecting MODE/SYNC to HIGH level. (see *Section 2.8* and *Section 2.9*).

3.3 Current limiter

This protection limits the current flowing through coil. As soon as ILIM is detected, the duty cycle is terminated and prevents the coil current against rising above peak current limit. There is no reset of device.

3.4 Short circuit protection

It protects the device against short-circuit at output terminals. When one or both output voltages are decreased by 0.7 V below their nominal output values the device enters into reset followed by soft start sequence.

3.5 Thermal shutdown protection

Thermal shutdown protects the device against damage due to overheating when maximum operating junction temperature is exceeded. The device is kept in reset until junction temperature decreases by 25°C approximately.

4 Application information

4.1 User mode details

The following table describes the different user modes available. Depending on the application constraints (processor I/O pins available) and expected efficiency, PWM or PFM mode are forced or automatically controlled by STw4141 internal digital gates.

Table 7. STw4141 available user modes

Mode	User mode / pins	EN	AUTO	MODE/ SYNC
OFF	Shutdown	L	X	X
FORCED	Forced PFM	H	L	L
	Forced PWM	H	L	H
	Forced PWM and synchronized external clock	H	L	CLK
AUTO	Auto mode	H	H	L
	Forced PWM	H	H	H
	Forced PWM and synchronized external clock	H	H	CLK

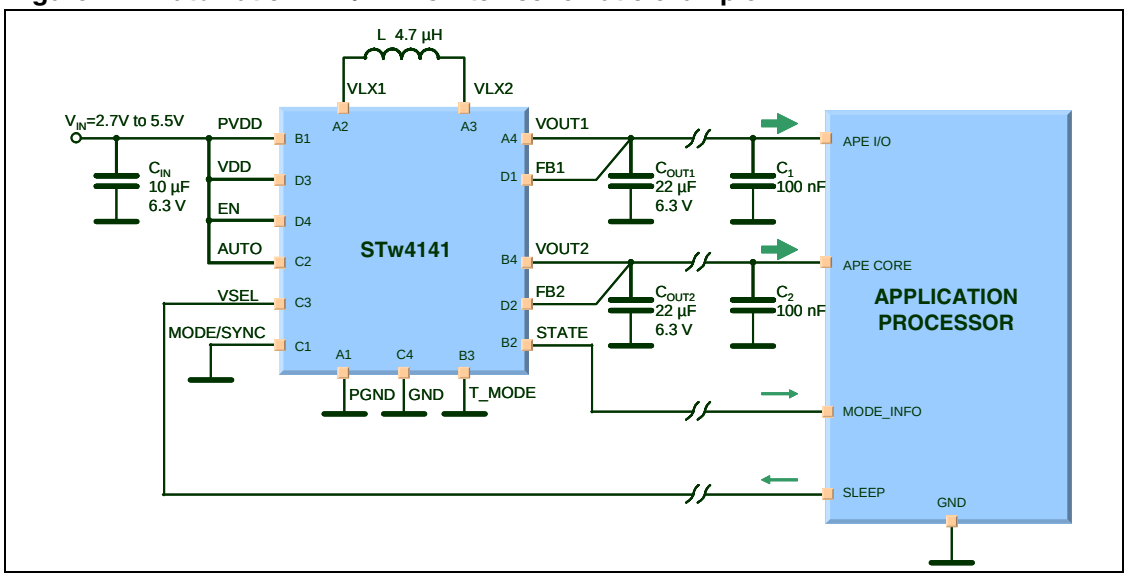
Table 8. Operating mode information (STATE pin - digital output)

Operation mode	State pin voltage level
PFM	VOUT1
PWM	GND

4.2 Automatic PWM/PFM mode

This user mode is designed to allow STw4141 to switch automatically between PWM and PFM modes. This feature improves the application efficiency because STw4141 enters in PFM mode according to application processor current consumption.

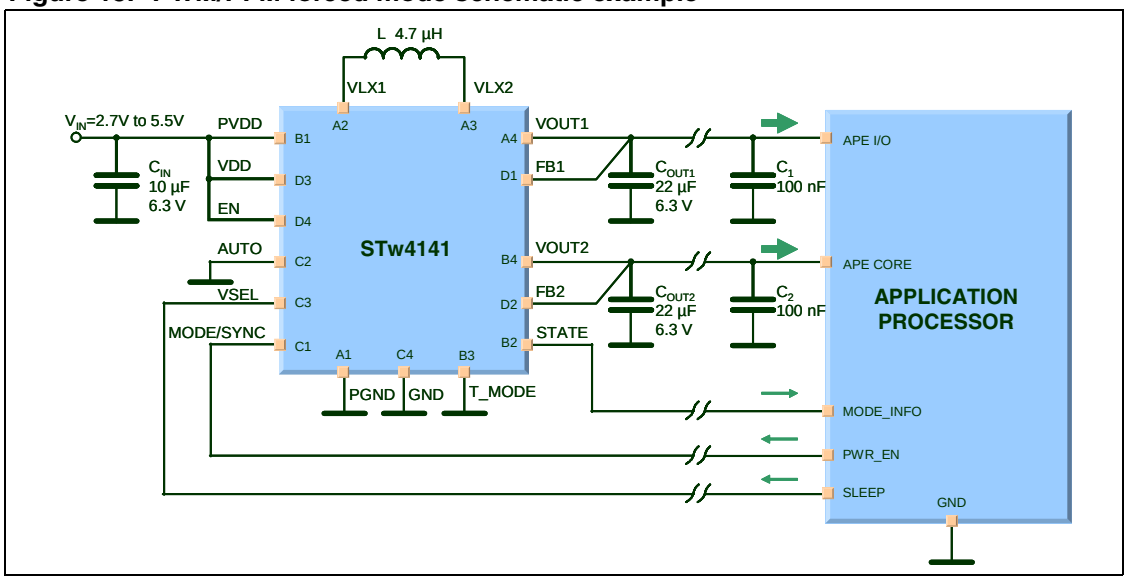
Figure 12. Automatic PWM/PFM switch schematic example



4.3 User selected PWM/PFM mode

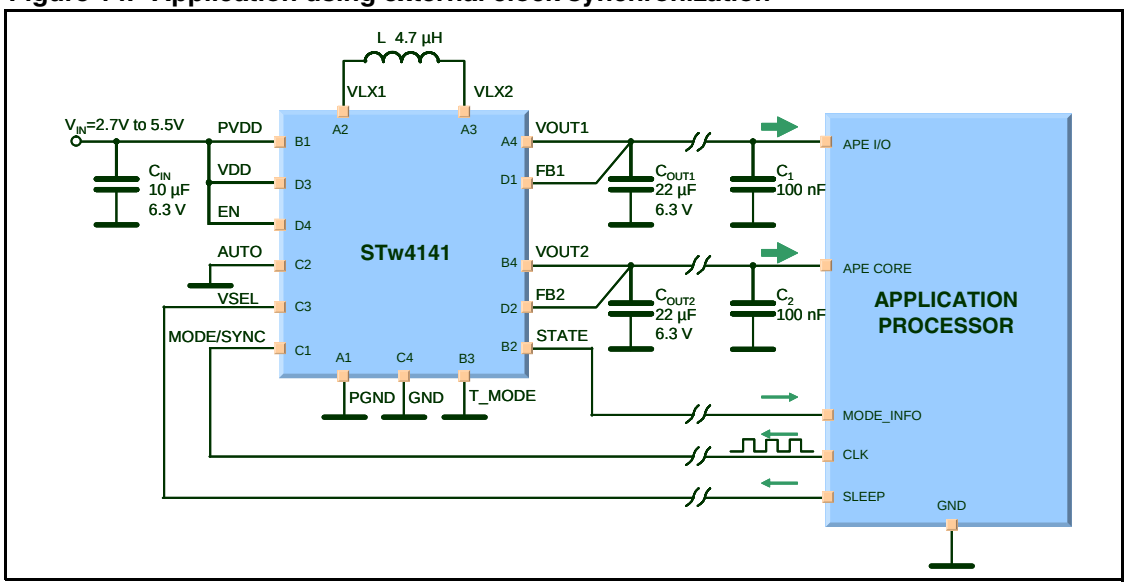
STw4141 PWM/PFM mode can also be controlled by the application processor. This feature is accessible through MODE/SYNC pin state. It is useful to users who want to use STw4141 with the modem digital processor. Therefore, MODE/SYNC pin is connected to SLEEP mobile phone signal.

Figure 13. PWM/PFM forced mode schematic example



4.4 External clock synchronization

Figure 14. Application using external clock synchronization



4.5 Checking Transient response versus external components

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} is immediately shifted by an amount equal to I_{LOAD} x ESR, where ESR is the equivalent series resistance of C_{OUT}. I_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. In order to improve the transient response, it is better to use two 10 µF ceramic capacitors on each output to reduce ESR.

4.6 Bill of Material

4.6.1 Inductor selection

The choice of which inductor to use depends on the price and size versus performance required with the STw4141 application. *Table 9* shows some typical surface mount inductors that work well in STw4141 applications.

Table 9. Bill of material: inductor selection

Part number	Supplier	Value (µH)	DCR (max)	Max DC current (mA)	Size (mm) W x L x H
VFL4012A-4R7M1R1	TDK	4.7	0.14	1100	3.5 x 3.7 x 1.2
VFL3012A-4R7MR74	TDK	4.7	0.16	740	2.6 x 2.8 x 1.2
744031004	WUERTH	4.7	0.085	900	3.8 x 3.8 x 1.8

4.6.2 Input capacitor (CIN selection)

Input capacitor of 10 µF ceramic low ESR capacitor should be used to reduce switching losses. It should be placed as close as possible to supply pins VDD and PVDD. The connection traces should be wide and short to minimize impedance.

4.6.3 Output capacitors (COUT selection)

The selection of COUT is driven by the required ESR to minimize voltage ripple and load step transients. There are two possibilities for output capacitors: either a 22 µF is connected to ground or two 10 µF ceramic are used to reduce ESR and switching losses. The capacitor should be placed as close as possible to V_{OUTx} pins. The connection traces should be wide and short to minimize impedance.

4.6.4 Capacitors selection

Table 10. Bill of Material: capacitor selection

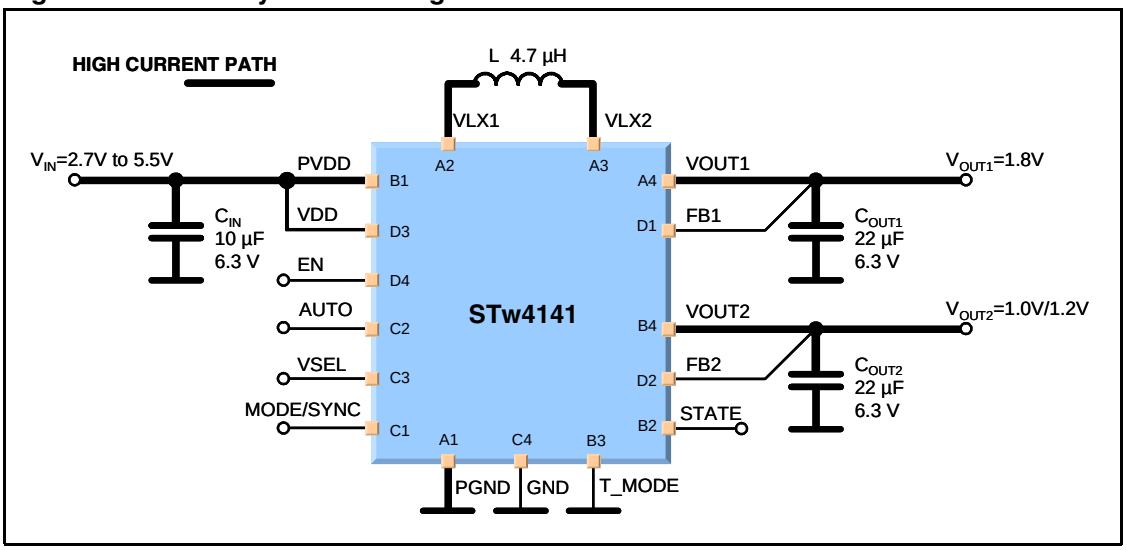
Component	Supplier	Part number	Value	Case size
C_{IN}	TDK	C1608X5R0J106MT	10 µF, 6.3V	0603
	TDK	C2012X5R0J106MT	10 µF, 6.3V	0805
	TAIYO YUDEN	JMK212BJ106MG-T	10 µF, 6.3V	0805
C_{OUT1}, C_{OUT2}	TDK	C1608X5R0J106MT	2 x 10 µF, 6.3V	2 x 0603
		C2012X5R0J106MT	2 x 10 µF, 6.3V	2 x 0805
		C2012X5R0J226MT	22 µF, 6.3V	0805
	TAIYO YUDEN	JMK212BJ106MG-T	2 x 10 µF, 6.3V	2 x 0805
		JMK212BJ226MG-T	22 µF, 6.3V	0805

4.7 PCB layout considerations

The Printed Circuit Board layout must include the following consideration:
Current paths carrying high currents (bold lines in *Figure 15*) must be wide and short to minimize impedance in order to reduce looses and EMI.

Small currents flow through voltage paths. No specific care is requested about voltage paths but it is recommended to follow the general rules for PCB routing to reduce influence of external and internal interferences.

Figure 15. Board layout track length and width



4.7.1 PCB layout

Figure 16 and *Figure 17* show the PCB layout. All components are on the top side of the board.

Figure 16. Demoboard top layer

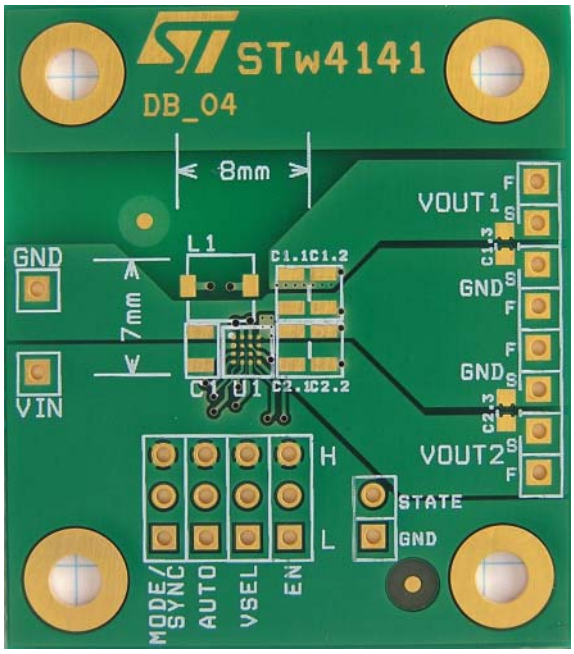
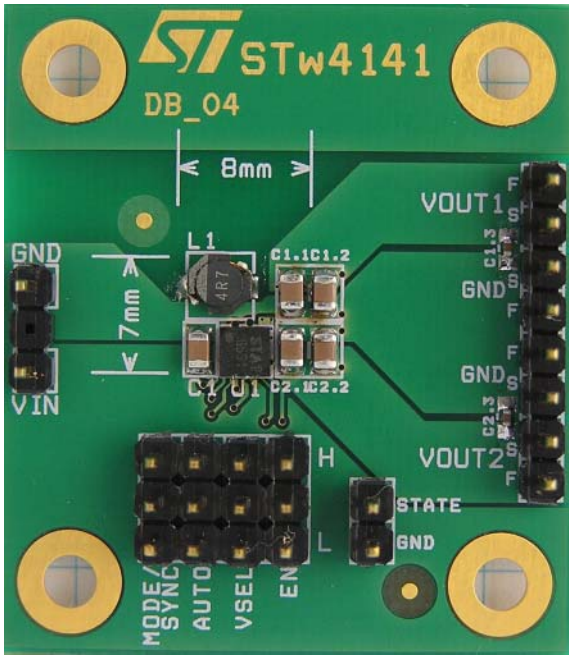


Figure 17. Demoboard assembled with 2x10µF output capacitors



4.7.2 TFBGA16 internal bumps access

Pad centers are at 500 µm distance. Pad diameter is 275 µm. The distance between two adjacent pad edges is only 225 µm. We recommend a distance for lead-out signals from the center of pad matrix by 75 µm wide trace. Isolation distance in this case is 75 µm (see *Figure 18* and *Figure 19*).

Figure 18. TFBGA16 ball pad spacing and track parameters to internal pads

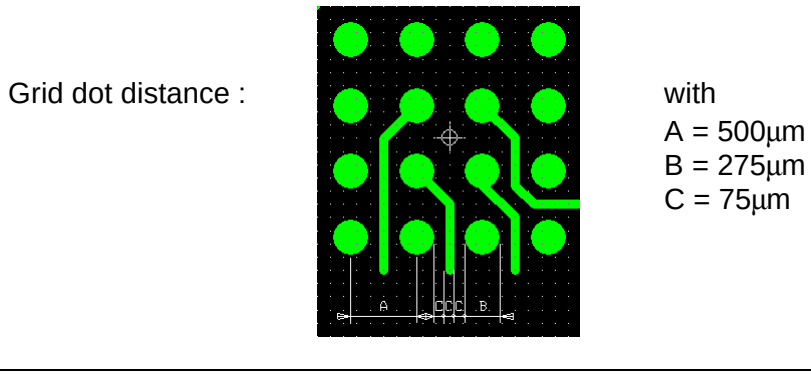
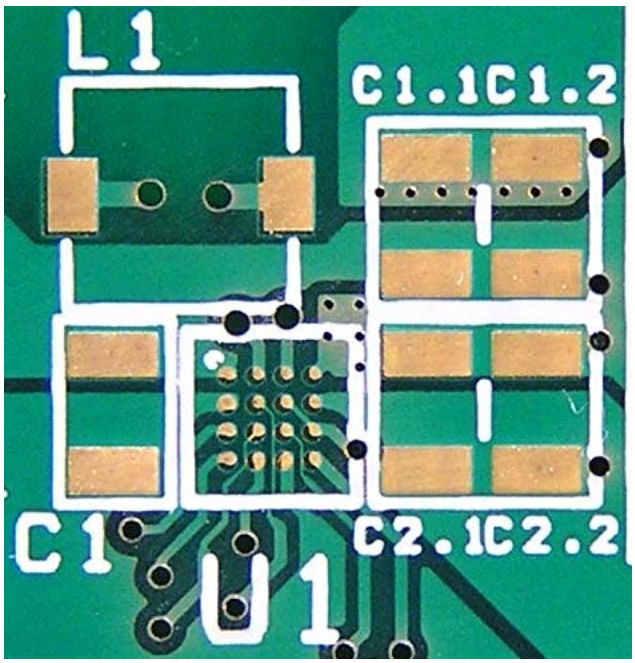


Figure 19. PCB routing example using TFBGA16



5 Package Outline and Mechanical Data

Table 11: TFBGA 3x3x1.20 16 F4x4 0.50. Package code: L0 - JEDEC/EAIJ reference number: N/A

Ref	Min.	Typ.	Max.
A	1.01		1.20 (*Note 1*)
A1	0.15		
A2		0.82	
b	0.25	0.30	0.35
D	2.85	3.00	3.15
D1		1.50	
E	2.85	3.00	3.15
E1		1.50	
e		0.50	
ddd	0.85		0.08
eee			0.15
fff			0.05

Note: 1 Max mounted height is 1.12 mm. Based on a 0.28 mm ball pad diameter.
Solder paste is 0.15 mm thickness and 0.28 mm diameter.

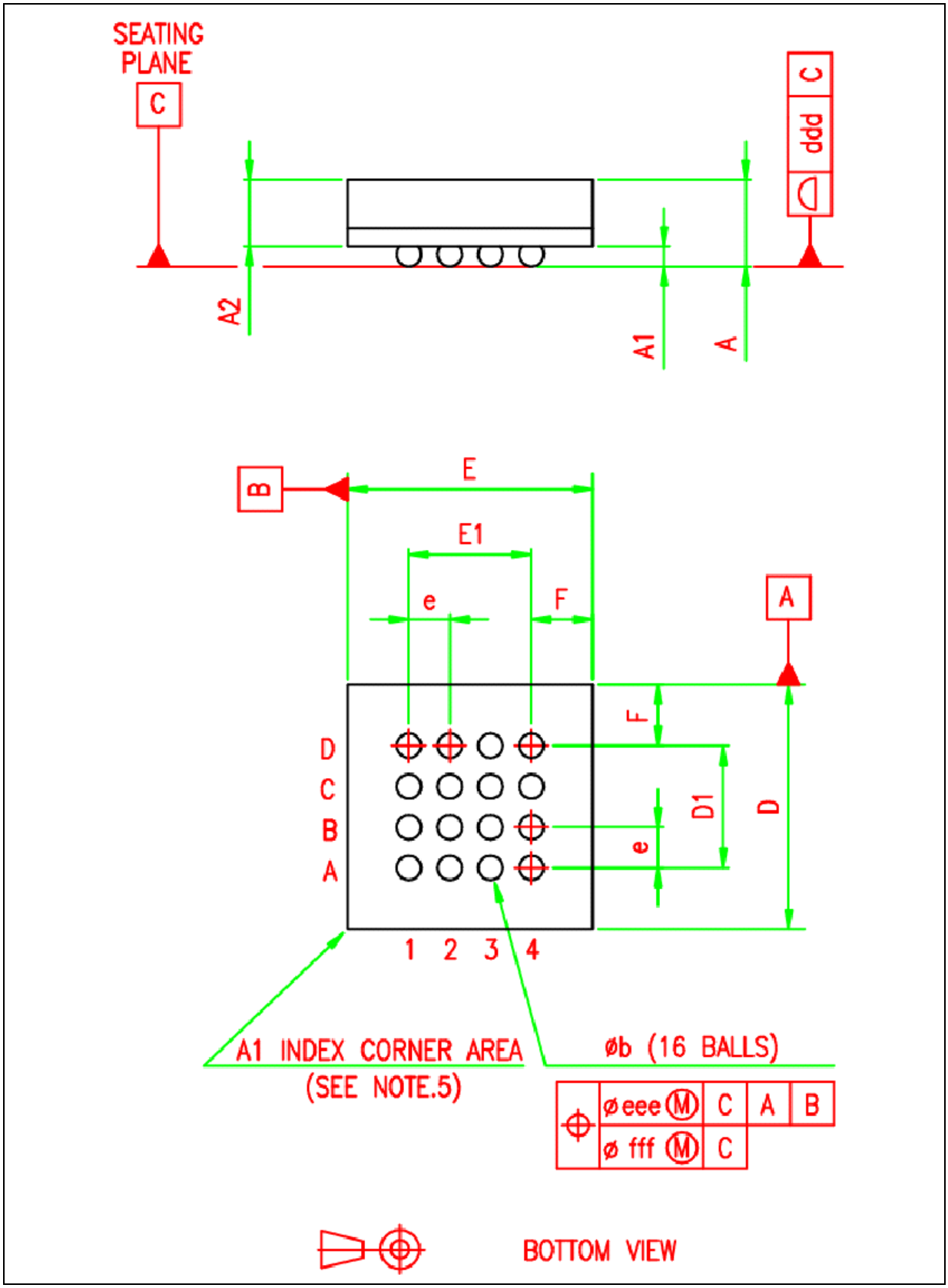
*2 TFBGA stands for **T**hin **P**rofile **F**ine Pitch **B**all **G**rid **A**rray.*
Thin profile: The total profile height (DIm A) is measured from the seating plane to the top of the component.
A = 1.01 to 1.20 mm
Fine pitch < 1.00 mm pitch.

3 The tolerance of position that controls the location of the pattern of balls with respect to datums A and B.
For each ball there is a cylindral tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

4 The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within the tolerance zone.
Each tolerance zone fff in the array is contained entirely in the respective above eee zone above.
The axis of each ball must be simultaneously in both tolerance zones.

5 Leadfree package according to JEDEC JESD-020-C

Figure 20. TFBGA 3x3x1.20 16 F4x4 0.50



6 Revision history

Date	Revision	Changes
8-Dec-2005	1	Initial release