STw5095

Low Power Asynchronous Stereo Audio Codec with Integrated Power Amplifiers

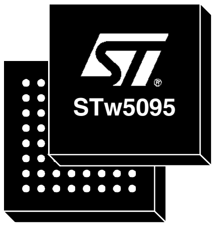
PRELIMINARY DATA

Features

- 20 bit audio resolution, 8kHz to 96kHz independent rate ADC and DAC
- Asynchronous sampling ADC and DAC: they do not require oversampled clock and information on the audio data sampling frequency (fs). Jitter tolerant fs
- Wide master clock range: from 4MHz to 32MHz
- I^2C/SPI compatible control I/F
- Stereo headphones drivers, handsfree loudspeaker driver, line out drivers
- Mixable analog line inputs
- Voice filters: 8/16kHz with voice channel filters
- Automatic gain control for microphone and line-in inputs
- Two programmable master/slave serial audio data interfaces (I^2S, SPI, PCM compatible and other formats)
- Frequency programmable clock outputs
- Multibit ΣΔ modulators with data weighted averaging ADC and DAC
- DSP functions for bass-treble-volume control, mute, mono/stereo selection, voice channel filters, de-emphasis filter and dynamic compression.
- 93 dB dynamic range ADC, 0.001% THD with full scale output @ 2.7V
- 95 dB dynamic range DAC, 0.02% THD performance @ 2.7V over 16Ω load

Analog inputs

- Selectable stereo differential or single-ended microphone amplifier inputs with 51dB range programmable gain
- One microphone biasing output
- Microphone plug-in and push-button detection input



TFBGA64 5x5 (64 pins)

- Selectable stereo differential or single-ended line inputs with 38 dB range programmable gain

Analog output drivers

- Stereo headphones outputs driving capability: 40 mW (0.1% THD) over 16Ω with 40 dB range programmable gain
- Common mode voltage headphones driver (phantom ground)
- Balanced loudspeaker output driving capability: up to 500mW (V_{CCLS}>3.5V; 1% THD) over 8Ω with 30dB range programmable gain
- Transient supression filter during power up and power down
- Balanced/unbalanced stereo line outputs driving capability 1kΩ

Applications

- Digital cellular telephones with mp3 player, stereo recorder, fm radio stereo listening and recording functions, live music recording
- Portable digital players and recorders

Description

STw5095 is a low power asynchronous stereo audio CODEC device with headphones amplifiers for high quality audio listening and recording.

The STw5095 control registers are accessed through a selectable I^2C-bus compatible or SPI compatible interface.

The STw5095 asynchronous stereo audio CODEC is designed to easily fit in most audio systems because it supports an extended master clock range (any value between 4 MHz and 32 MHz) and at the same time it supports any audio data rate (independent in AD and DA paths) from 8 kHz to 48 kHz and from 88 kHz to 96 kHz, moreover it can tolerate jitter on audio data without degrading performance. The audio data serial interfaces (for AD and DA) can be Master or Slave, are I^2S compatible and they support other formats that can easily interface to standard serial ports. The two audio interfaces can be used as a single bidirectional interface. Two frequency programmable clock sources are available to generate the master clock for the audio sub-system of other devices. The internal D to A and A to D converters work with up to 24 bit resolution.

The supply voltage can be the same for the whole device, in the range 2.4 V to 2.7 V, or it can be differentiated for digital (V_{CC}: 1.8 V to 2.7 V), analog (V_{CCA}: 2.4 V to 3.3 V) and loudspeaker driver (V_{CCLS}: V_{CCA} to 5.5 V) to obtain best performance and maximum power to the loudspeaker (up to 500 mW).

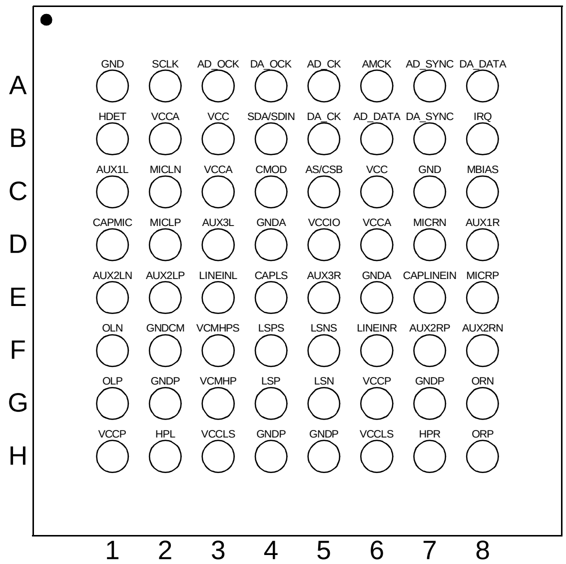
STw5095 has multiple analog mixable inputs and outputs. It can directly drive Stereo Headphones without external capacitors and it has a Loudspeaker driver that can also be used for monophonic group listening. Stereo differential and single ended microphones, auxiliary line in stereo and mono signals can be mixed and connected to the ADC or directly to the drivers, mixed also with DAC audio signals.

STw5095 stereo audio Codec main applications include multimedia handheld devices such as cellular phones with added low-power high-quality MP3 and⁄ or FM radio listening/recording features, or any battery powered equipment such as PDAs, Camcorders, etc. that require Stereo Audio Codec with Headphones drivers.

Ordering codes

Part Number	Details
STw5095	TFBGA 64 Tray
STw5095T	TFBGA 64 Tape and Reel

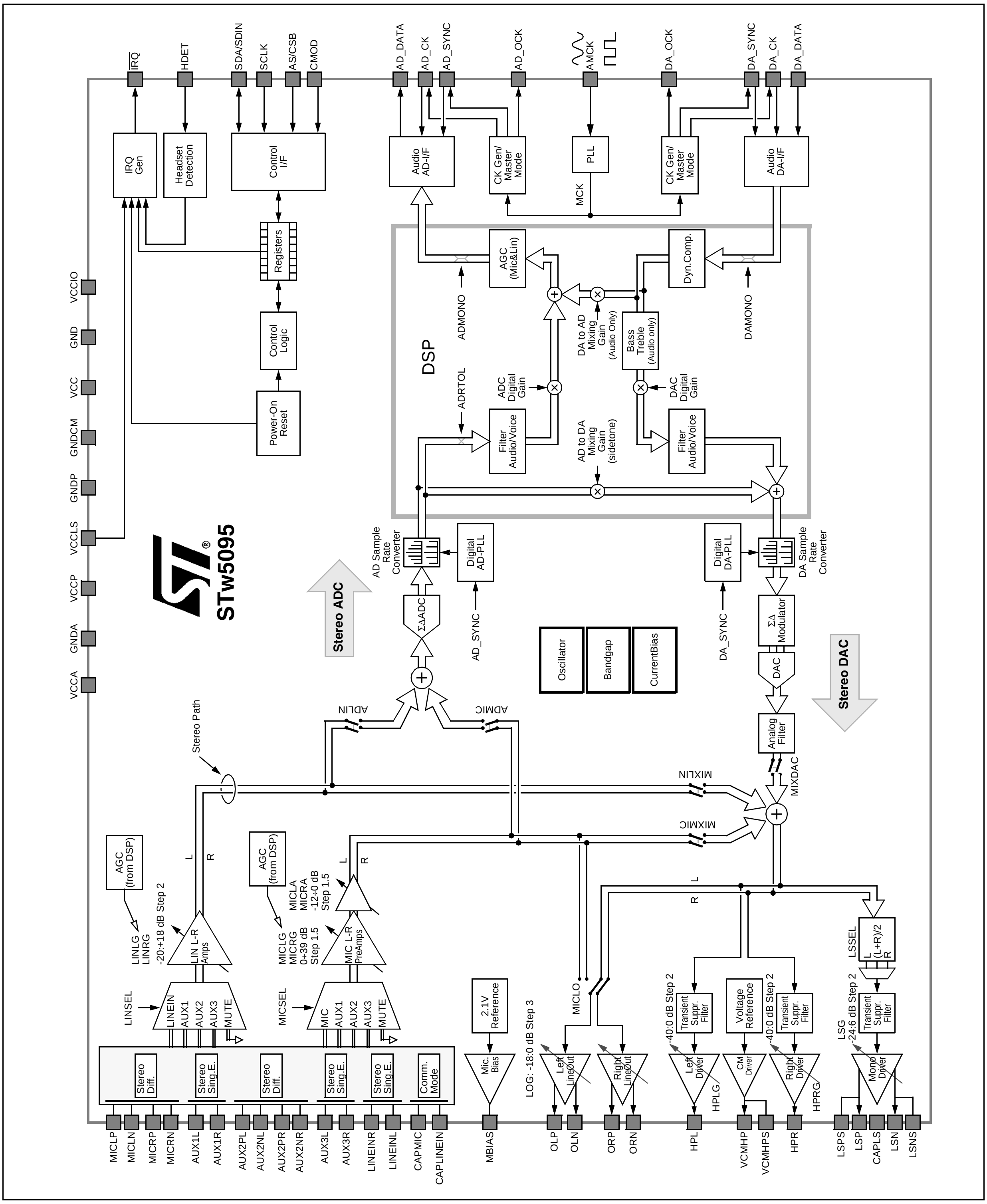
Pin configuration (top view)



Contents

1 Functional Block Diagram

Figure 1. STw5095 block diagram



Note: This diagram shows the functionality of the device and of some control registers bits but it does not necessarily reflect the exact hardware implementation.

2 Pin Description

Table 1. Pin description

Pin N°	Name	Type	Description
D2 C2 E8 D7	MICLP MICLN MICRP MICRN	AI	Left and Right channel differential pins for microphone input.
C8	MBIAS	AO	Microphone Biasing Pin. Fixed voltage reference.
D1	CAPMIC	AI	A capacitor must be connected between CAPMIC and Ground.
C1 D8	AUX1L AUX1R	AI	Left and Right channel single ended pins for microphone or line input.
E2 E1 F7 F8	AUX2LP AUX2LN AUX2RP AUX2RN	AI	Left and Right channel differential pins for microphone or line input.
D3 E5	AUX3L AUX3R	AI	Left and Right channel single ended pins for microphone or line input.
E3 F6	LINEINL LINEINR	AI	Left and Right channel single ended pins for line input.
E7	CAPLINEIN	AI	A capacitor must be connected between CAPLINEIN and Ground.
G4 G5	LSP, LSN	AO	Analog differential loudspeaker amplifier output for Left channel or Right channel or the sum of both. This output can drive 50nF (with series resistor) or directly an earpiece transducer of 8Ω ; It can deliver up to 500mW.
F4 F5	LSPS, LSNS	AO	LSPS, LSNS (sense) pins must be connected on the application board to LSP, LSN pins respectively (see application note). The connection must be as close as possible to the pins.
E4	CAPLS	AI	A capacitor can be connected between this node and Ground. See application notes
H2 H7	HPL HPR	AO	Audio single ended headphones amplifier outputs for Left and Right channels. The outputs can drive 50nF (with series resistor) or directly an earpiece transducer of 16Ω
G3	VCMHP	AO	Common mode voltage headphones output. The negative pins of headphones left and right speakers can be connected to this pin to avoid decoupling capacitors.
F3	VCMHPS	AO	VCMHPS (sense) pin must be connected on the application board to VCMHP pin (see application note). The connection must be as close as possible to the pins.
G1 F1 H8 G8	OLP OLN ORP ORN	AO	Audio differential line out amplifier for Left and Right channels. This outputs can drive up to 1kΩ resistive load. Can be used as single ended outputs.

Table 1. Pin description

Pin N°	Name	Type	Description
C4	CMOD	DI	Control interface type selector: I^2C-bus mode or SPI mode.
A2	SCLK	DI	Control interface serial clock input.
B4	SDA/SDIN	DIOD	Control interface serial data input-output in I^2C mode (SDA), Control interface serial data input in SPI mode (SDIN).
C5	AS/CSB	DI	Control interface address select in I^2C mode (AS). Interface enable signal in SPI mode (CSB).
A7	AD_SYNC	DIO	Frame Sync for stereo A/D converter.
B7	DA_SYNC	DIO	Frame Sync for stereo D/A converter.
A5	AD_CK	DIO	Serial Data Clock for stereo A/D converter.
B5	DA_CK	DIO	Serial Data Clock for stereo D/A converter.
B6	AD_DATA	DO	Serial Data Out for stereo A/D converter.
A8	DA_DATA	DI	Serial Data In for stereo D/A converter.
B1	HDET	AI	Headset detection input (Microphone Plug-in and Push-Button detection).
B8	IRQ	DO	Programmable Interrupt output. Active low signal.
A3	AD_OCK	DO	Oversampled Clock Out from AD clock generator.
A4	DA_OCK	DO	Oversampled Clock Out from DA clock generator.
A6	AMCK	DI AI	Master Clock Input. Accepted range 4 MHz to 32 MHz. AMCK is a Digital square wave AMCK is an Analog sinewave (see AMCKSIN *Section 4.8 on page 36*)
B2 C3 D6	VCCA	P	Power Supply pins for the analog section. Standard Operating range: from 2.7 V to 3.3 V Low Voltage (LV) Range: from 2.4 V to 2.7 V
D4 E6	GNDA	P	Ground pins for the analog section.
F2	GNDCM	P	Ground pin for analog reference. GNDCM can be connected to GNDA.
G6 H1	VCCP	P	Power Supply pins for the left and right output drivers (headphones and line-out). Operating range: from V_{CCA} to 3.3V
H3 H6	VCCLS	P	Power Supply pins for the mono differential output driver. Operating range: from V_{CCA} to 5.5V
G2 G7 H4 H5	GNDP	P	Ground pins for the left, right and mono-differential output drivers. GNDP and GNDA must be connected together.
B3 C6	VCC	P	Power Supply pins for the digital section. Operating range: from 1.71 V to 2.7 V

Table 1. Pin description

Pin N°	Name	Type	Description
A1 C7	GND	P	Ground pins for the digital section.
D5	VCCIO	P	Power Supply pin for the Digital I/O buffers. Operating ranges: from 1.2 V to 1.8 V and from 1.71 V to V_{CC}

Note: VCC, VCCA, VCCP, VCCLS can be connected together for low cost applications: Operating range: 2.4 V-2.7 V.

Type definitions

AI	-	Analog input
AO	-	Analog Output
AIO	-	Analog Input Output
DI	-	Digital Input
DO	-	Digital output
DIO	-	Digital Input Output
DIOD	-	Digital Input Output Open Drain
P	-	Power Supply or Ground

3 Functional Description

3.1 Power supply

STw5095 can have different supply voltages for different blocks, to optimize performance, power consumption and connectivity. See *Operative supply voltage on page 50* for voltage definition.

The correct sequence to apply supply voltage is to set first (and unset last) the digital I/O supply (V_{CCIO}). The other supply voltages can be set in any order and can be disconnected individually, if needed. Disconnection does not cause any harm to the device and no extra current is pulled from any supply during this operation. Moreover if a voltage conflict is detected, like $V_{CCA} < V_{CC}$ (not allowed), simply all blocks connected to V_{CCA} are set to power down and no extra current is pulled from supply.

When V_{CCIO} is set and V_{CC} (digital supply) is not set, all the digital output pins are in high impedance state, while the digital inputs are disconnected to avoid power consumption for any input voltage value between GND and V_{CCIO}. Before V_{CC} is disconnected the device has to be reset (SWRES bit in CR30).

When the analog supply (V_{CCA}) is set and V_{CC} is not set, all the analog inputs are in high impedance state.

The control registers are powered by VCC pin (digital supply) so if this pin is disconnected all the information stored in control registers is lost. When the digital supply voltage is set, a power-on-reset (POR) circuit sets all the registers content to the default value and then generates an IRQ signal writing 1 in bits PORMSK and POREV in CR31 and CR32 respectively.

All supplies must be on during operation.

3.2 Device programming

STw5095 can be programmed by writing Control Registers with SPI or I^2C compatible control interface (both slave). The interface is always active, there is no need to have the master clock running to program the device registers.

The choice between the two interfaces is done via an input pin (CMOD):

1. CMOD connected to GND: I^2C compatible mode selected
   The device address is selected with AS pin:

AS connected to GND:	chip address 001101**0**1(35hex) for reading, 001101**0**0 (34hex) for writing
AS connected to V_{CCIO}:	chip address 001101**1**1(37hex) for reading, 001101**1**0 (36hex) for writing

   When this mode is selected control registers are accessed through pins:
   SCLK (clock)
   SDA (serial data out/in, open drain)
2. CMOD connected to V_{CCIO}: SPI compatible mode selected
   When this mode is selected control registers are accessed through:
   CSB (chip select, active low)
   SCLK (clock)
   SDIN (serial data in)
   AD_OCK or DA_OCK or IRQ (serial data out, if selected)

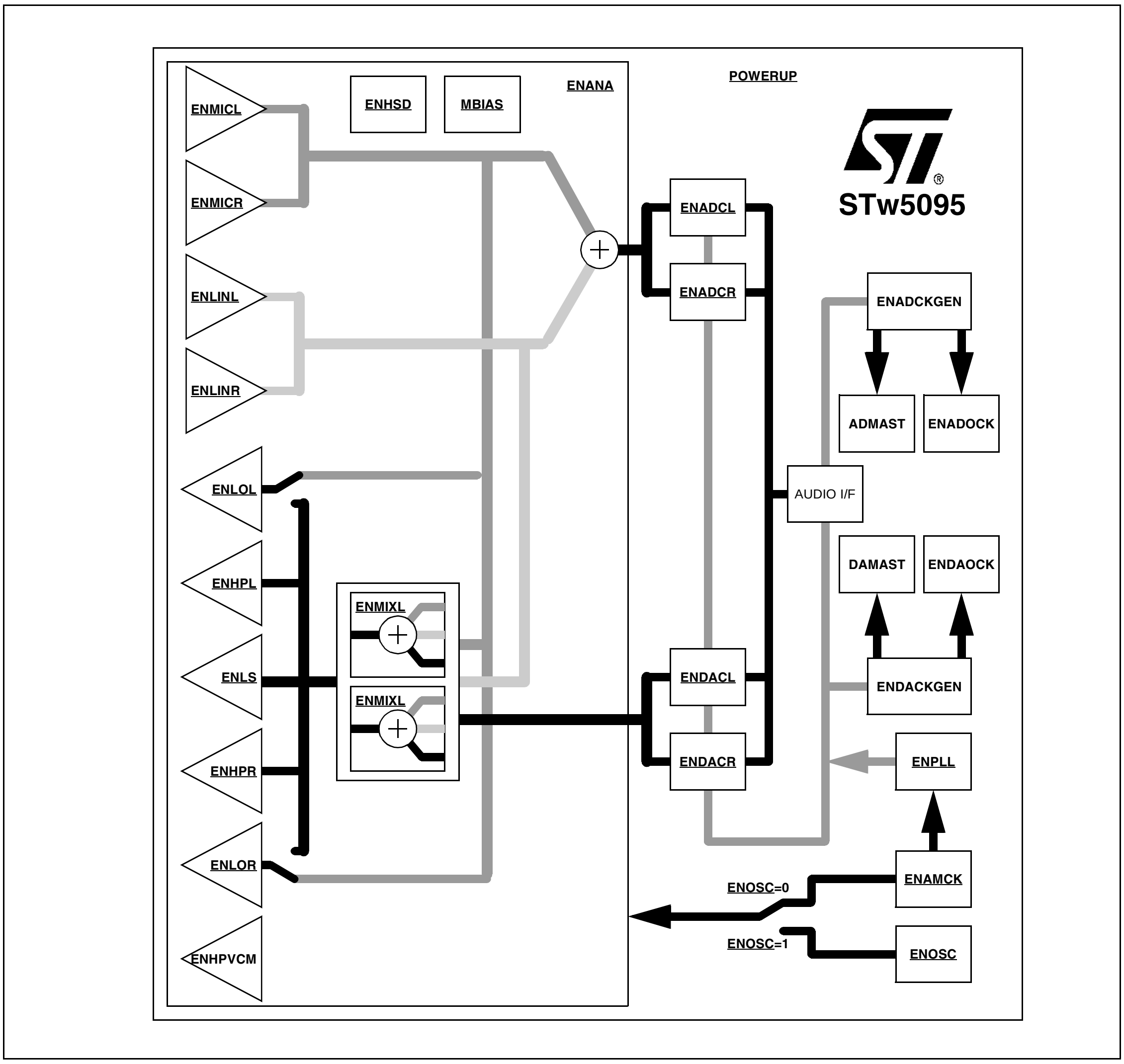
Device Programming: I^2C. The I^2C Control Interface timing is shown in *Section 5.1 on page 41*. The interface has an internal counter that keeps the current address of the control register to be read or written. At each write access of the interface the address counter is loaded with the data of the *register address* field. The value in the address counter is increased after each data byte read or write. It is possible to access the interface in 2 modes: single-byte mode in which the address and data of a single register are specified, and multi-byte mode in which the address of the first register to be written or read is specified and all the following bytes exchanged are the data of successive registers starting from the one specified (in multi-byte mode the internal address counter restart from register 0 after the last register 36). Using the multi-byte mode it is possible to write or read all the registers with a single access to the device on the I^2C bus.

Device Programming: SPI. The SPI Control Interface timing is shown in *Section 5.2 on page 42*. Bits SPIOSEL (SPI Output Select) in CR33 control the out pin selection for serial data out (none, AD_OCK, DA_OCK or IRQ), while bit SPIOHIZ=1 in CR33 selects the high impedance state of serial data out pin when idle. The first bit sent on SDIN, after CSB falling edge, sets the interface for writing (SDIN=1) or reading (SDIN=0), then a 7-bit Control Register address follows.
If the interface is set for writing then the last 8 bits on SDIN are written in the control register. If the interface is set for reading then after the 7 bit address STw5095 sends out 8 bits data on the pin selected with bits SPIOSEL in CR33, while bits present at SDIN pin are ignored. If SPIOSEL=00 (no out pin selected) the reading access on SPI interface can still be useful to clear the IRQ event bits in CR32.

3.3 Power up

STw5095 internal blocks can individually be switched on and off according to the user needs. A general Power Up bit is present at bit 7 of CR0. See the following drawing to select the needed block for the desired function. A fast-settling function is activated to quickly charge external capacitors when the device is switched on (CAPLS, CAPLINEIN and CAPMIC).

Figure 2. Power up block diagram



3.4 Master clock

The master clock pin (AMCK) accepts any frequency from 4 MHz to 32 MHz. The 4-32 MHz range is divided in sub-ranges that have to be programmed in bits CKRANGE in CR30. The jitter and spectral properties of this clock have a direct impact on the DAC and ADC performance because it is used to directly or by integer division drive the continuous-time to sampled-time interfaces.

Note that AMCK clock des not need to have any relation to any other digital or analog input or output.

AMCK can be either a squarewave or a sinewave, bit AMCKSIN in CR30 selects the proper input mode. When a sinewave is used as input, AMCK pin must be decoupled with a capacitor. Specification for sinusoidal input can be found in *Section 9.2: AMCK with sinusoidal input on page 53*.

The AMCK clock is not needed when only analog functions are used. For this purpose an internal oscillator with no external components can be used to operate the device (see *Analog-only operation on page 17*).

3.5 Data rates

STw5095 supports any data rate in 2 ranges: 8 kHz to 48 kHz and 88 kHz to 96 kHz. The range is selected with bits DA96K and AD96K in CR29 for AD and DA paths respectively.

Note: When AD96K=1 it is required to have DA96K=1.

The rates are fully independent in A/D and D/A paths. Moreover the rates do not have to be specified to the device and they can change on the fly, within one range, while data is flowing.

The 2 audio data interfaces (for A/D and D/A) can independently operate in master or slave mode.

3.6 Clock generators and master mode function

STw5095 provides 2 internal clock generators that can drive, if needed, the audio interfaces (master mode), and/or two independent master clocks.

The AMCK clock input frequency is internally raised via a PLL to obtain a clock (MCK) in the range 32 MHz to 48 MHz. The ratio MCK/AMCK is defined in CR30 (see MCKCOEFF in *Section 4.6 on page 32*).

MCK is used to obtain, by fractional division, the oversampled clock (OCK), word clock (SYNC) and bit clock (CK), that will therefore have edges aligned with MCK (the OCK period can have jitter of 1 MCK period).

The frequency of OCK, SYNC and CK is set with DAOCKF in CR21/20 for DA interface, and ADOCKF in CR24/23 for AD interface.

The ratio between OCK and SYNC clocks is selected with bit DAOCK512 in CR22 for DA interface and bit ADOCK512 in CR25 for AD interface. The ratio between CK and SYNC clocks depends on the selected interface format (see *Audio digital interfaces* paragraph below). Note that SPI format can only be slave.

The ADOCK and DAOCK output clocks are activated by bits ENADOCK and ENDAOCK respectively, while master mode generation is activated with two bits: first ADMAST (DAMAST) sets ADSYNC and ADCK (DASYNC and DACK) pins as outputs, then ADMASTGEN (DAMASTGEN) generates the SYNC and CK clocks. The logical value at SYNC and CK pins before data generation depends on the interface selected format.

See description of CR20 to CR25 for further details.

3.7 Audio digital interfaces

Two separate audio data interfaces are provided for AD and DA paths to have maximum flexibility in communicating with other devices. The 2 interfaces can have different rates and can work in different formats and modes (i.e AD interface can be 8 kHz PCM slave while DA is 44.1 kHz I^2S master).

The pins used by the interfaces are:
AD_SYNC, AD_CK and AD_DATA for AD path word clock, bit clock and data, respectively, and DA_SYNC, DA_CK and DA_DATA for DA path word clock, bit clock and data, respectively.

Data is exchanged with MSB first and left channel data first in all formats. Data word-length is selected with bits DAWL in CR26 and ADWL in CR27. AD_DATA pin, outside the selected time slot, is in the impedance condition selected by bit ADHIZ in CR28 in all data formats except Right-Aligned-Format.

In the following paragraphs SYNC, CK and DATA will be used when the distinction between AD and DA is not relevant. When Master Mode is selected (bits DAMAST and ADMAST in CR22 and CR25 respectively) the SYNC and CK clocks are generated internally. In addition, an oversampled clock can be generated for each interface (AD_OCK and DA_OCK). The OCK clock is available in Slave Mode also, if needed.

The AD and DA interfaces can also be used as a single bidirectional interface when they are configured with the same format (Delayed, DSP, etc.) and AD_SYNC is connected to DA_SYNC and DA_CK to AD_CK. Master Mode is still available selecting ADMAST or DAMAST (not both).

The interfaces features are controlled with control registers CR26, CR27 and CR28.

Supported operating formats:

- **Delayed-Format (I^2S compatible)** (DAFORM or ADFORM =000): the Audio Interface is I^2S compatible (*Figure 8 on page 45*). The number of CK periods within one SYNC period is not relevant, as long as enough CK periods are used to transfer the data and the maximum frequency limit specified for bit clock is not exceeded. CK can be either a continuous clock or a sequence of bursts. In master mode there are 32 CK periods per SYNC period (that means 16 CK periods per channel) when the word length is 16 bit, while there are 64 CK periods per SYNC period (or 32 CK periods per channel) when word length is 18bit or higher. Bits ADSYNCP, DASYNCP and ADCKP, DACKP affect the interface format inverting the polarity of SYNC and CK pins respectively.
- **Left-Aligned-Format** (DAFORM or ADFORM =001): this format is equivalent to Delayed-Format without the 1 bit clock delay at the beginning of each frame (*Figure 8 on page 45*).
- **Right-Aligned-Format** (DAFORM or ADFORM =010): this format is equivalent to Delayed-Format, except that the Audio Data is right aligned and that the number of CK periods is fixed to 64 for each SYNC period (*Figure 8 on page 45*).
- **DSP-Format** (DAFORM or ADFORM =011) in this format the Audio Interface starting from a frame sync pulse on SYNC receives (DA) or sends (AD) the Left and Right data one after the other (*Figure 9 on page 46*). The number of CK periods within one SYNC period is not relevant, as long as enough CK periods are used to transfer the data and the maximum frequency limit specified for bit clock is not exceeded. CK can be either a continuous clock or a sequence of bursts. In Master Mode there are 32 CK periods per SYNC period when the word length is 16 bit, while there are 64 CK periods per SYNC period when word length is 18bit or higher. Bit CKP (ADCKP and DACKP) affects the interface format inverting the polarity of CK pin. Bit SYNCP (ADSYNCP and DASYNCP) switches between

delayed (SYNCP=0) and non delayed (SYNCP=1) formats.
DSP-Format is suited to interface with a Multi-Channel Serial Port.

- **SPI-Format** (DAFORM or ADFORM =100) in this format Left and Right data is received with separate data burst. Every burst is identified with a low level on SYNC signal (*Figure 9 on page 46*). There is no timing difference between the Left and Right data burst: the two channels are identified by the startup order: the first burst after AD path or DA path power-up identifies the Left channel data, the second one is the Right channel data, then Left and Right data repeat one after the other. CK must have 16 periods per channel in case of 16 bit data word and 32 periods per channel in case of 18 bit to 32 bit data word. The SPI interface can be configured as a single-channel (mono) interface with bit SPIM (ADSPIM and DASPIM). The mono interface always exchanges the left channel sample. SPI-Format can only be Slave: if Master Mode is selected the CK and SYNC pins are set to 0. Bit CKP (ADCKP and DACKP) affects the interface format inverting the polarity of CK pin.
- **PCM-Format** (DAFORM or ADFORM =111): this format is monophonic, as it can only receive (DA) and transmit (AD) single channel data (*Figure 9 on page 46*). It is mainly used when voice filters are selected. If audio filters are used then the same sample is sent from DA-PCM interface to both channel of DA path, and the left channel sample from AD path is sent to AD-PCM interface. If in the AD path the right channel has to be sent to the PCM interface then the following must be set: ADRTOL=1 (CR27) and ENADCL=0 (CR1). In Master Mode the number of CK periods per SYNC period is between 16 and 512 (see DAPCMF in CR22 and ADPCMF in CR25, *Section 4.6 on page 32* for details). Bit CKP (ADCKP and DACKP) affects the interface format inverting the polarity of CK pin. Bit SYNCP (ADSYNCP and DASYNCP) switches between delayed (SYNCP=0) and non delayed (SYNCP=1) formats.

3.8 Analog inputs

STw5095 has a stereo Microphone preamplifier and a stereo Line In amplifier, with inputs selectable among 5: MIC (for Microphone preamplifier only), LINEIN (for Line In amplifier only) and 3 different AUX inputs (for Microphone and Line In amplifiers). The AUX inputs can be used simultaneously for Line In amplifiers and Microphone preamplifiers.

- **Microphone preamplifier:** it has a very low noise input, specifically designed for low amplitude signals. For this reason it has a high input gain (up to 39 dB) keeping a constant 50 kΩ input impedance for the whole gain range. However it can also be used as a line in preamplifier because it can accept a high dynamic input signal (up to 4 V_{pp}). There are two separate gain and attenuation stages in order to improve the S/N ratio when the preamplifier output range is below full scale (volume control).The gain and attenuation controls are separate for left and right channel (CR3 and CR4 respectively). The Preamplifier input is selected with bits MICSEL in CR18, and it is disconnected when MICMUTE=1. If a single ended input is selected then the preamplifier uses the selected pin as the positive input and connects the negative input (for both left and right channels) to CAPMIC pin, which has to be connected through a capacitor to a low noise ground (typically the same reference ground of the input).
The stereo Microphone preamplifier is powered up with bits ENMICL and ENMICR in CR1.
- **Line In amplifier:** it is designed for high level input signal. The input gain is in the range -20 dB up to 18 dB. The Line In amplifier input is selected with bits LINSEL in CR18, and it is disconnected when LINMUTE=1. If a single ended input is selected then the amplifier uses the selected pin as the positive input and connects the negative input (for both left and right channels) to CAPLINEIN pin, which has to be connected through a capacitor to a

low noise ground (typically the same reference ground of the input).
The stereo Line In amplifier is powered up with bits ENLINL and ENLINR in CR1.

3.9 Analog output drivers

STw5095 provides 3 different analog signal outputs and 1 common mode reference output:

- **Line Out Drivers:** it is a stereo differential output, it can be used as single-ended output just by using the positive or negative pin. It can drive 1 kΩ resistive load. The load can be connected between the positive and negative pins or between one pin and ground through a decoupling capacitor. The output gain is regulated with LOG bits in CR7, in the range 0 to -18 dB, simultaneously for left and right channels. When used as a single ended output the effective gain is 6 dB lower. It is muted with bit MUTELO in CR19. The input signal of this stereo output can come from the analog mixer or directly from MIC preamplifiers. The output Common Mode Voltage level is controlled with bits VCML in CR19. The supply voltage of line out drivers is V_{CCP}.
  The Line Out Drivers are powered up with bits ENLOL and ENLOR in CR1. The output pins are in high impedance state with a 180kΩ pull-down resistor when the Line Out Drivers are powered down.
- **Headphones Drivers:** it is a stereo single ended output. It can drive 16 Ohm resistive load and deliver up to 40 mW. The output gain is regulated with HPLG and HPRG bits in CR8 and CR9 respectively, with a range of -40 to 6 dB. It is muted with bit MUTEHP in CR19. The input signal of this stereo output comes from the analog mixer.The output Common Mode Voltage is controlled with bits VCML in CR19. The supply voltage of headphones drivers is V_{CCP}.
  The Headphones Drivers are powered up with bits ENHPL and ENHPR in CR2.The output pins are in high impedance state when the Headphones Drivers are powered down.
- **Common Mode Voltage Driver:** it is a single ended output with output voltage value selectable with bits VCML in CR19, from 1.2 V to 1.65 V in steps of 150 mV. The output voltage should be set to the value closest to $V_{CCP}/2$ to optimize output drivers performance. The Common Mode Voltage Driver is designed to be connected to the common pin of stereo headphones, so that decoupling capacitors are not needed at HPL and HPR outputs. The supply voltage of the common mode voltage driver is V_{CCP}.
  The Common Mode Voltage Driver is powered up with bit ENHPVCM in CR2.The output pin is in high impedance state when the Common Mode Voltage Driver is powered down.
- **Loudspeaker Driver:** it is a monophonic differential output. It can drive 8 Ω resistive load and deliver up to 500 mW to the load. The output gain is regulated with LSG bits in CR7, in the range -24 to +6 dB. The input signal of the loudspeaker driver comes from the analog mixers: bits LSSEL in CR29 select left channel, right channel, (L+R)/2 (mono) or mute. The output Common Mode Voltage is obtained with an internal voltage divider from V_{CCLS} and it is connected to CAPLS pin. The supply voltage of the loudspeaker driver is V_{CCLS}.
  The Loudspeaker Driver is powered up with bit ENLS in CR2.The output pin is in high impedance state when the Loudspeaker Driver is powered down.

Note: ***Note on direct connection of V_{CCLS} To the battery:***
The voltage of batteries of handheld devices during charging is usually below 5.5 V, making V_{CCLS} supply pin suitable for a direct connection to the battery. In this case if STw5095 is delivering the maximum power to the load and the ambient temperature is above 70 °C then the simultaneous charging of the battery can overheat the device. A basic protection scheme is implemented in STw5095 (activated with bit LSLIM in CR19): it limits the maximum gain of the

loudspeaker to -6 dB when V_{CCLS} is above 4.2 V, and it removes the limit for V_{CCLS} below 4.0 V. The loudspeaker gain is left unchanged if it is set below -6 dB with bits LSG. This event (V_{CCLS} > 4.2 V) can generate, if enabled (bit VLSMSK in CR31), an IRQ signal.

3.10 Analog mixer

STw5095 can send to the output drivers the sum of stereo audio signals from 3 different sources, DA path (bit MIXDAC in CR17), Microphone Preamplifiers (bit MIXMIC in CR17) and Line In Amplifiers (bit MIXLIN in CR17). The mixer does not have a gain control on the inputs, therefore the user should reduce the levels of the input signals within the analog signal range. The stereo Analog Mixer is powered up with bits ENMIXL and ENMIXR in CR2.

3.11 AD path

The AD path converts audio signals from Microphone Preamplifiers (selected with bit ADMIC in CR17) and Line In Amplifiers (bit ADLIN in CR17) inputs to digital domain. If both inputs are selected then the sum of the two is converted. After AD conversion the audio data is resampled with a sample rate converter and then processed with the internal DSP. Two different filters are selectable in the DSP (bit ADVOICE in CR29): stereo Audio Filter, with DC offset removal and FIR image filtering; and a standard mono Voice-channel filter (uses left channel input and feeds both channel output). The AD path includes a digital gain control (ADCLG, ADCRG in CR12 and CR13 respectively) in the range -57 to +8 dB. The maximum gain from Mic Preamplifier to AD interface is then 47 dB. When Audio filter is selected in both AD and DA paths then DA audio data can be summed to AD data and sent to the AD Audio Interface (see DA2ADG in CR15). Left and Right channels can be independently switched on and off to save power, if needed (bits ENADCL and ENADCR in CR1)

3.12 DA path

The DA path converts digital data from the digital audio interface to analog domain and feeds it to the analog mixer. Incoming audio data is processed with a DSP where different filters are selectable (bit DAVOICE in CR29): Audio Filter, stereo, with FIR image filtering, bass and treble controls (bits BASS and TREBLE in CR14), de-emphasis filter; and a standard Voice-channel filter, mono (uses left channel input and feeds both channel output). A dynamic compression function is available for both audio and voice filters (bit DYNC in CR14). The DA path includes a digital gain control (DACLG, DACRG in CR10 and CR11 respectively) in the range -65 to 0 dB. AD to DA mixing (sidetone) can be enabled: see CR16 for details. Left and Right channel can be independently switched on and off to save power, if needed (bits ENDACL and ENDACR in CR1)

3.13 Analog-only operation

STw5095 can operate without AMCK master clock if analog-only functions are used. It is possible to mix Microphone and Line In preamplifiers signals and listen through headphones, loudspeaker or send them to line-out. The analog-only operation is enabled with bit ENOSC in CR0. When ENOSC=1 the AD and DA paths cannot be used.

In Analog Mode STw5095 can handle two different stereo audio signals, so it can be used as a front end for an external voice codec that does not include microphone preamplifiers and power drivers: mic signal is sent through Microphone preamplifiers directly to line out drivers (Transmit path), while Receive signal is sent through Line In amplifiers to the selected power drivers.

3.14 Automatic Gain Control (AGC)

STw5095 provides a digital Automatic Gain Control in AD path. The circuit can control the input gain at MIC preamplifier, Line In amplifier or both (bits ENAGCMIC and ENAGCLIN in CR35). When one input is selected, the center gain value used for the input is fixed with bits MICLG, MICRG, LINLG and LINRG in CR3 to CR6 (like in normal operation), then the AGC circuit adds to all the gains a value in the range -10.5 dB to +10.5 dB (or, extended with bit AGCRANGE in CR35, -21 dB to 21 dB), in order to obtain an average level at the digital interface output in the range -6 dB to -30 dB (selected with bits AGCLEV in CR35). The AGC added gain acts directly in the input gain, to avoid input saturation and improve S/N ratio, so it cannot exceed the input gain range. When MIC and Line-In inputs are selected simultaneously the control is performed on the sum of the two, preserving the balance fixed with input gains. Different values for Attack and Decay constants can be selected, depending on the kind of signal the AGC has to control (i.e. voice, music). The Attack and Decay time constants are related to the AD data rate (see bits AGCATT and AGCDEL in CR34).

3.15 Interrupt request: IRQ pin

STw5095 interrupt request feature can signal to a control device the occurrence of particular events. Two control registers are used to choose the behavior of IRQ pin: the first is a Status/ Event Register (CR32), where bits can represent the status of an internal function (i.e. a voltage is above or below a threshold) or an event (i.e. a voltage changed crossing a threshold); the second is a Mask Register (CR31) where if a bit in the mask is set to 1 then the corresponding bit in the Status/Event Register can affect IRQ pin status.

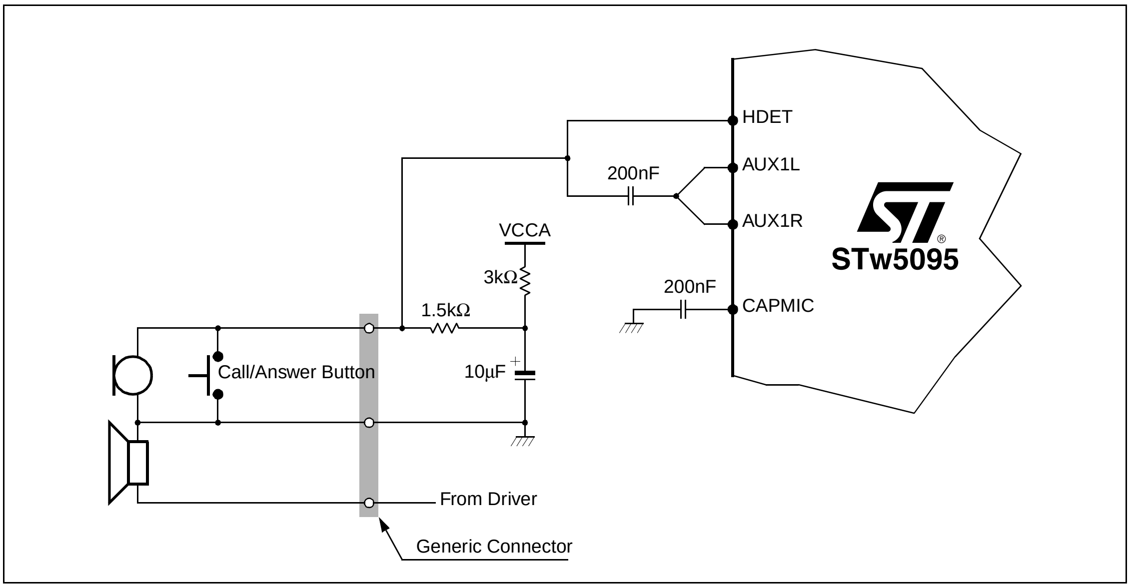
The IRQ pin is always active low. At V_{CC} power up an interrupt request is generated by the Power-On-Reset circuit that sets to 1 bits PORMSK in CR31 and POREV in CR32. After this event the PORMSK bit should be cleared by the user and bit IRQCMOS in CR33 should be set according to the application (open drain or CMOS).

When an IRQ event occurs and SPI control interface is selected with no serial output pin it is still possible to identify the event (and relative status) that generated the interrupt request. This can be done by setting the IRQ mask/enable bits (in CR31) one at the time (with successive writings) and reading the IRQ pin status. A simple example of this is the headset plug-in detection: at first we set bit HSDETMSK=1 in CR31 (with all the other bits set to 0). If there is an interrupt request then we set HSDETMSK=0 and HSDETEN=1, so we can read the HSDET status at IRQ pin. Then we read CR32 to clear its content (even if no data is sent out).

3.16 Headset plug-in and push-button detection

STw5095 can detect the plug-in of a microphone connector and the press/release event of a call/answer push-button. An application example can be found below, while specifications can be found in *Section 9.4 on page 54*.

Figure 3. Plug-in and push-button detection application note



3.17 Microphone biasing circuit

The Microphone Biasing Circuit can drive mono or stereo microphones and can switch them off when not needed in order to save the current used by the microphone biasing network. Two bits control the behavior of the microphone bias circuit: MBIAS in CR17 enables the circuit (fixed voltage at MBIAS pin), while bit MBIASPD in CR17 affects the behavior of MBIAS pin when the function is not enabled. In particular when MBIASPD=1 the MBIAS pin is pulled down, otherwise it is left in tristate mode. The specification for the microphone biasing circuit can be found in *Section 9.6 on page 55*, and an application note is shown in *Section 17 on page 66*.

4 Control Registers

4.1 Summary

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR0 (00h)	Supply & Power Control #1	POWERUP	ENANA	ENAMCK	ENOSC	ENPLL	ENHSD	A24V	D12V	0000 0000
CR1 (01h)	Power Control #2	ENADCL	ENADCR	ENDACL	ENDACR	ENMICL	ENMICR	ENLINL	ENLINR	0000 0000
CR2 (02h)	Power Control #3	ENLOL	ENLOR	ENHPL	ENHPR	ENHPVCM	ENLS	ENMIXL	ENMIXR	0000 0000
CR3 (03h)	Mic Gain Left	MICLA(2:0)			MICLG(4:0)					0000 0000
CR4 (04h)	Mic Gain Right	MICRA(2:0)			MICRG(4:0)					0000 0000
CR5 (05h)	Line in Gain Left	X	X	X	LINLG(4:0)					0000 1001
CR6 (06h)	Line in Gain Right	X	X	X	LINRG(4:0)					0000 1001
CR7 (07h)	LO gain & LS gain	X	LOG(2:0)			LSG(3:0)				0000 0011
CR8 (08h)	HPL Gain	X	X	X	HPLG(4:0)					0000 0011
CR9 (09h)	HPR Gain	X	X	X	HPRG(4:0)					0000 0011
CR10 (0Ah)	DAC Digital Gain Left	X	X	DACLG(5:0)						0000 0000
CR11 (0Bh)	DAC Digital Gain Right	X	X	DACRG(5:0)						0000 0000
CR12 (0Ch)	ADC Digital Gain Left	X	X	ADCLG(5:0)						0000 1000
CR13 (0Dh)	ADC Digital Gain Right	X	X	ADCRG(5:0)						0000 1000
CR14 (0Eh)	Bass/Treble/De-emphasis	DYNC	TREBLE(2:0)			BASS(3:0)				0000 0000
CR15 (0Fh)	DA to AD mixing gain	X	X	X	DA2ADG(4:0)					0000 0000
CR16 (10h)	AD to DA mix/sidetone gain	X	X	AD2DAG(5:0)						0000 0000
CR17 (11h)	Mixer Switches & Mic Bias	MBIAS	MBIASPD	ADMIC	ADLIN	MIXMIC	MIXLIN	MIXDAC	MICLO	0000 0000
CR18 (12h)	Input Switches	X	IN2VCM	LINMUTE	LINSEL(1:0)		MICMUTE	MICSEL(1:0)		0010 0100
CR19 (13h)	Drivers Control	VCML(1:0)		X	MUTELO	MUTEHP	LSLIM	LSSEL(1:0)		0101 1000
CR20 (14h)	DAOCK Frequency Ls byte	DAOCKF(7:0)								0000 0000
CR21 (15h)	DAOCK Frequency Ms byte	DAOCKF(15:8)								0000 0000
CR22 (16h)	DA Clock Generator Control	X	X	DAMAST	DAMASTGEN	ENDAOCK	DAOCK512	DAPCMF(1:0)		0000 0000
CR23 (17h)	ADOCK Frequency Ls byte	ADOCKF(7:0)								0000 0000
CR24 (18h)	ADOCK Frequency Ms byte	ADOCKF(15:8)								0000 0000
CR25 (19h)	AD Clock Generator Con-trol	X	X	ADMAST	ADMASTGEN	ENADOCK	ADOCK512	ADPCMF(1:0)		0000 0000
CR26 (1Ah)	DAC Data IF Control	X	DAFORM(2:0)			DASPIM	DAWL(2:0)			0000 0000
CR27 (1Bh)	ADC Data IF Control	ADRTOL	ADFORM2:0)			ADSPIM	ADWL(2:0)			0000 0000
CR28 (1Ch)	DAC&ADC Data IF Control	AMCKINV	DACKP	DASYNCP	DAMONO	ADCKP	ADSYNCP	ADMONO	ADHIZ	0000 0000
CR29 (1Dh)	Digital Filters Control	X	DAVOICE	DA96K	RXNH	ADVOICE	AD96K	ADNH	TXNH	0000 0000
CR30 (1Eh)	Soft Reset & AMCK Range	SWRES	X	X	X	AMCKSIN	CKRANGE(2:0)			0000 0000
CR31 (1Fh)	interrupt Mask	VLSHEN	PUSHBEN	HSDETEN	VLSHMSK	PUSHBMSK	HSDETMSK	OVFMSK	PORMSK	0000 0000
CR32 (20h)	Interrupt Status	VLSH	PUSHB	HSDET	VLSHEV	PUSHBEV	HSDETEV	OVFEV	POREV	0000 0000
CR33 (21h)	Misc. Control	X	X	SPIOHIZ	SPIOSEL(1:0)		IRQCMOS	OVFDA	OVFAD	0000 0000
CR34 (22h)	AGC Attack/Decay coeff.	AGCATT(3:0)				AGCDEC(3:0)				0000 0000
CR35 (23h)	AGC Control	X	ENAGCLIN	ENAGCMIC	AGCRANGE	AGCLEV(3:0)				0000 0000
CR36 (24h)	RESERVED	X	X	X	X	X	X	X	X	0000 0000

Note: X reserved, write zero

4.2 Supply and power control

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR0 (00h)	Supply & Power Control #1	POWERUP	ENANA	ENAMCK	ENOSC	ENPLL	ENHSD	A24V	D12V	0000 0000
CR1 (01h)	Power Control #2	ENADCL	ENADCR	ENDACL	ENDACR	ENMICL	ENMICR	ENLINL	ENLINR	0000 0000
CR2 (02h)	Power Control #3	ENLOL	ENLOR	ENHPL	ENHPR	ENHPVCM	ENLS	ENMIXL	ENMIXR	0000 0000

Bits	Name	Val.	CR0 Description	Def.
7	POWERUP	1 0	All the enabled analog and digital blocks are in power up All the device is in power down	0
6	ENANA	1 0	The analog blocks can be enabled All the analog blocks are in power down	0
5	ENAMCK	1 0	AMCK clock input pin is enabled AMCK clock input pin is disabled	0
4	ENOSC	1 0	The Internal Oscillator is enabled. The analog blocks use Oscillator clock The Internal Oscillator is in power down	0
3	ENPLL	1 0	The PLL is enabled The PLL is in power down	0
2	ENHSD	1 0	The Headset Plug-in Detector is enabled The Headset Plug-in Detector is disabled	0
1	A24V	1 0	Analog Supply Pins voltage range is 2.4V<V_{CCA}<2.7V Analog Supply Pins voltage range is 2.7V<V_{CCA}<3.3V	0
0	D12V	1 0	Digital I/O Pins voltage range is 1.2V<V_{CCIO}<1.8V Digital I/O Pins voltage range is 1.71V<V_{CCIO}<V_{CC}	0

Bits	Name	Value	CR1 Description	Def.
7	ENADCL	1 0	The left channel A/D converter is enabled The left channel A/D converter is in power down	0
6	ENADCR	1 0	The right channel A/D converter is enabled The right channel A/D converter is in power down	0
5	ENDACL	1 0	The left channel D/A converter is enabled The left channel D/A converter is in power down	0
4	ENDACR	1 0	The right channel D/A converter is enabled The right channel D/A converter is in power down	0
3	ENMICL	1 0	The left channel microphone preamplifier is enabled The left channel microphone preamplifier is in power down	0
2	ENMICR	1 0	The right channel microphone preamplifier is enabled The right channel microphone preamplifier is in power down	0
1	ENLINL	1 0	The left channel line-in preamplifier is enabled The left channel line-in preamplifier is in power down	0
0	ENLINR	1 0	The right channel line-in preamplifier is enabled The right channel line-in preamplifier is in power down	0

Bit #	Name	Value	CR2 Description	Def.
7	ENLOL	1 0	The left channel line out driver is enabled The left channel line out driver is in power down (default)	0
6	ENLOR	1 0	The right channel line out driver is enabled The right channel line out driver is in power down (default)	0
5	ENHPL	1 0	The left channel headphones driver is enabled The left channel headphones driver is in power down (default)	0
4	ENHPR	1 0	The right channel headphones driver is enabled The right channel headphones driver is in power down (default)	0
3	ENHPVCM	1 0	The headphones reference voltage generator is enabled The headphones reference voltage generator is in power down (def)	0
2	ENLS	1 0	The 8Ω loudspeaker amplifier is enabled The 8Ω loudspeaker amplifier is in power down (default)	0
1	ENMIXL	1 0	The left channel analog output mixer is enabled The left channel analog output mixer is in power down (default)	0
0	ENMIXR	1 0	The right channel analog output mixer is enabled The right channel analog output mixer is in power down (default)	0

4.3 Gains

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR3 (03h)	Mic Gain Left	MICLA(2:0)			MICLG(4:0)					0000 0000
CR4 (04h)	Mic Gain Right	MICRA(2:0)			MICRG(4:0)					0000 0000
CR5 (05h)	Line in Gain Left	X	X	X	LINLG(4:0)					0000 1001
CR6 (06h)	Line in Gain Right	X	X	X	LINRG(4:0)					0000 1001
CR7 (07h)	LO gain & LS gain	X	LOG(2:0)			LSG(3:0)				0000 0011
CR8 (08h)	HPL Gain	X	X	X	HPLG(4:0)					0000 0011
CR9 (09h)	HPR Gain	X	X	X	HPRG(4:0)					0000 0011
CR10 (0Ah)	DAC Digital Gain Left	X	X	DACLG(5:0)						0000 0000
CR11 (0Bh)	DAC Digital Gain Right	X	X	DACRG(5:0)						0000 0000
CR12 (0Ch)	ADC Digital Gain Left	X	X	ADCLG(5:0)						0000 1000
CR13 (0Dh)	ADC Digital Gain Right	X	X	ADCRG(5:0)						0000 1000

Bits	Name CR3 Name CR4	Value	CR3 and CR4 Description	Def.
7-5	MICLA(2:0) MICRA(2:0)	 000 001 010 ... 110 111	Left (CR3) and Right (CR4) Channels Microphone Attenuation 0.0 dB Gain (default) -1.5 dB Gain -3.0 dB Gain ...step 1.5 dB -9.0 dB Gain -12.0 dB Gain	000
4-0	MICLG(4:0) MICRG(4:0)	 00000 00001 00010 ... 11010	Left (CR3) and Right (CR4) Channels Microphone Gain 0.0 dB Gain (default) 1.5 dB Gain 3.0 dB Gain ...step 1.5 dB 39.0 dB Gain	00000

Bits	Name CR5 Name CR6	Value	CR5 and CR6 Description	Def.
4-0	LINLG(4:0) LINRG(4:0)	 00000 00001 00010 ... 01001 ... 10011	Left (CR5) and Right (CR6) Channels Line In Gain 18.0 dB Gain 16.0 dB Gain 14.0 dB Gain ...step 2.0 dB 0.0 dB Gain (default) ...step 2.0 dB -20.0 dB Gain	01001

Bits	Name	Value	CR7 Description		Def.
6-4	LOG(2:0)		Left and Right Channel Line Out Drivers Gain		000
			Gain to Differential Output	Equivalent Single-Ended Gain	
		000	-18.0 dB Gain (default)	-24.0 dB Gain (default)	
		001	-15.0 dB Gain	-21.0 dB Gain	
		010	-12.0 dB Gain	-18.0 dB Gain	
		...	...step 3 dB	...step 3 dB	
		110	00 dB Gain	-6.0 dB Gain	
3-0	LSG(3:0)		8Ω Loudspeaker Gain		0011
		0000	6.0 dB Gain		
		0001	4.0 dB Gain		
		0010	2.0 dB Gain		
		0011	0.0 dB Gain (default)		
		...	...step 2.0 dB		
		1111	-24.0 dB Gain		

Bits	Name CR8 Name CR9	Value	CR8 and CR9 Description	Def.
4-0	HPLG(4:0) HPRG(4:0)		Left (CR8) and Right (CR9) Channels Headphones Driver Gain	00011
		00000	0.0 dB Gain	
		00001	-2.0 dB Gain	
		00010	-4.0 dB Gain	
		00011	-6.0 dB Gain (default)	
		...	...step 2.0 dB	
		10100	-40.0 dB Gain	

Bits	Name CR10 Name CR11	Value	CR10 and CR11 Description	Def.
5-0	DACLG(5:0) DACRG(5:0)		Left (CR10) and Right (CR11) Channels DAC Digital Gain	000000
		000000	0.0 dB Gain (default)	
		000001	-1.0 dB Gain	
		000010	-2.0 dB Gain	
		000011	-3.0 dB Gain	
		000100	-4.0 dB Gain	
		000101	-5.0 dB Gain	
		000110	-6.0 dB Gain	
		000111	-7.0 dB Gain	
		001000	-8.0 dB Gain	
		001001	-9.0 dB Gain	
		001010	-10.0 dB Gain	
		001011	-11.0 dB Gain	
		001100	-12.0 dB Gain	
		001101	-13.0 dB Gain	
		001110	-14.0 dB Gain	
		001111	-15.0 dB Gain	
		010000	-16.0 dB Gain	
		010001	-17.0 dB Gain	
		010010	-18.0 dB Gain	
		010011	-20.0 dB Gain	
		010100	-22.0 dB Gain	
		010101	-24.0 dB Gain	
		010110	-26.0 dB Gain	
		010111	-28.0 dB Gain	
		011000	-30.0 dB Gain	
		011001	-32.0 dB Gain	
		011010	-34.0 dB Gain	
		011011	-36.0 dB Gain	
		011100	-38.0 dB Gain	
		011101	-41.0 dB Gain	
		011110	-44.0 dB Gain	
		011111	-47.0 dB Gain	
		100000	-50.0 dB Gain	
		100001	-53.0 dB Gain	
		100010	-56.0 dB Gain	
		100011	-59.0 dB Gain	
		100100	-65.0 dB Gain	
		100101	$-\infty$ dB Gain	

Bits	Name CR12 Name CR13	Value	CR12 and CR13 Description	Def.
5-0	ADCLG(5:0) ACDRG(5:0)		Left (CR12) and Right (CR13) Channels ADC Digital Gain	001000
		000000	8.0 dB Gain	
		000001	7.0 dB Gain	
		000010	6.0 dB Gain	
		000011	5.0 dB Gain	
		000100	4.0 dB Gain	
		000101	3.0 dB Gain	
		000110	2.0 dB Gain	
		000111	1.0 dB Gain	
		001000	0.0 dB Gain (default)	
		001001	-1.0 dB Gain	
		001010	-2.0 dB Gain	
		001011	-3.0 dB Gain	
		001100	-4.0 dB Gain	
		001101	-5.0 dB Gain	
		001110	-6.0 dB Gain	
		001111	-7.0 dB Gain	
		010000	-8.0 dB Gain	
		010001	-9.0 dB Gain	
		010010	-10.0 dB Gain	
		010011	-11.0 dB Gain	
		010100	-12.0 dB Gain	
		010101	-14.0 dB Gain	
		010110	-16.0 dB Gain	
		010111	-18.0 dB Gain	
		011000	-20.0 dB Gain	
		011001	-22.0 dB Gain	
		011010	-24.0 dB Gain	
		011011	-26.0 dB Gain	
		011100	-28.0 dB Gain	
		011101	-30.0 dB Gain	
		011110	-33.0 dB Gain	
		011111	-36.0 dB Gain	
		100000	-39.0 dB Gain	
		100001	-42.0 dB Gain	
		100010	-45.0 dB Gain	
		100011	-48.0 dB Gain	
		100100	-51.0 dB Gain	
		100101	-57.0 dB Gain	
		100110	$-\infty$ dB Gain	

4.4 DSP control

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR14 (0Eh)	Bass/Treble/De-emphasis	DYNC	TREBLE(2:0)			BASS(3:0)				0000 0000
CR15 (0Fh)	DA to AD mixing gain	X	X	X	DA2ADG(4:0)					0000 0000
CR16 (10h)	AD to DA mix/sidetone gain	X	X	AD2DAG(5:0)						0000 0000

Bits	Name	Value	CR14 Description	Def.
7	DYNC	1 0	Audio Dynamic Compression in D/A path is enabled Audio Dynamic Compression in D/A path is disabled	0
6-4	TREBLE(2:0)	 011 010 001 000 111 110 101 100	Treble Control in D/A path +6.0 dB Treble Gain +4.0 dB Treble Gain +2.0 dB Treble Gain 0.0 dB Treble Gain -2.0 dB Treble Gain -4.0 dB Treble Gain -6.0 dB Treble Gain De-emphasis filter enabled	000
3-0	BASS(3:0)	 0101 0100 0011 0010 0001 0000 1111 1110 1101 1100 1011	Bass Control in D/A path +12.5 dB Bass Gain +10.0 dB Bass Gain +7.5 dB Bass Gain +5.0 dB Bass Gain +2.5 dB Bass Gain 0.0 dB Bass Gain -2.5 dB Bass Gain -5.0 dB Bass Gain -7.5 dB Bass Gain -10.0 dB Bass Gain -12.5 dB Bass Gain	0000

Bits	Name	Value	CR15 Description	Def.
4-0	DA2ADG(4:0)*		DA to AD mixing (Audio filter in D/A and A/D path selected)	00000
		00000	DA to AD mixing Disabled (default)	
		00001	+2.0dB Gain	
		00010	0.0dB Gain	
		00011	-2.0dB Gain	
		00100	-4.0dB Gain	
		00101	-6.0dB Gain	
		00110	-8.0dB Gain	
		00111	-10.0dB Gain	
		01000	-12.0dB Gain	
		01001	-14.0dB Gain	
		01010	-16.0dB Gain	
		01011	-18.0dB Gain	
		01100	-20.0dB Gain	
		01101	-22.0dB Gain	
		01110	-24.0dB Gain	
		01111	-26.0dB Gain	
		10000	-28.0dB Gain	
		10001	-30.0dB Gain	
		10010	-32.0dB Gain	
		10011	-34.0dB Gain	
		10100	-36.0dB Gain	
		10101	-38.0dB Gain	
		10110	-40.0dB Gain	

* When Voice filter in D/A or A/D path is selected this function is disabled

Note: D/A to A/D mixing is performed at AD data rate, so if A/D and D/A rates are different then asynchronous sampling artifacts may occur.

Bits	Name	Value	CR16 Description	Def.
5-0	AD2DAG(5:0)		AD to DA mixing (sidetone)	000000
		000000	AD to DA mixing Disabled (default)	
		000001	-1.0dB Gain	
		000010	-2.0dB Gain	
		000011	-3.0dB Gain	
		000100	-4.0dB Gain	
		000101	-5.0dB Gain	
		000110	-6.0dB Gain	
		000111	-7.0dB Gain	
		001000	-8.0dB Gain	
		001001	-9.0dB Gain	
		001010	-10.0dB Gain	
		001011	-11.0dB Gain	
		001100	-12.0dB Gain	
		001101	-13.0dB Gain	
		001110	-14.0dB Gain	
		001111	-15.0dB Gain	
		010000	-16.0dB Gain	
		010001	-17.0dB Gain	
		010010	-18.0dB Gain	
		010011	-19.0dB Gain	
		010100	-20.0dB Gain	
		010101	-21.0dB Gain	
		010110	-22.0dB Gain	
		010111	-23.0dB Gain	
		011000	-24.0dB Gain	
		011001	-25.0dB Gain	
		011010	-26.0dB Gain	
		011011	-27.0dB Gain	
		011100	-28.0dB Gain	
		011101	-29.0dB Gain	
		011110	-30.0dB Gain	
		011111	-31.0dB Gain	
		100000	-32.0dB Gain	
		100001	-33.0dB Gain	
		100010	-34.0dB Gain	
		100011	-35.0dB Gain	
		100100	-36.0dB Gain	
		100101	-37.0dB Gain	
		100110	-38.0dB Gain	
		100111	-39.0dB Gain	
		101000	-40.0dB Gain	
		101001	-41.0dB Gain	
		101010	-42.0dB Gain	

4.5 Analog functions

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR17 (11h)	Mixer Switches & Mic Bias	MBIAS	MBIASPD	ADMIC	ADLIN	MIXMIC	MIXLIN	MIXDAC	MICLO	0000 0000
CR18 (12h)	Input Switches	X	IN2VCM	LINMUTE	LINSEL(1:0)		MICMUTE	MICSEL(1:0)		0010 0100
CR19 (13h)	Drivers Control	VCML(1:0)		X	MUTELO	MUTEHP	LSLIM	LSSEL(1:0)		0101 1000

Bits	Name	Value	CR17 Description	Def.
7	MBIAS	1 0	Microphone Bias Enabled (2.1V typ at MBIAS Pin) Microphone Bias Disabled	0
6	MBIASPD	1 0	MBIAS Pin is pulled down when Microphone Bias is disabled MBIAS Pin is in High Impedance state when Microphone Bias is disabled	0
5	ADMIC	1 0	Microphone Preamplifiers are connected to AD path Microphone Preamplifiers are not connected to AD path	0
4	ADLIN	1 0	Line In Preamplifiers are connected to AD path Line In Preamplifiers are not connected to AD path	0
3	MIXMIC	1 0	Microphone Preamplifiers are connected to Mixers Microphone Preamplifiers are not connected to Mixers	0
2	MIXLIN	1 0	Line In Preamplifiers are connected to Mixers Line In Preamplifiers are not connected to Mixers	0
1	MIXDAC	1 0	Stereo DAC path is connected to Mixers Stereo DAC path is not connected to Mixers	0
0	MICLO	1 0	Microphone Preamplifiers are connected to Line Out Drivers Mixers are connected to Line Out Drivers	0

Bits	Name	Value	CR18 Description	Def.
6	IN2VCM	1 0	Unused Analog input pins are biased to Common Mode voltage Unused Analog input pins are in high impedance state	0
5	LINMUTE	1 0	Line In Preamplifiers are muted Line In Preamplifiers are not muted	1
4-3	LINSEL(1:0)	00 01 10 11	Input Pins connected to Line In Preamplifiers (if LINMUTE=0) LINEIN (LINEINL, LINEINR) AUX1 (AUX1L, AUX1R) AUX2 (AUX2LP-AUX2LN, AUX2RP-AUX2RN) AUX3 (AUX3L, AUX3R)	00
2	MICMUTE	1 0	Microphone Preamplifiers are muted Microphone Preamplifiers are not muted	1
1-0	MICSEL(1:0)	00 01 10 11	Input Pins connected to Microphone Preamplifiers (if MICMUTE=0) MIC (MICLP-MICLN, MICRP-MICRN) AUX1 (AUX1L, AUX1R) AUX2 (AUX2LP-AUX2LN, AUX2RP-AUX2RN) AUX3 (AUX3L, AUX3R)	00

Bits	Name	Value	CR19 Description	Def.
7-6	VCML(1:0)	00 01 10 11	Common Mode Voltage Level for Line Out and Headphones drivers 1.20 V 1.35 V (default) 1.50 V 1.65 V	01
4	MUTELO	1 0	Line Out Drivers are muted Line Out Drivers are not muted	1
3	MUTEHP	1 0	Headphones Drivers (HP) are muted Headphones Drivers (HP) are not muted	1
2	LSLIM	1 0	Loudspeaker Driver (LS) gain is limited when V_{CCLS} is above 4.2V typ Loudspeaker Driver (LS) gain is not limited	0
1-0	LSSEL(1:0)	00 01 10 11	Mute Loudspeaker Driver (LS) is muted Right Right Channel Mixer only connected to Loudspeaker driver Left Left Channel Mixer only connected to Loudspeaker driver Mono (Left + Right)/2 Channel Mixers connected to Loudspeaker driver	00

4.6 Digital audio interfaces master mode and clock generators

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR20 (14h)	DAOCK Frequency Ls byte	DAOCKF(7:0)								0000 0000
CR21 (15h)	DAOCK Frequency Ms byte	DAOCKF(15:8)								0000 0000
CR22 (16h)	DA Clock Generator Control	X	X	DAMAST	DAMASTGEN	ENDAOCK	DAOCK512	DAPCMF(1:0)		0000 0000
CR23 (17h)	ADOCK Frequency Ls byte	ADOCKF(7:0)								0000 0000
CR24 (18h)	ADOCK Frequency Ms byte	ADOCKF(15:8)								0000 0000
CR25 (19h)	AD Clock Generator Control	X	X	ADMAST	ADMASTGEN	ENADOCK	ADOCK512	ADPCMF(1:0)		0000 0000

Bits	Name CR21-20 Name CR24-23	Value	CR21-20 and CR24-23 Description	Def.
15-0	DAOCKF(15:0) ADOCKF(15:0)	K	The following formulas can be used to obtain the value of K for the desired FS or OCK respectively in the clock generator $K(FS) = round\left(2^{25}\frac{FS}{AMCK \cdot MCKCOEFF}\right)$ $K(OCK) = round\left(2^{25}\frac{OCK}{AMCK \cdot MCKCOEFF \cdot OSR}\right)$ FS: Data Rate (DA_SYNC or AD_SYNC frequency in Master Mode) OCK: Oversampled Clock Frequency (DA_OCK or AD_OCK) AMCK: Input Master Clock Frequency MCKCOEFF: See CR30 for definition OSR: See bit 2 in CR22 and CR25	0000h

Note: CR21-20 and CR24-23 are meaningful in Master Mode Only.

Bits	Name CR22 (Name CR25)	Value	CR22 and CR25 Description	Def.
5	DAMAST (ADMAST)	1 0	DA (AD) Audio interface is in Master Mode (low impedance output) DA (AD) Audio interface is in Slave Mode (high impedance input)	0
4	DAMASTGEN (ADMASTGEN)	1 0	DA (AD) Master Generator is enabled DA (AD) Master Generator is disabled	0
3	ENDAOCK (ENADOCK)	1 0	DA_OCK (AD_OCK) Output Clock is enabled DA_OCK (AD_OCK) Output Clock is disabled	0
2	DAOCK512 (ADOCK512)	1 0	Definition of DA_OSR (AD_OSR) DA_OCK/DA_SYNC (AD_OCK/AD_SYNC) Ratio In Master Mode is 512 DA_OCK/DA_SYNC (AD_OCK/AD_SYNC) Ratio In Master Mode is 256	0
1-0	DAPCMF(1:0) (ADPCMF(1:0))	00 00 01 10 11 11	DA_CK/DA_SYNC (AD_CK/AD_SYNC) Ratio in PCM Master Mode - 16 when CR26 DAWL=000 (CR27 ADWL=000) - 32 when CR26 DAWL≠000 (CR27 ADWL≠000) - 64 - 128 - 256 when CR22 DAOCK512=0 (CR25 ADOCK512=0) - 512 when CR22 DAOCK512=1 (CR25 ADOCK512=1)	00

4.7 Digital audio interfaces

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR26 (1Ah)	DAC Data IF Control	X	DAFORM(2:0)			DASPIM	DAWL(2:0)			0000 0000
CR27 (1Bh)	ADC Data IF Control	ADRTOL	ADFORM2:0)			ADSPIM	ADWL(2:0)			0000 0000
CR28 (1Ch)	DAC&ADC Data IF Control	AMCKINV	DACKP	DASYNCP	DAMONO	ADCKP	ADSYNCP	ADMONO	ADHIZ	0000 0000

Bits	Name	Value	CR26 Description	Def.
6-4	DAFORM(2:0)	 000 001 010 011 100 111	DA Audio Interface Format Selection Delayed Format (I^2S Compatible) Left Aligned Format Right Aligned Format DSP Format SPI Format PCM Format (uses left channel)	000
3	DASPIM	1 0	DA interface in SPI mode receives one word for both channels DA interface in SPI mode receives two words (alternated, left channel first)	0
2-0	DAWL(2:0)	 000 001 010 011 100	DA interface word length 16 bit 18 bit 20 bit 24 bit 32 bit	000

Bits	Name	Value	CR27 Description	Def.
7	ADRTOL	1 0	AD Right Channel sent to PCM I/F (must set ENADCR=0 in CR1) Normal Operation	0
6-4	ADFORM(2:0)	 000 001 010 011 100 111	AD Audio Interface Format Selection Delayed Format (I^2S compatible) Left Aligned Format Right Aligned Format DSP Format SPI Format PCM Format (sends out left channel)	000
3	ADSPIM	1 0	AD interface in SPI mode sends one channel (left) AD interface in SPI mode sends two channels (alternated, left first)	0
2-0	ADWL(2:0)	 000 001 010 011 100	AD interface word length 16 bit 18 bit 20 bit 24 bit 32 bit	000

Bits	Name	Value	CR28 Description	Def.
7	AMCKINV	1 0	AMCK is inverted AMCK is not inverted	0
6	DACKP	1 0	DA Bit Clock Pin (DA_CK) polarity is inverted DA Bit Clock Pin (DA_CK) polarity is not inverted	0
5	DASYNCP	 1 0	DSP and PCM Formats in DA Interface Non Delayed format Delayed Format	0
		 1 0	Delayed, Left-aligned, Right-aligned and SPI Formats in DA Interface DA Sync Pin (DA_SYNC) polarity is inverted DA Sync Pin (DA_SYNC) polarity is not inverted	
4	DAMONO	1 0	Mono Mode: (L+R)/2 from Audio Interface is used on both DAC channels Stereo Mode	0
3	ADCKP	1 0	AD Bit Clock Pin (AD_CK) polarity is inverted AD Bit Clock Pin (AD_CK) polarity is not inverted	0
2	ADSYNCP	 1 0	DSP and PCM Formats in AD Interface Non Delayed format Delayed Format	0
		 1 0	Delayed, Left-aligned, Right-aligned and SPI Formats in AD Interface DA Sync Pin (DA_SYNC) polarity is inverted DA Sync Pin (DA_SYNC) polarity is not inverted	
1	ADMONO	1 0	Mono Mode: (L+R)/2 from ADC is sent to both channels in the Audio Interface Stereo Mode	0
0	ADHIZ	1 0	AD data pin (AD_DATA) is in high impedance state when no data is available AD data pin (AD_DATA) is forced to 0 when no data is available	0

4.8 Digital filters, software reset and master clock control

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR29 (1Dh)	Digital Filters Control	X	DAVOICE	DA96K	RXNH	ADVOICE	AD96K	ADNH	TXNH	0000 0000
CR30 (1Eh)	Soft Reset & AMCK Range	SWRES	X	X	X	AMCKSIN	CKRANGE(2:0)			0000 0000

Bits	Name	Value	CR29 Description	Def.
6	DAVOICE	1 0	DA path Voice RX filter is enabled (single channel, left used) DA path Audio filters are enabled	0
5	DA96K	1 0	DA path data rate is in the range 88 kHz to 96 kHz DA path data rate is in the range 8 kHz to 48 kHz	0
4	RXNH	1 0	DA path High pass Voice RX filter is disabled DA path High pass Voice RX filter is enabled (300Hz @ 8kHz rate)	0
3	ADVOICE	1 0	AD path Voice TX filter is enabled (single channel, left used) AD path Audio filters are enabled	0
2	AD96K	1 0	AD path data rate is in the range 88 kHz to 96 kHz AD path data rate is in the range 8 kHz to 48 kHz	0
1	ADNH	1 0	AD path Audio DC filter is disabled AD path Audio DC filter is enabled	0
0	TXNH	1 0	AD path High pass Voice TX filter is disabled AD path High pass Voice TX filter is enabled (300Hz @ 8kHz rate)	0

Bits	Name	Value	CR30 Description	Def.
7	SWRES	1 0	Software reset: All registers content is reset to the default value Control Register content is left unchanged	0
3	AMCKSIN	1 0	Signal at AMCK pin is a sinusoid Signal at AMCK pin is a square wave	0
2-0	CKRANGE(2:0)	 000 001 010 011 100 101	AMCK range — MCKCOEFF 4.0 MHz to 6.0 MHz — 8.0 6.0 MHz to 8.0 MHz — 6.0 8.0 MHz to 12.0 MHz — 4.0 12.0 MHz to 16.0 MHz — 3.0 16.0 MHz to 24.0 MHz — 2.0 24.0 MHz to 32.0 MHz — 1.5	000

4.9 Interrupt control and control interface SPI out mode

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR31 (1Fh)	interrupt Mask	VLSHEN	PUSHBEN	HSDETEN	VLSHMSK	PUSHBMSK	HSDETMSK	OVFMSK	PORMSK	0000 0000
CR32 (20h)	Interrupt Status	VLSH	PUSHB	HSDET	VLSHEV	PUSHBEV	HSDETEV	OVFEV	POREV	0000 0000
CR33 (21h)	Misc. Control	X	X	SPIOHIZ	SPIOSEL(1:0)		IRQCMOS	OVFDA	OVFAD	0000 0000

Bits	Name	Value	CR31 Description	Def.
7	VLSHEN	1 0	VLSH status can be seen at IRQ output VLSH status is masked	0
6	PUSHBEN	1 0	PUSHB status can be seen at IRQ output PUSHB status is masked	0
5	HSDETEN	1 0	HSDET status can be seen at IRQ output HSDET status is masked	0
4	VLSHMSK	1 0	VLSH event can be seen at IRQ output VLSH event is masked	0
3	PUSHBMSK	1 0	PUSHB event can be seen at IRQ output PUSHB event is masked	0
2	HSDETMSK	1 0	HSDET event can be seen at IRQ output HSDET event is masked	0
1	OVFMSK	1 0	OVF event can be seen at IRQ output OVF event is masked	0
0	PORMSK	1 0	POR event can be seen at IRQ output POR event is masked	0

Note: Value at IRQ pin is:

$$\text{IRQ} = \begin{cases} (1 \text{ or } Z) & \text{when } (\text{CR31 \& CR32}) = 00 \text{ hex} \\ 0 & \text{when } (\text{CR31 \& CR32}) \neq 00 \text{ hex} \end{cases}$$

Bits	Name	Read only	CR32 Description	Def.
7	VLSH*	1 0	V_{CCLS} is above 4.2 V V_{CCLS} is below 4.0 V	0
6	PUSHB*	1 0	Headset Button is pressed Headset Button is released	0
5	HSDET*	1 0	Headset Connector is inserted Headset Connector is not inserted	0
4	VLSHEV	1 0	VLSH bit has changed VLSH bit has not changed	0
3	PUSHBEV	1 0	Headset Button Status has changed Headset Button Status has not changed	0
2	HSDETEV	1 0	Headset Connector Status has changed Headset Connector Status has not changed	0
1	OVFEV	1 0	An Audio Data overflow has occurred in DSP No Audio Data overflow has occurred in DSP	0
0	POREV	1 0	Device was reset by Power-On-Reset Device was not reset by Power-On-Reset	0

Note: content of bits 4 to 0 in CR32 is cleared after reading, while it is left unchanged if accessed for writing.

*Bits 7 to 5 represent the status when the Control register is read, not when the event occurred.

Bits	Name	Val.	CR33 Description	Def.
5	SPIOHIZ	1 0	SPI Control Interface Out Pin is set to high impedance state when inactive SPI Control Interface Out Pin is set to zero when inactive	0
4-3	SPIOSEL(1:0)	 00 01 10 11	Out Pin Selection for SPI Control Interface No output. Control registers cannot be read in SPI mode SPI Output sent to IRQ pin SPI Output sent to DA_OCK pin SPI Output sent to AD_OCK pin	00
2	IRQCMOS	1 0	IRQ Interrupt Request Pin is set to CMOS (active low) IRQ Interrupt Request Pin is set to Pull Down	0
1	OVFDA	1 0	An overflow (saturation) occurred in DA path No overflow occurred in DA channel	0
0	OVFAD	1 0	An overflow (saturation) occurred in AD path No overflow occurred in AD channel	0

Note: content of bits 1 to 0 in CR33 is cleared after reading, while it is left unchanged if accessed for writing.

4.10 AGC

CR# (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0	Def.
CR34 (22h)	AGC Attack/Decay coeff.	AGCATT(3:0)				AGCDEC(3:0)				0000 0000
CR35 (23h)	AGC Control	X	ENAGCLIN	ENAGCMIC	AGCRANGE	AGCLEV(3:0)				0000 0000

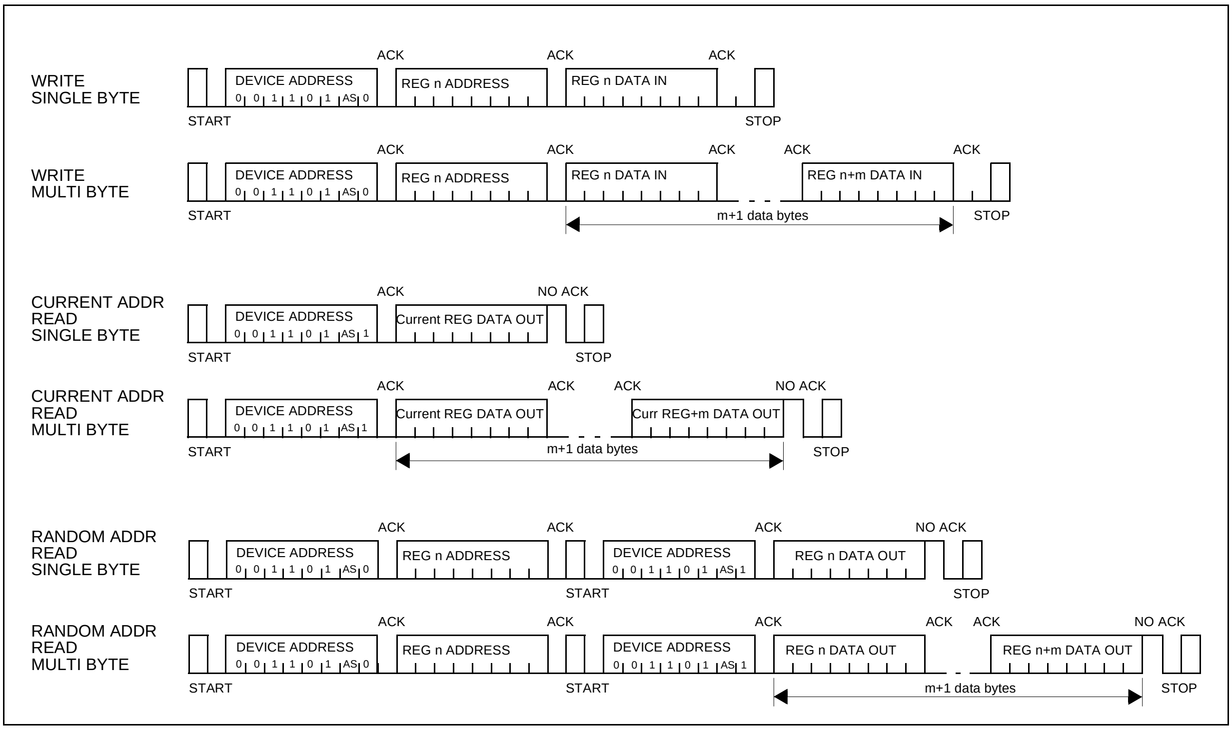
Bits	Name	Value	CR34 Description		Def.
7-4	AGCATT(3:0)		AGC Attack Time Constant; FS=AD data rate		0000
			Audio filter in AD path	Voice filter in AD path	
		0000	4096 / FS	8192 / FS	
		0001	2048 / FS	4096 / FS	
		0010	1365 / FS	2731 / FS	
		0011	1024 / FS	2048 / FS	
		0100	683 / FS	1365 / FS	
		0101	512 / FS	1024 / FS	
		0110	341 / FS	683 / FS	
		0111	256 / FS	512 / FS	
		1000	171 / FS	341 / FS	
		1001	128 / FS	256 / FS	
		1010	85 / FS	171 / FS	
		1011	64 / FS	128 / FS	
		1100	43 / FS	85 / FS	
		1101	32 / FS	64 / FS	
3-0	AGCDEC(3:0)		AGC Decay Time Constant; FS=AD data rate		0000
			Audio filter in AD path	Voice filter in AD path	
		0000	65536 / FS	131072/ FS	
		0001	32768 / FS	65536 / FS	
		0010	21845 / FS	43691 / FS	
		0011	16384 / FS	32768 / FS	
		0100	10923 / FS	21845 / FS	
		0101	8192 / FS	16384 / FS	
		0110	5461 / FS	10923 / FS	
		0111	4096 / FS	8192 / FS	
		1000	2731 / FS	5461 / FS	
		1001	2048 / FS	4096 / FS	
		1010	1365 / FS	2731 / FS	
		1011	1024 / FS	2048 / FS	
		1100	683 / FS	1365 / FS	
		1101	512 / FS	1024 / FS	
		1110	341 / FS	683 / FS	
		1111	256 / FS	512 / FS	

Bits	Name	Value	CR35 Description	Def.
6	ENAGCLIN	1 0	AGC control on AD path acts on Line In Gain AGC control on AD path does not act on Line In Gain	0
5	ENAGCMIC	1 0	AGC control on AD path acts on Mic Gain AGC control on AD path does not act on Mic Gain	0
4	AGCRANGE	1 0	AGC action range is -21.0 dB to +21.0 dB AGC action range is -10.5 dB to +10.5 dB	0
3-0	AGCLEV(3:0)	 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001	AGC requested output level -30.0dB Gain -30.0dB Gain -27.0dB Gain -24.0dB Gain -21.0dB Gain -18.0dB Gain -15.0dB Gain -12.0dB Gain -9.0dB Gain -6.0dB Gain	0000

5 Control Interface and Master Clock

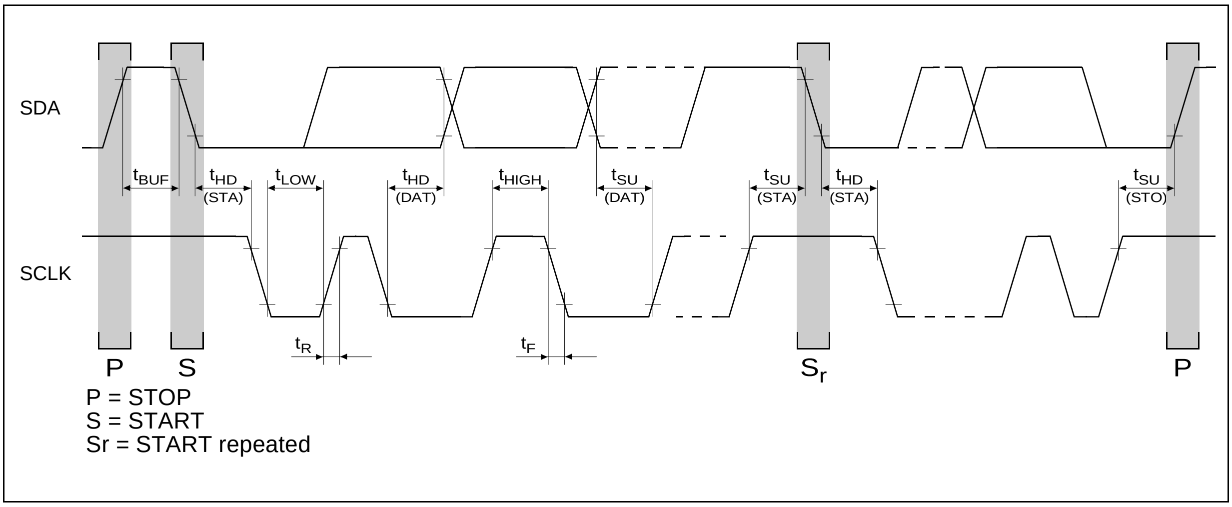
5.1 Control interface I²C mode

Figure 4. Control interface I²C format



Note: CMOD pin tied to GND

Figure 5. Control interface: I²C format timing

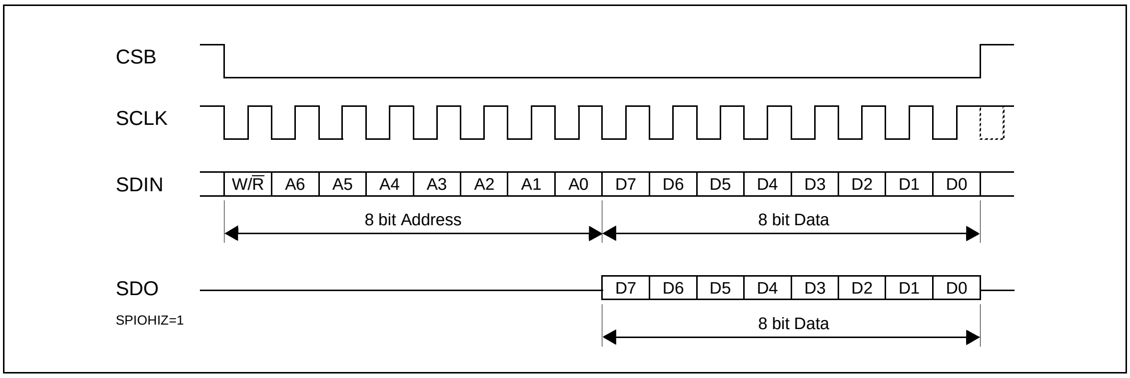


Control interface timing with I²C format

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Clock frequency				400	kHz
t_{HIGH}	Clock pulse width high		600			ns
t_{LOW}	Clock pulse width low		1300			ns
t_R	SDA and SCLK rise time				1000	ns
t_F	SDA and SCLK fall time				300	ns
$t_{HD:STA}$	Start condition hold time		600			ns
$t_{SU:STA}$	Start condition setup time		600			ns
$t_{HD:DAT}$	Data input hold time		0			ns
$t_{SU:DAT}$	Data input setup time		250			ns
$t_{SU:STO}$	Stop condition setup time		600			ns
t_{BUF}	Bus free time		1300			ns

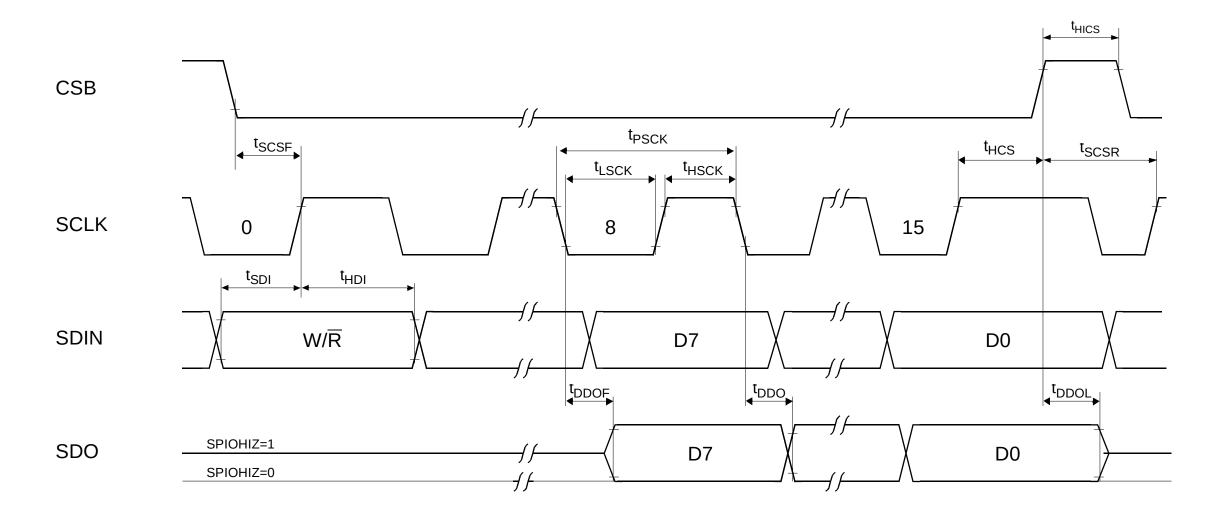
5.2 Control interface SPI mode

Figure 6. Control Interface SPI format(1)



1. CMOD pin tied to V_{CCIO}; SDO pin position selected with bits SPIOSEL in CR33.

Figure 7. Control interface: SPI format timing



Control interface signal timing with SPI format

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HICS}	CSB pulse width high		80			ns
t_{SCSR}	Setup time CSB rising edge to SCLK rising edge		20			ns
t_{SCSF}	Setup time CSB falling edge to SCLK rising edge		20			ns
t_{HCS}	Hold time CSB rising edge from SCLK rising edge		20			ns
t_{SDI}	Setup time SDIN to SCLK rising edge		20			ns
t_{HDI}	Hold time SDIN from SCLK rising edge		20			ns
t_{DDOF}	SDO first Delay time from SCLK falling edge				30	ns
t_{DDO}	SDO Delay time from SCLK falling edge				20	ns
t_{DDOL}	SDO Delay time from CSB rising edge				30	ns
t_{PSCK}	Period of SCK		100			ns
t_{HSCK}	SCK pulse width high	Measured from V_{IH} to V_{IH}	40			ns
t_{LSCK}	SCK pulse width low	Measured from V_{IL} to V_{IL}	40			ns

5.3 Master clock timing

AMCK timing

Symbol	Parameter	AMCK range	Min.	Typ.	Max.	Unit
t_{CKDC}	AMCK duty cycle	4 MHz-8 MHz 8 MHz-32 MHz	45 40		55 60	% %

6 Audio Interfaces

Figure 8. Audio interfaces formats: delayed, left and right justified

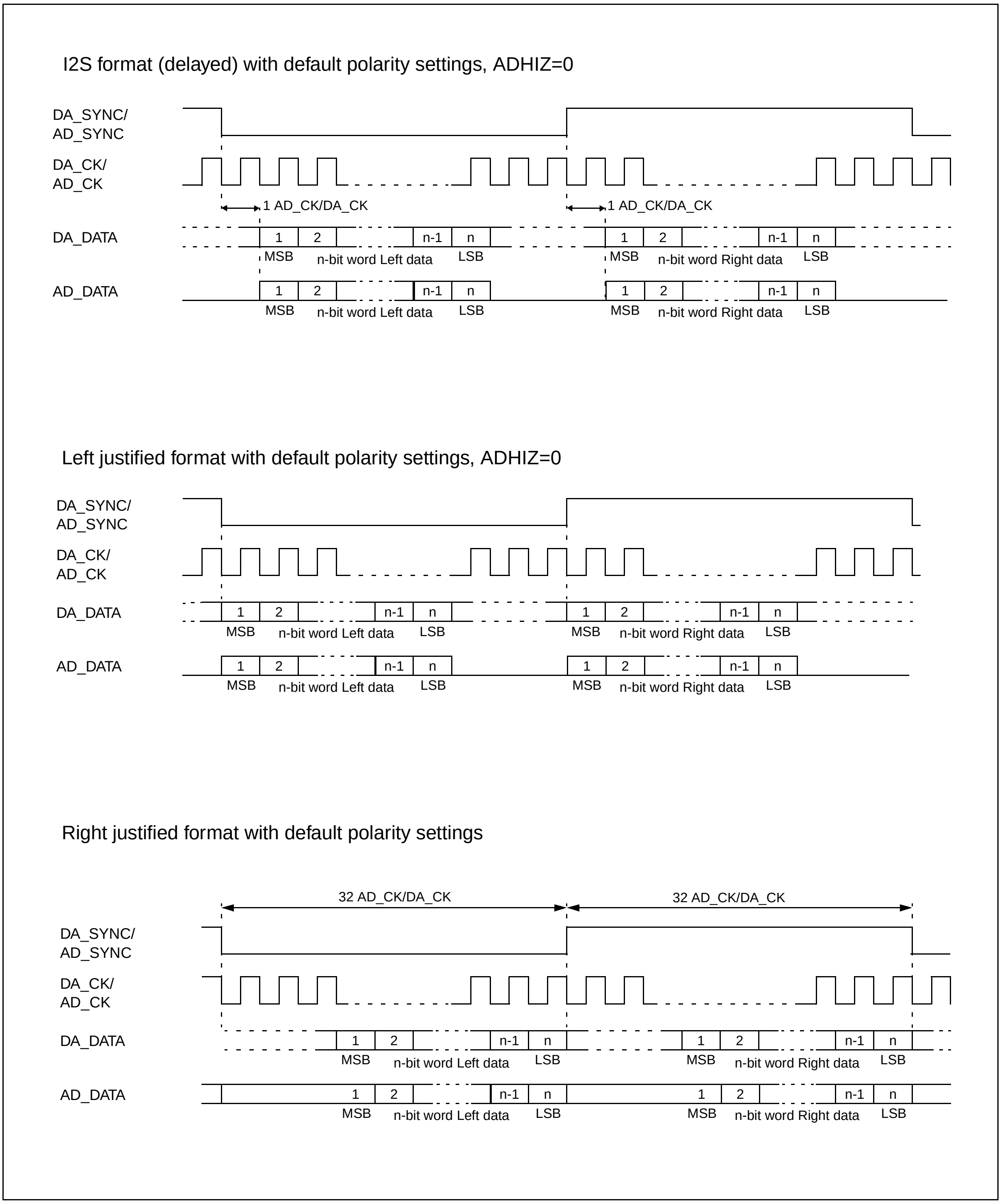


Figure 9. Audio interfaces formats: DSP, SPI and PCM

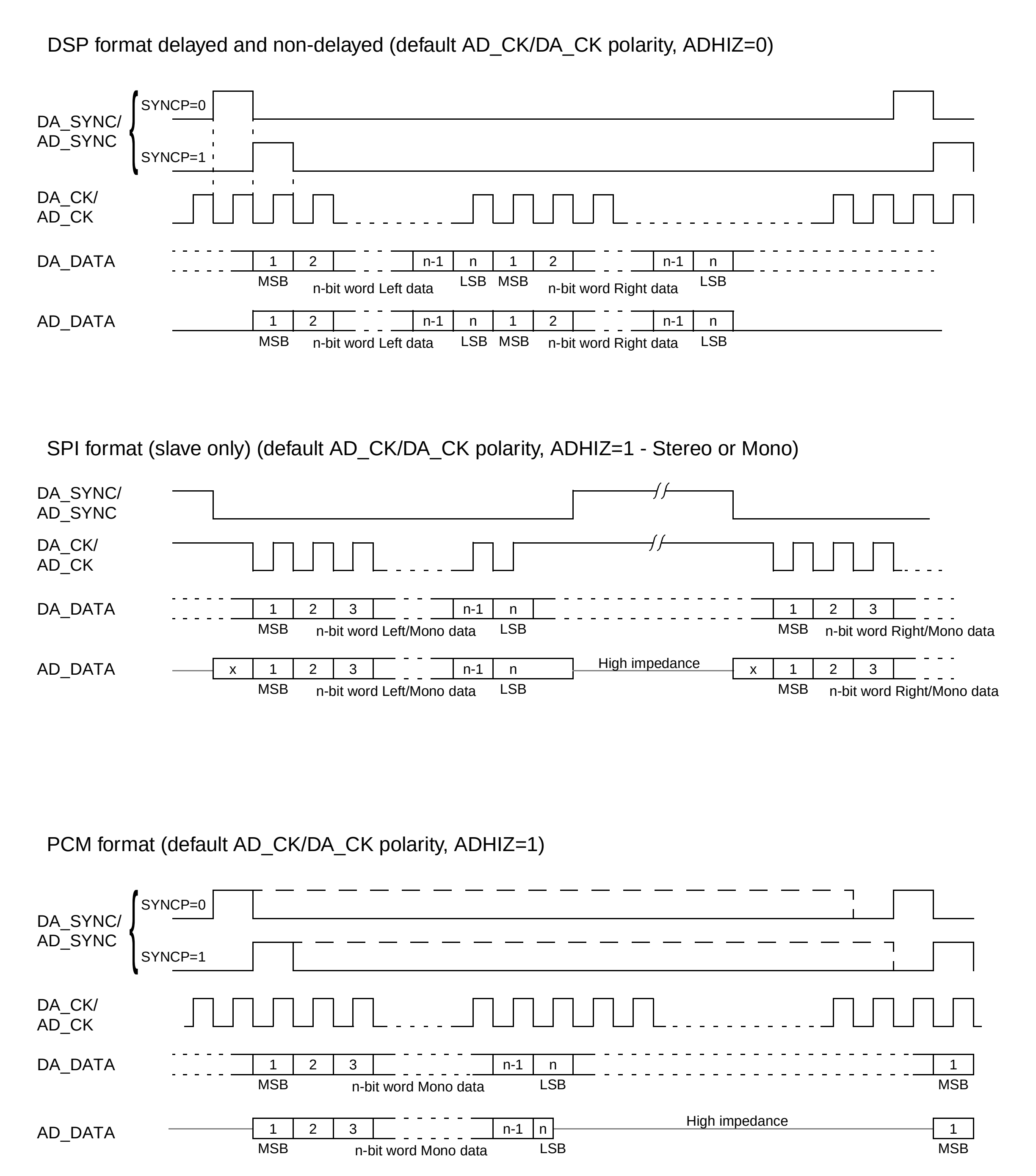


Figure 10. Audio interface timings: Master mode

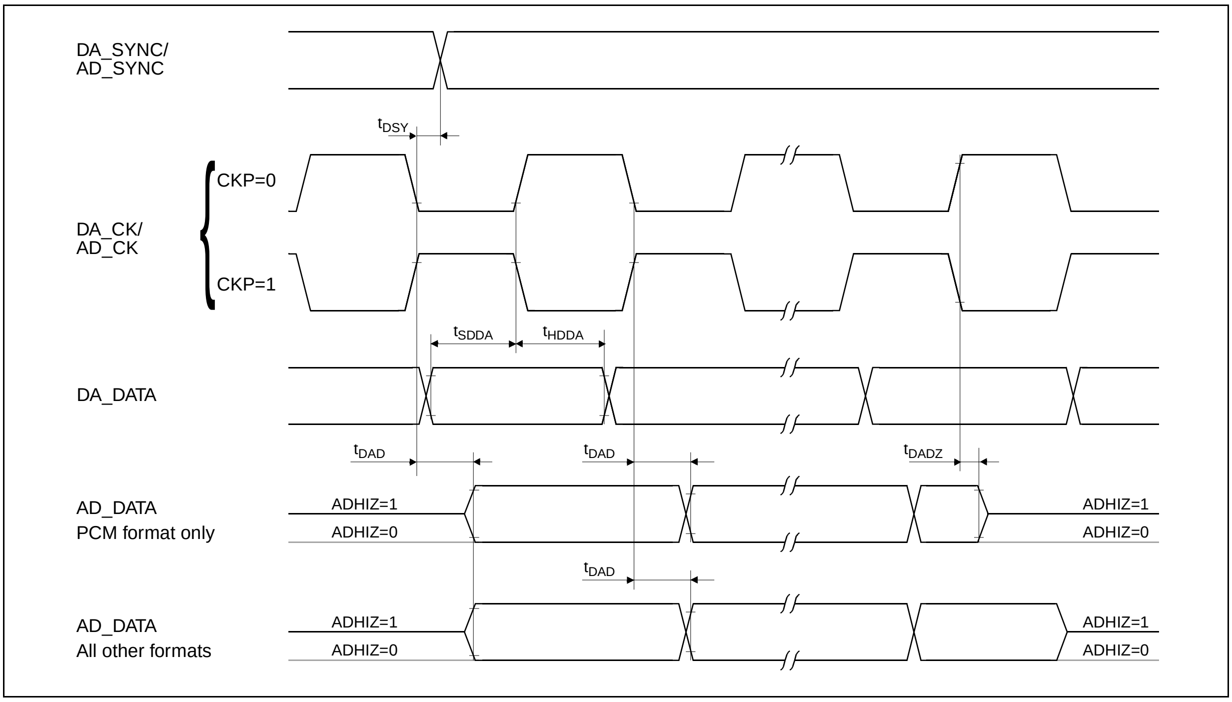
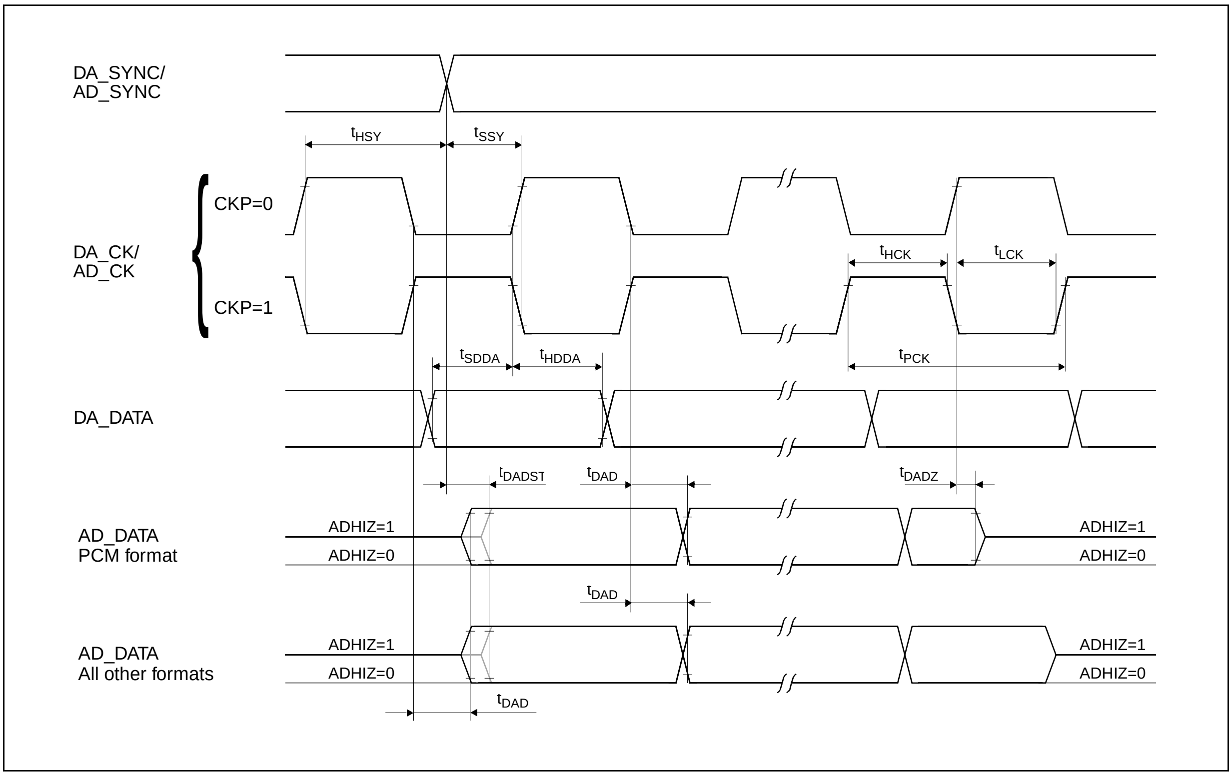


Figure 11. Audio interface timing: Slave mode



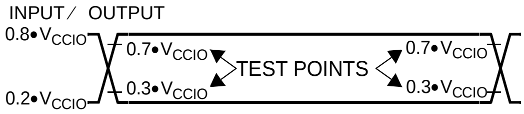
Audio interface signals timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{DSY}	Delay of AD_SYNC/ DA_SYNC edge from AD_CK/DA_CK active edge	Master Mode			10	ns
t_{SDDA}	Setup time DA_DATA to DA_CK active edge		10			ns
t_{HDDA}	Hold time DA_DATA from DA_CK active edge		10			ns
t_{DAD}	Delay of AD_DATA edge from AD_CK active edge				30	ns
t_{DADST}	Delay of the first AD_DATA edge from AD_SYNC active edge	AD_SYNC active edge comes after AD_CK active edge			30	ns
t_{DADZ}	Delay of AD_DATA high impedance from AD_SYNC inactive edge	PCM format	10		50	ns
t_{SSY}	Setup time AD_SYNC/ DA_SYNC to AD_CK/ DA_CK active edge	Slave Mode	20			ns
t_{HSY}	Hold time AD_SYNC/ DA_SYNC from AD_CK/ DA_CK active edge	Slave Mode	20			ns
t_{PCK}	Period of AD_CK/DA_CK	Slave Mode	100			ns
t_{HCK}	AD_CK/DA_CK pulse width high	Measured from V_{IH} to V_{IH}	40			ns
t_{LCK}	AD_CK/DA_CK pulse width low	Measured from V_{IL} to V_{IL}	40			ns

7 Timing Specifications

Unless otherwise specified, V_{CCIO} = 1.71 V to 2.7 V,T_{amb} = -30°C to 85°C, max capacitive load 20 pF; typical characteristics are specified at V_{CCIO} = 2.4 V, T_{amb} = 25 °C; all signals are referenced to GND, see Note below figure for timing definitions.

Figure 12. A.C. testing input-output waveform



AC Testing: inputs are driven at 0.8•V_{CCIO} for a logic '1' and 0.2•V_{CCIO} for a logic '0'.
Timing measurements are made at 0.7•V_{CCIO} for a logic '1' and 0.3•V_{CCIO} for a logic '0'.

Note: A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purpose of this specification the following conditions apply (see Figure 12 above):
a) All input signal are defined as: V_{IL} = 0.2•V_{CCIO}, V_{IH} = 0.8•V_{CCIO}, t_R < 10ns, t_F < 10ns.
b) Delay times are measured from the inputs signal valid to the output signal valid.
c) Setup times are measured from the data input valid to the clock input invalid.
d) Hold times are measured from the clock signal valid to the data input invalid.

Note: All timing specifications subject to change.

8 Operative Ranges

8.1 Absolute maximum ratings

Parameter	Value	Unit
V_{CC} or V_{CCIO} to GND	-0.5 to 3.6	V
V_{CCA} or V_{CCP} to GND	-0.5 to 5	V
V_{CCLS} to GND	-0.5 to 7	V
Voltage at Analog Inputs ($V_{CCA} \leq 3.3V$)	GND-0.5 to V_{CCA}+0.5	V
Maximum Power delivered to the load from LSP/N	500	mW
Peak Current at HPR,HPL	100	mA
Current at V_{CCP}, V_{CCLS}, GNDP	350	mA
Current at any digital output	50	mA
Voltage at any digital input ($V_{CCIO} \leq 2.7V$); limited at ± 50mA	GND-0.5 to V_{CCIO}+0.5	V
Storage temperature range	-64 to 150	°C
Operating temperature range[1]	-30 to 85	°C

1. in some operating conditions the temperature can be limited to 70 °C. See Loudspeaker Driver description from *Section 3.9* for details.

8.2 Operative supply voltage

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}	Digital supply		1.71	2.7	V
V_{CCA}	Analog supply Note: $V_{CCA} \geq V_{CC}$	A24V=0 (bit 1 in CR0) A24V=1 (bit 1 in CR0)	2.7 2.4	3.3 2.7	V V
V_{CCIO}	Digital I/O supply	D12V=0 (bit 0 in CR0) D12V=1 (bit 0 in CR0)	1.71 1.2	V_{CC} 1.8	V V
V_{CCP}	Stereo power drivers supply		V_{CCA}	3.3	V
V_{CCLS}	Mono power driver supply		V_{CCA}	5.5	V
V_G	Single supply voltage range	$V_{CC}=V_{CCA}=V_{CCIO}=V_{CCP}=V_{CCLS}$ A24V=1 (bit 1 in CR0)	2.4	2.7	V

8.3 Power Dissipation

Unless otherwise specified, $V_{CCP} = V_{CCLS} = V_{CCA}$ = 2.7V to 3.3V, $V_{CCIO} = V_{CC}$ = 1.71V to 2.7V, T_{amb} = -30°C to 85°C, all analog outputs not loaded; typical characteristics are specified at $V_{CCIO} = V_{CC}$ = 1.8V, $V_{CCP} = V_{CCLS} = V_{CCA}$ = 2.7V, T_{amb} = 25°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POFF	Power Down Dissipation	No Master Clock AMCK=13MHz		0.2 2.9		µW µW
PAD	Stereo ADC power			26.3		mW
PDA	Stereo DAC power			22.6		mW
PDAAD	Stereo ADC+DAC power			44.0		mW
PAA	Stereo Analog Path power			13.8		mW

8.4 Typical power dissipation

T_{amb} = 25°C; Analog Supply: $V_{CCP} = V_{CCLS} = V_{CCA}$ = 2.7V; Digital Supply:$V_{CCIO} = V_{CC}$ = 1.8V

Full scale signal in every path, 20kΩ load at analog outputs.

No Master Clock

N.	Function	CR0-CR2 setting	Other settings	Supply	Current	Power
1	Power Down	CR0=0x00 CR1=0x00 CR2=0x00		Analog: Digital: **Total:**	0.02 µA 0.20 µA	0.05 µW 0.36 µW **0.41 µW**
2	Stereo analog path (Mic-LO)	CR0=0xD0 CR1=0x0C CR2=0xC0	MICLO=1 MICSEL=2	Analog: Digital: **Total:**	4.3 mA 2.0 µA	11.6 mW 0.0 mW **11.6 mW**
3	Stereo analog path (Mic-Mixer-LO)	CR0=0xD0; CR1=0x0C; CR2=0xC3	MIXMIC=1 MICSEL=2	Analog: Digital: **Total:**	5.4 mA 2.0 µA	14.6 mW 0.0 mW **14.6 mW**

Master clock AMCK = 13 MHz

N.	Function	CR0-CR2 setting	Other settings	Supply	Current	Power
4	Power Down	CR0=0x00 CR1=0x00 CR2=0x00		Analog: Digital: **Total:**	0.02 µA 2.20 µA	0.05 µW 3.96 µW **4.01 µW**
5	Stereo ADC	CR0=0xE8 CR1=0xCC CR2=0x00	MICSEL=1 ADMIC=1	Analog: Digital: **Total**:	7.9 mA 2.8 mA	21.3 mW 5.0 mW **26.3 mW**
6	Stereo DAC	CR0=0xE8 CR1=0x30 CR2=0x33	MIXDAC=1	Analog: Digital: **Total:**	6.1 mA 3.8 mA	16.5 mW 6.8 mW **23.3 mW**
7	Stereo analog path (Mic-LO)	CR0=0xE8 CR1=0x0C CR2=0xC0	MICLO=1 MICSEL=2	Analog: Digital: **Total:**	4.8 mA 0.8 mA	13.0 mW 1.4 mW **13.8 mW**
8	Stereo ADC Stereo DAC	CR0=0xE8 CR1=0xFC CR2=0x33	MICSEL=2 ADMIC=1 MIXDAC=1	Analog: Digital: **Total:**	13.5 mA 5.8 mA	36.5 mW 10.4 mW **46.9 mW**
9	Stereo ADC Stereo DAC Stereo analog path	CR0=0xE8 CR1=0xFF CR2=0xF3	LINSEL=2; MICSEL=2 ADLIN=1;MIXDAC=1 MICLO=1	Analog: Digital: **Total:**	15.2 mA 5.8 mA	41.0 mW 10.4 mW **51.4 mW**
10	Voice TX+RX	CR0=0xE8 CR1=0xA8 CR2=0x06	MICSEL=2; LSMODE=2 ADMIC=1 MIXDAC=1 ADVOICE=1 DAVOICE=1	V_{CCA},V_{CCP}: V_{CCLS}: Digital **Total:**	6.8 mA 1.3 mA 2.5 mA	18.4 mW 5.5 mW 4.5 mW **28.4 mW**

9 Electrical Characteristics

Unless otherwise specified, V_{CCIO} = 1.71 V to 2.7 V, T_{amb} = -30°C to 85°C; typical characteristic are specified at V_{CCIO} = 2.0 V, T_{amb} = 25°C; all signals are referenced to GND.

9.1 Digital interfaces

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	All digital inputs DC AC			0.3•V_{CCIO} 0.2•V_{CCIO}	V V
V_{IH}	Input high voltage	All digital inputs, DC AC	0.7•V_{CCIO} 0.8•V_{CCIO}			V V
V_{OL}	Output low voltage	All digital outputs I_L = 10µA I_L = 2µA			0.1 0.4	V V
V_{OH}	Output high voltage	All digital outputs I_L = 10µA I_L = 2µA	V_{CCIO}-0.1 V_{CCIO}-0.4			V V
I_{IL}	Input low current	Any digital input, GND < V_{IN} < V_{IL}	-1		1	µA
I_{IH}	Input high current	Any digital input, V_{IH} < V_{IN} < V_{CCIO}	-1		1	µA
I_{OZ}	Output current in high impedance (Tristate)	Tristate outputs	-1		1	µA

Note: *See Figure 12: A.C. testing input-output waveform on page 49.*

9.2 AMCK with sinusoidal input

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{AMCK}	Minimum External Capacitance	AMCKSIN=1, see CR30	100			pF
V_{AMCK}	AMCK sinusoidal voltage swing	AMCKSIN=1, see CR30	0.5		V_{CCIO}	V_{PP}

9.3 Analog interfaces

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{MIC}	MIC input leakage	GND< V_{MIC}< V_{CCA}	-100		+100	µA
R_{MIC}	MIC input resistance		30	50		kΩ
R_{LIN}	Line in input resistance		30			kΩ
R_{LHP}	Headphones (HP) drivers load resistance	HPL, HPR to GNDP or VCMHP	14.4	16/32		Ω
C_{LHP}	Headphones (HP) drivers load capacitance	HPL, HPR to GNDP or VCMHP			50 50*	pF nF
R_{LLS}	Loudspeaker (LS) differential driver load resistance	LSP to LSN	6.4	8		Ω
C_{LLS}	Loudspeaker (LS) differential driver load capacitance	LSP to LSN			50 50*	pF nF
V_{OFFLS}	Differential offset voltage at LSP, LSN	R_L = 50Ω	-50		+50	mV
R_{LOL}	Line out (OL) diff./single-ended driver load resistance	OLP/ORP to OLN/ORN or OLP/ORP to GND (decoupled)	1			kΩ
C_{LOL}	Line out (OL) diff./single-ended driver load capacitance	OLP/ORP to OLN/ORN or OLP/ORP to GND			TBD	

* with series resistor

9.4 Headset plug-in and push-button detector

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
HD_{VL}	Plug-in detected	Voltage at HDET			V_{CCA}-1	V
HD_{VH}	Plug-in undetected	Voltage at HDET	V_{CCA}-0.5			V
HD_H	Plug-in detector hysteresis			100		mV
PB_{VL}	Push-button pressed	Voltage at HDET			0.5	V
PB_{VH}	Push-button released	Voltage at HDET	1			V
PB_D	Push-button de-bounce time		15		50	ms

9.5 Microphone bias

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{MBIAS}	MBIAS output voltage		1.95	2.1	2.25	V
I_{MBIAS}	MBIAS output current	From MBIAS to ground			600	µA
R_{MBIAS}	MBIAS output load		3.5			kΩ
C_{MBIAS}	MBIAS output capacitance				150	pF
PSR_{MB4} PSR_{MB20}	MBIAS power supply rejection	f<4kHz f<20kHz	60 50			dB dB

9.6 Power supply rejection ratio

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PSR_{L20} PSR_{L200}	PSRR V_{CCLS}	Each output(LSP, LSN) f<20kHz f<200kHz		65 47		dB dB
PSR_{PH} PSR_{POS} PSR_{POD}	PSRR V_{CCP}	Headphones f<20kHz Line out single ended f<20kHz Line out differential f<20kHz		65 TBD TBD		dB dB dB
PSR_{AM} PSR_{AL}	PSRR V_{CCA}	Mic input f<20kHz Line In f<20kHz		50 TBD		dB dB

9.7 LS gain limiter

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VLS_{LIMH}	High voltage at V_{CCLS} (VLSH=1)	V_{CCLS} raising		4.2		V
VLS_{LIML}	Low voltage at V_{CCLS} (VLSH=0)	V_{CCLS} falling		4.0		V
VLS_{LIMD}	V_{CCLS} Hysteresis			200		mV

Note: See CR32 for VLSH definition. See Loudspeaker driver description in *Section 3.9* for details.

10 Analog Input/output Operative Ranges

10.1 Analog levels

Reference full scale analog levels

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0dBFS level	2.7V < V_{CCA} < 3.3V		12 4		dBV_{pp} V_{pp}
	0dBFS level low voltage mode	2.4V < V_{CCA} < 2.7V		10 3.18		dBV_{pp} V_{pp}

10.2 Microphone input levels

Absolute levels at pins connected to preamplifiers

Analog supply range: 2.7 V < V_{CCA} < 3.3 V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Overload level, single ended	MIC gain = 0 to 6dB		707 2 -6		mV_{RMS} V_{pp} dBFS
	Overload level,single ended, versus MIC gain	MIC gain > 6dB		−(MIC_Gain)		dBFS
	Overload level, differential	MIC gain = 0dB		1.41 4 0		mV_{RMS} V_{pp} dBFS
	Overload level, differential, versus MIC gain	MIC gain > 0dB		−(MIC_Gain)		dBFS

Note: When 2.4 V < V_{CCA} < 2.7 V, voltage values are reduced by 2dB.

10.3 Line input levels

Absolute levels at pins connected to the line-in amplifiers

Analog supply range: 2.7 V < V_{CCA} < 3.3 V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Overload level, single ended	Line in gain from -20dB to 6dB		707 2 -6		mV_{RMS} V_{pp} dBFS
	Overload level (single ended) versus line in gain	Line in gain > 6dB		−(Line_In_Gain)		dBFS
	Overload level (differential)	Line in gain from -20dB to 0dB		1.41 4 0		mV_{RMS} V_{pp} dBFS
	Overload level (differential) versus line in gain	Line in gain > 0dB		−(Line_In_Gain)		dBFS

Note: When 2.4 V < V_{CCA} < 2.7 V, the values are reduced by 2dB

10.4 Line output levels

Absolute levels at OLP/OLN, ORP/ORN

Analog supply range: 2.7 V < V_{CCA} < 3.3 V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Output level, single ended	0 dB gain Full scale digital input		707 2 -6		mV_{RMS} V_{pp} dBFS
	Output level, differential	0 dB Gain Full scale digital input		1.41 4 0		mV_{RMS} V_{pp} dBFS

Note: When 2.4 V < V_{CCA} < 2.7 V, the values are reduced by 2dB

10.5 Power output levels HP

Absolute levels at HPL - HPR

Analog supply range: 2.7 V < V_{CCA} < 3.3 V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Output level	-6dB gain Full scale digital input		707 2 -6		mV_{RMS} V_{pp} dBFS
	Max output power(1)	16 Ω load V_{CCP} > 3.2 V	40			mW

Note: When 2.4 V < V_{CCA} < 2.7 V, the values are reduced by 2dB

10.6 Power output levels LS

Absolute levels at LSP - LSN (Differential)

Analog supply range: 2.7 V < V_{CCA} < 3.3 V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Output level	0 dB gain Full scale digital input		1.41 4 0		V_{RMS} V_{pp} dBFS
	Max output power(1)	8 Ω load V_{CCLS} > 4V	500			mW

1. In some operating conditions the maximum output power can be limited. See "*Section 8.1: Absolute maximum ratings*" and "Loudspeaker Driver" description from *Section 3.9: Analog output drivers* for details.

Note: When 2.4 V < V_{CCA} < 2.7 V, the values are reduced by 2dB

11 Stereo Audio ADC Specifications

Typical measures at V_{CCA}=V_{CCP}=V_{CCLS}=2.7V; V_{CCIO}=V_{CC}=1.8 V; Tamb=25° C;13 MHz AMCK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ADN	Resolution				20	Bits
ADDRM ADDRLI	Dynamic range	20Hz to 20kHz, A-weighted Measured at -60dBFS MIC input, 21dB gain Line-In, 0dB gain	87 89	91 93		dB dB
ADSNA ADSN	Signal to noise ratio	Max level at MIC input, 21dB gain A-weighted Unweighted (20 Hz to 20 kHz)		90 86		dB dB
	Input referred ADC noise	A-weighted Mic input 0dB Gain Mic input 21dB Gain Mic input 39dB Gain Line in input 0dB Gain Line in input 18dB Gain		37 3.3 1.9 30 7.5		µV µV µV µV µV
ADTHD	Total harmonic distortion	Max level at MIC input, 21dB gain		0.001	0.003	%
	Deviation from linear phase	Measurement bandwidth 20Hz to 20kHz, Fs= 48kHz. Combined digital and analog filter characteristics			1	Deg
ADf_{PB}	Passband	Combined digital and analog filter characteristics AD96K=0	0		0.45Fs	kHz
	Passband ripple	Combined digital and analog filter characteristics AD96K=0			0.2	dB
ADf_{SB}	Stopband	Combined digital and analog filter characteristics AD96K=0	0.55Fs			kHz
	Stopband Attenuation	Measurement bandwidth up to 3.45Fs. Combined digital and analog filter characteristics, AD96K=0	60			dB
ADt_{gd}	Group delay	Audio filters, 96kHz FS Audio filters, 48kHz FS Audio filters, 8kHz FS		0.11 0.4 2.6		ms ms ms
	Interchannel isolation			90		dB
	Interchannel gain mismatch				0.2	dB
	Gain error				0.5	dB

Note: When 2.4 V < V_{CCA} < 2.7 V, the values are reduced by 2dB

12 Stereo Audio DAC Specifications

Typical measures at V_{CCA}=V_{CCP}=V_{CCLS}=2.7V; V_{CCIO}=V_{CC}=1.8V; Tamb=25° C;13MHz AMCK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DAN	Resolution				20	Bits
DADR	Dynamic range	20Hz to 20kHz, A-weighted. Measured at -60dBFS Differential line out Single-ended line out HPL/HPR to GND or VCMHP LSP-LSN	90	95 93 94 94		dB dB dB dB
DASNA DASN	Signal to noise ratio	2Vpp output HPL, HPR gain set to -6dB, 16Ω load A-weighted Unweighted (20 Hz to 20 kHz)		94 90		dB dB
DATHDL	Total harmonic distortion Worst case load	$2V_{pp}$ output HPL, HPR gain set to -6dB, 16Ω load		0.02	0.04	%
DATHD	Total harmonic distortion	$2V_{pp}$ output, HPL, HPR gain set to -6dB, 1kΩ load		0.004		%
	Deviation from linear phase	Measurement bandwidth 20Hz to 20kHz, Fs= 48kHz. Combined digital and analog filter characteristics			1	Deg
DAf_{PB}	Passband	Combined digital and analog filter characteristics, DA96K=0	0		0.45Fs	kHz
	Passband ripple	Combined digital and analog filter characteristics, DA96K=0			0.2	dB
DAf_{SB}	Stopband	Combined digital and analog filter characteristics, DA96K=0	0.55Fs			kHz
	Stopband attenuation	Measurement bandwidth up to 3.45Fs. Combined digital and analog filter characteristics, DA96K=0	50			dB
TSF	Transient suppression filter cut-off frequency		15		23	Hz
	Out of band noise	Measurement bandwidth 20 kHz to 100 kHz. Zero input signal		-85		dBr
DAt_{gd}	Group delay	Audio filters, 96kHz FS Audio filters, 48kHz FS Audio filters, 8kHz FS		0.09 0.4 2.6		ms ms ms
	Interchannel isolation	2Vpp output HPR, HPL unloaded HPR, HPL with 16Ω to VCMHP		100 60		dB dB

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Interchannel gain mismatch				0.2	dB
	Gain error				0.5	dB
SUT	Startup time from power up	FS=48 kHz Line out HPL/R out		1 10		ms ms

Note: When 2.4 V < V_{CCA} < 2.7 V, values are reduced by 2 dB

13 AD to DA Mixing (Sidetone) Specifications

Typical measures at V_{CCA}=V_{CCP}=V_{CCLS}=2.7V; V_{CCIO}=V_{CC}=1.8V; Tamb=25° C;13MHz AMCK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
STDEL	AD to DA mixing (sidetone) delay	Valid for audio and voice filters		5	10	µs

14 Stereo Analog-only Path Specifications

Measured at differential line-out, ENOSC=1, No master clock.
Typical measures at V_{CCA}=V_{CCP}=V_{CCLS}=2.7V; V_{CCIO}=V_{CC}=1.8V; Tamb=25° C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AADRM AADRLI	Dynamic range	20Hz to 20kHz, A-weighted. Measured at -60dBFS MIC input, 21dB gain Line-In, 0dB gain	90 90	95 97		dB dB
AASNA AASN	Signal to noise ratio	Max level at line-in input, 0dB gain, A-weighted Unweighted (20 Hz to 20 kHz)		97 94		dB dB
AATHD	Total harmonic distortion	1kHz @ 0dBFS MIC input, 21dB gain Line-in input, 0dB gain		0.003 0.004	0.01 0.02	% %

Note: When 2.4V<V_{CCA}<2.7V, the values are reduced by 2dB.

15 ADC (TX) & DAC (RX) Specifications With Voice Filters Selected

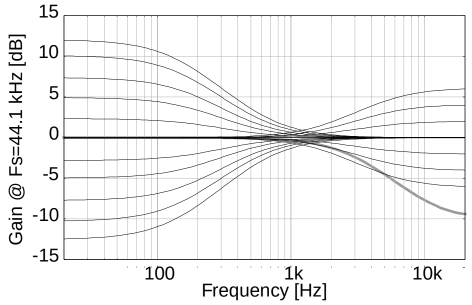
Typical measures at $V_{CCA}=V_{CCP}=V_{CCLS}=2.7V$; $V_{CCIO}=V_{CC}=1.8V$; Tamb=25° C;13MHz AMCK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
		300Hz to 3.4kHz; 1kHz @ -60dBFS				
TXDR	Dynamic range	TX Path, MIC input, 21dB gain	86	89		dB
RXDR		RX Path, LS Output, 0dB gain	83	86		dB
		300Hz to 3.4kHz; 1kHz @ 0dBFS				
TXSN	Signal to noise ratio	TX Path, MIC input, 21dB gain		88		dB
RXSN		RX Path, LS Output, 0dB gain		86		dB
		1kHz @ 0dBFS				
THD	THD	TX Path, MIC input, 21dB gain		<0.001		%
		RX Path, LS Output, 0dB gain		0.005		%
TXG	TX gain mask	f=60Hz			-30	dB
		f=100Hz			-24	dB
		f=200Hz			-6	dB
		f=300Hz	-1.5		0.5	dB
		f=400Hz-3000Hz	-0.5		0.5	dB
		f=3400Hz	-1.5		0.0	dB
		f=4000H			-14	dB
		f=4600Hzz			-35	dB
		f=8000Hz			-47	dB
RXG	RX gain mask	f=60Hz			-20	dB
		f=100Hz			-12	dB
		f=200Hz			-2	dB
		f=300Hz	-1.5		0.5	dB
		f=400Hz-3000Hz	-0.5		0.5	dB
		f=3400Hz	-1.5		0.0	dB
		f=4000Hz			-14	dB
		f=5000Hz			-50	dB
	RX out of band noise	Measurement bandwidth 4kHz to 100kHz. Zero input signal		-85		dBr
	Group delay	TX path		0.32		ms
		RX path		0.28		ms

Note: When $2.4V<V_{CCA}<2.7V$, the values are reduced by 2dB

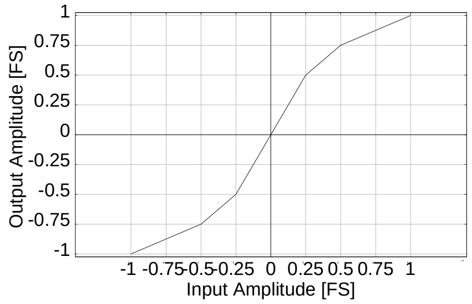
16 Typical Performance Plots

Figure 13. Bass treble control, de-emphasis filter



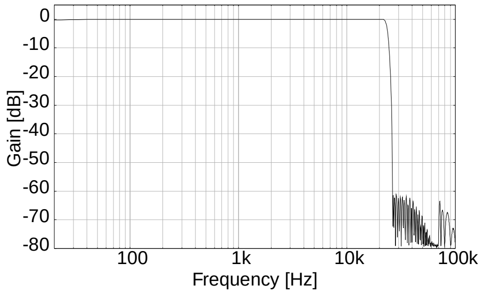
Bass and treble gains are independently selectable in any combination.
The de-emphasis filter (thick line, alternative to treble control) compensates for pre-emphasis used on some audio CDs.
Gain error < 0.1dB. Filter characteristics at Fs=44.1kHz are plotted

Figure 14. Dynamic compressor transfer function



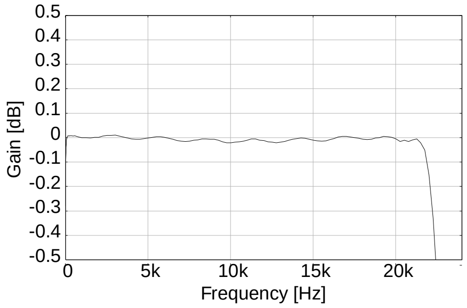
Audio signal transfer function when the Dynamic Compressor is active.

Figure 15. ADC audio path measured filter response



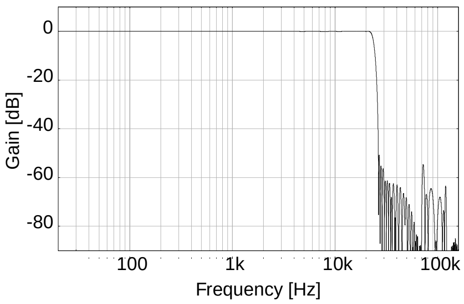
48 kHz sample rate.
Full ADC path Frequency response up to 100 kHz.

Figure 16. ADC in band audio path measured filter response



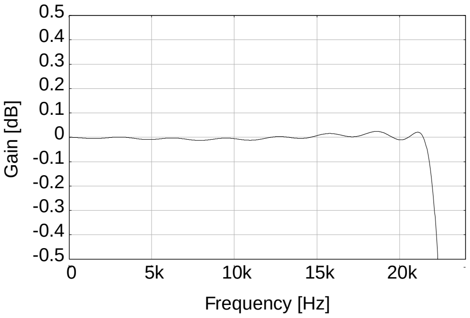
48 kHz Sample Rate.
In band Frequency response

Figure 17. DAC digital audio filter characteristics



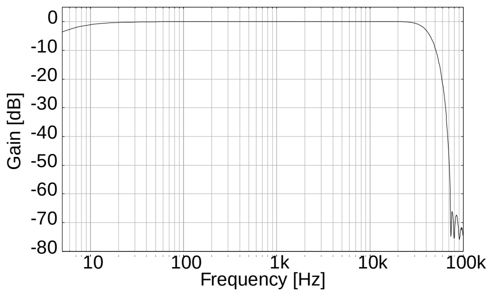
DA96K=0; 48 kHz Sample Rate
Frequency response up to 166kHz (3.45 Fs @ 48kHz sampling rate)

Figure 18. DAC in band digital audio filter characteristics



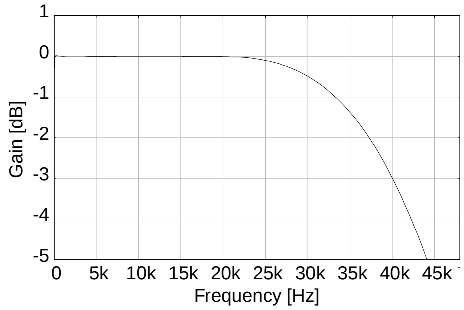
48 kHz Sample Rate
In band Frequency response

Figure 19. ADC 96 kHz audio path measured filter response



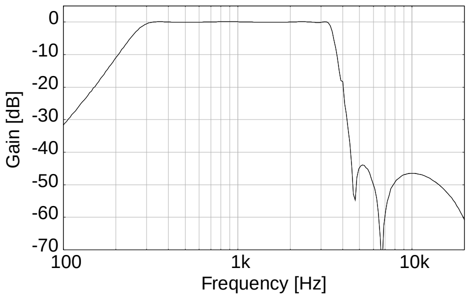
The plot is extended down to 5 Hz to show the high pass filter implemented in the ADC 96 kHz sample rate,
96 kHz audio filter selected signal from Mic input

Figure 20. ADC 96 kHz audio in-band measured filter response



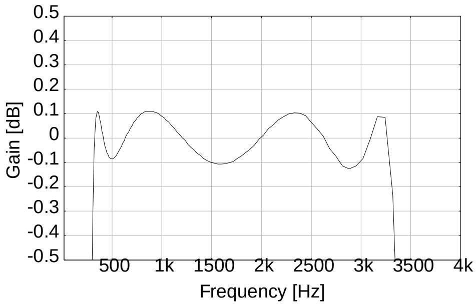
96 kHz sample rate,
96 kHz audio filter selected signal from Mic input.

Figure 21. ADC voice TX path measured filter response



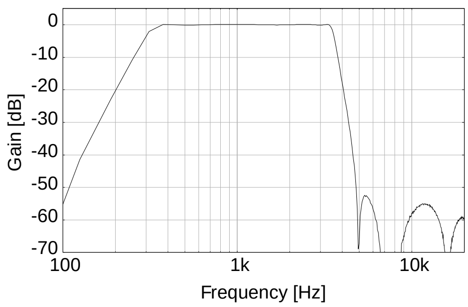
8 kHz Sample rate, tx voice filter selected.
Signal from Mic input

Figure 22. ADC voice TX path measured in-band filter response



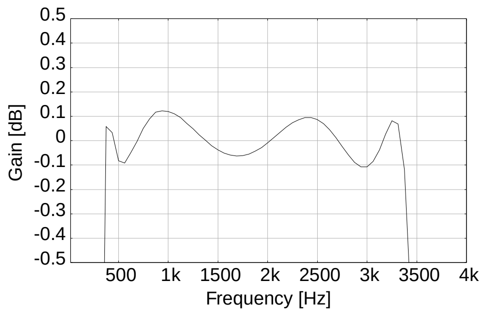
8 kHz sample rate, tx voice filter selected signal from Mic input.

Figure 23. DAC voice (RX) digital filter characteristics



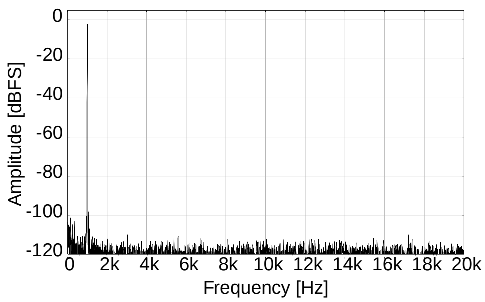
8 kHz sample rate, rx voice filter

Figure 24. DAC voice (RX) in-band digital filter characteristics



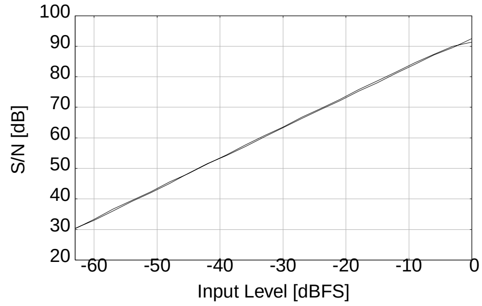
8 kHz sample rate, rx voice filter

Figure 25. ADC path FFT



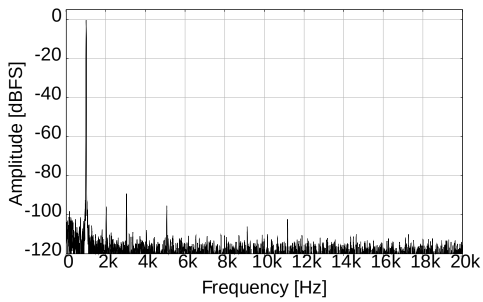
12 MHz master clock.
Differential input at Mic preamplifier, 21 dB gain.
48 kHz sampling rate.
Both channels active

Figure 26. ADC S/N versus input-level



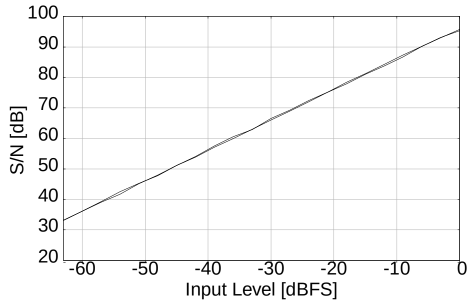
12 MHz master clock
Differential input at Line-In Amplifier, 0 dB Gain.
48 kHz Sampling Rate
A-Weighted, Both channels active

Figure 27. DAC path FFT



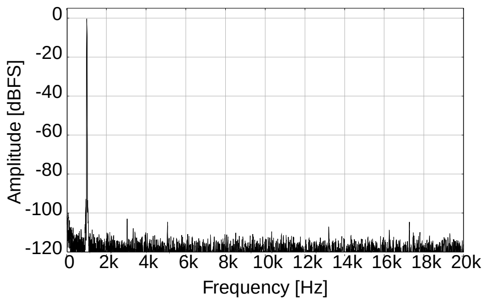
12 MHz master clock.
48 kHz sampling rate
Differential output at line-out, 1kΩ load.
Both channels active

Figure 28. DAC S/N versus input-level



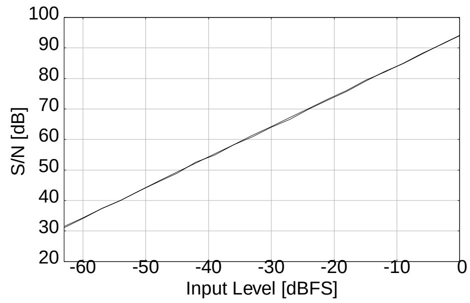
12 MHz master clock.
48 kHz Sampling Rate
Differential output at Line-Out, 1kΩ load.
A-Weighted, Both channels active

Figure 29. Analog path FFT



Differential input at Mic Preamplifier, 21 dB Gain.
Direct Mic to Line-Out connection (MICLO=1)
Differential output at Line-Out, 20kΩ load. Both channels active

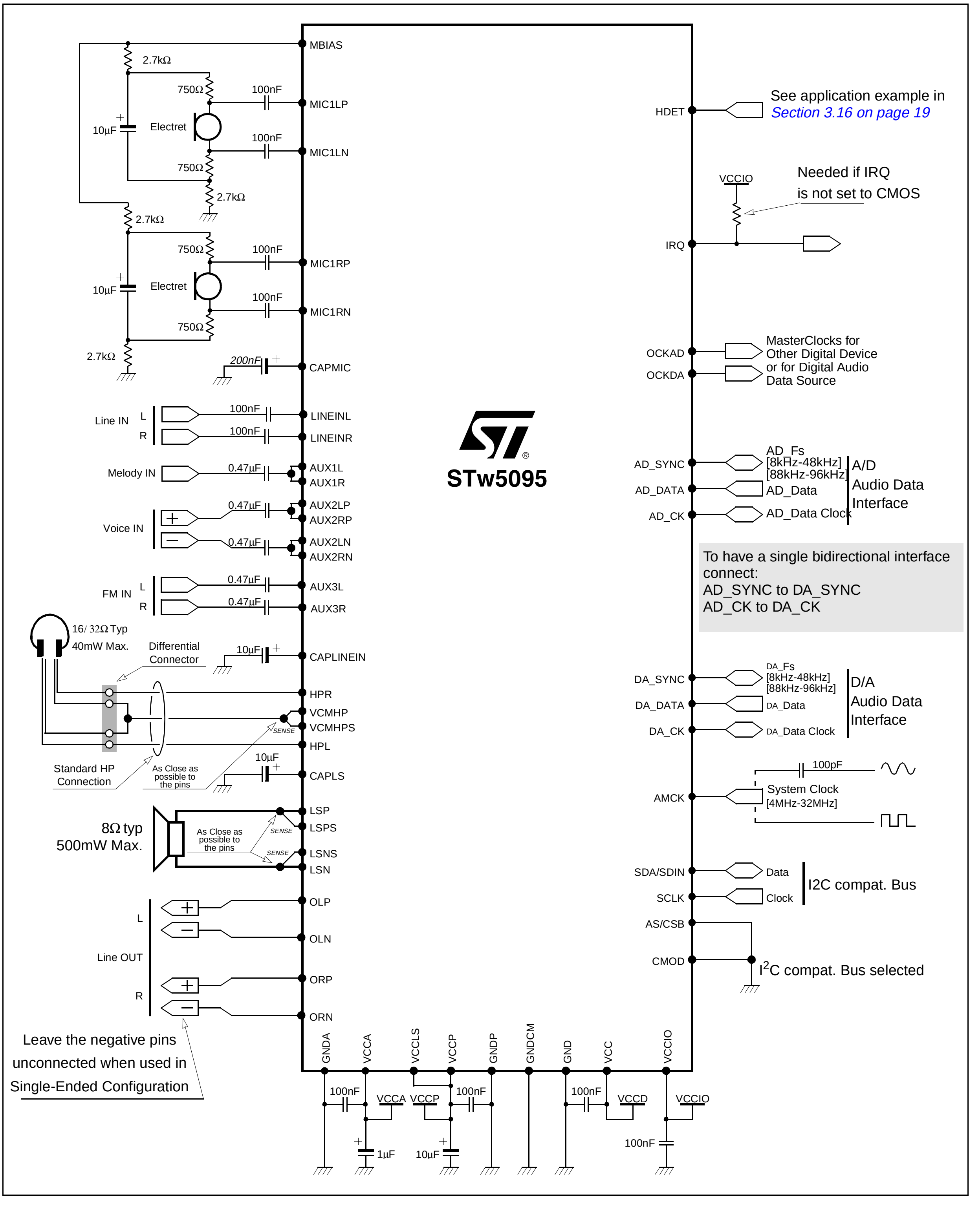
Figure 30. Analog path S/N versus input-level



Differential input at Line-In Amplifier, 0 dB Gain.
Line-In to DA-Mixer to Line-Out connection.
Differential output at Line-Out, 20kΩ load. A-weighted, both channels active

17 Application Schematics

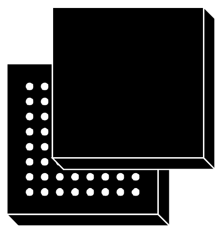
Figure 31. STw5095 application schematics



18 Package Outline

	Dimensions [mm]		
Ref.	**Min.**	**Typ.**	**Max.**
A (1)	1.010		1.200 (2)
A1	0.150		
A2		0.820	
b	0.250	0.300	0.350
D	4.850	5.000	5.150
D1		3.500	
E	4.850	5.000	5.150
E1		3.500	
e	0.450	0.500	0.550
f	0.600	0.750	0.900
ddd			0.080

OUTLINE AND MECHANICAL DATA

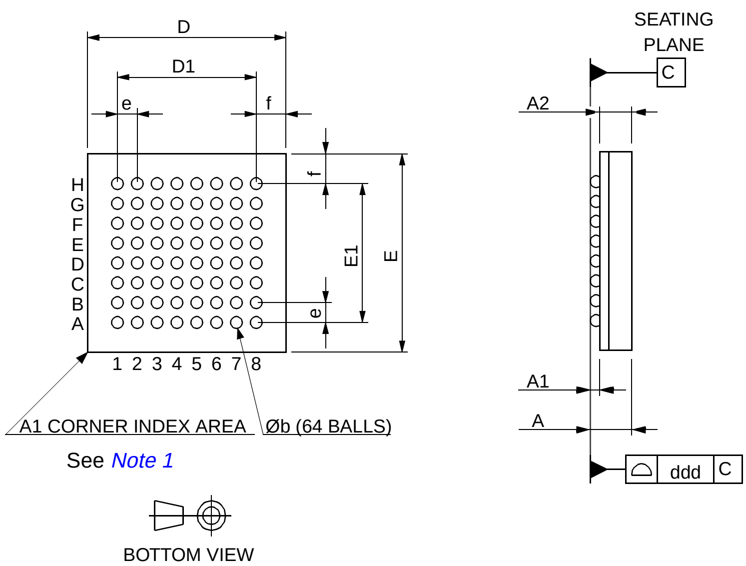


TFBGA 5x5x1.20 64 F8x8 0.50

Thin Profile **F**ine Pitch **B**all **G**rid **A**rray

1. The total profile height is measured from the seating plane to the top of the component.
2. Max mounted height is 1.12mm.Based on a 0.28mm ball pad diameter. Solder paste is 0.15mm thickness and 0.28mm diameter.

Figure 32. Package mechanical data



Note: 1 The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

19 Revision history

Date	Revision	Changes
8-Nov-2005	1.0	Initial release