Monochrome Analog Output CMOS Image Sensors

DESCRIPTION

The VV5430 is a highly-integrated VLSI camera device based on the unique CMOS sensor technology from STMicroelectronics. It delivers a fully-formatted composite monochrome video signal. Standards options include EIA (320 x 244) and CCIR (384 x 287).

It is possible to develop a single chip video camera using this device that requires only supply voltage in, and delivers composite video out for connection to a video monitor.

The integrated 75Ω driver eliminates the need for additional active components to drive standard loads, including double terminated lines.

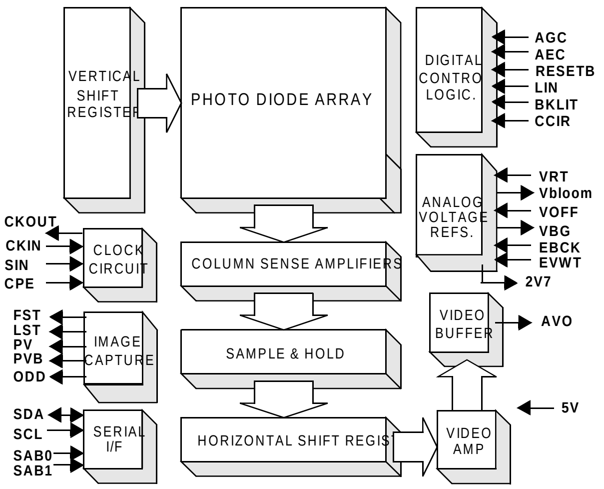
It is also suitable for applications requiring the digitisation of the video signal or external microprocessor control.

In the VV5430 Frame, Line and Pixel timing signals are provided to facilitate pixel-locked digitisation of the analog video data. In addition to the these outputs a synchronisation input (SIN) is also provided to allow the start of frame to be synchronised to an external event.

The device features automatic exposure control that allows a fixed-aperture lens to be used, and incorporates Normal and Backlit modes to give operation over a wide range of scene types.

A bi-directional serial interface on the VV5430 allows an external controller to set operational parameters and control exposure and gain values directly.

DEVICE FUNCTIONALITY



KEY FEATURES

- Complete Video Camera on a single chip
- Minimal support circuit
- EIA/CCIR standard compatible options
- Low power operation - single voltage supply
- Integral 75 ohm driver
- 384 x 287 pixel array
- Automatic exposure and gain control
- Linear or gamma corrected output option
- Automatic black level calibration
- Serial Interface Control
- Frame and line timing signals for external ADC

APPLICATIONS

- Security/Observation systems
- Biometric identification
- Toys and games
- Digital Image capture systems

SPECIFICATIONS

Pixel resolution	384 x 287 (CCIR) 320 x 243 (EIA)
Array size	4.66mm x 3.54mm
Min. illumination (min. detectable signal)	0.5 lux
Exposure control	Automatic (to 146000:1)
Gain control	Automatic (to +20dB)
Signal/Noise ratio	46dB
Supply voltage	5.0v DC +/– 5%
Supply current	<45mA
Operating temperature (ambient)	0^oC - 40^oC (for extended temp. info please contact STMicroelectronics)
Package type	48LCC

Table of Contents

1. Revision History

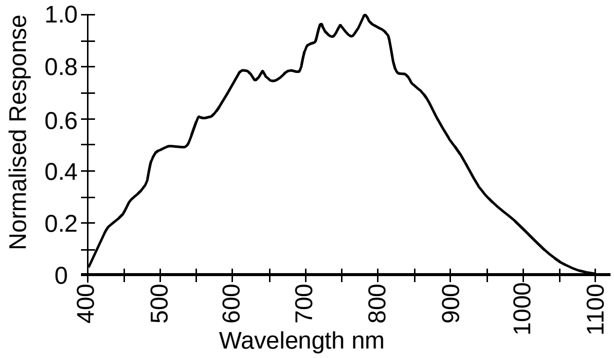
The following is a list of specific changes made to this datasheet since the previous revisions. It does not include general fomatting changes, but is intended to highlight changes that may affect device operation in a customer system.

Section	Change
2	Removed obsolete test descriptions Corrected Defect Specification
6	Added reference to generating SIN on only odd or only evenfields, not both.
10	Setup Code 1: Bit 10 was incorrectly described. This bit should be set to 0 for normal operation.

Table 1 : Revision History

2. Specifications

2.1 Device Specifications



Illumination Colour Temp.	3200^{o} K
Clock Frequency	Std. CCIR
Exposure	Maximum
Gain	x1
Auto. Gain Control (AGC)	Off
Correction mode	Linear

Figure 1 : Spectral Response

The sensor is tested using the example support circuit illustrated later in this document. Standard imaging conditions used for optical tests employ a tungsten halogen lamp to uniformly illuminate the sensor (to better than 0.5%), or to illuminate specific areas. A neutral density filter is used to control the level of illumination where required.

Parameter	Value
Supply Voltage	-0.5 to +7.0 volts
Voltage on other input pins	-0.5 to V_{DD} + 0.5 volts
Ambient Operating Temperature (contact STMicroelectronics for extended temp. ranges)	0^{o}C to 40^{o}C
Storage Temperature	-30^{o}C to 125^{o}C
Maximum DC TTL output Current Magnitude	10mA (per o/p, one at a time, 1sec. duration)

Table 2 : Absolute Maximum Ratings

Note: Stresses exceeding the Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Operating supply voltage	4.75	5.0	5.25	Volts	
V_{IH}	Input Voltage Logic “1”	2.4		V_{DD}+0.5	Volts	
V_{IL}	Input Voltage Logic “0”	-0.5		0.8	Volts	
T_A	Ambient Operating Temperature	0		40	^{o}C	Still air

Table 3 : DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CKIN	EIA Crystal frequency		12.0000		MHz	1
CKIN	CCIR Crystal frequency		14.7456		MHz	1
SCL	Serial Data Clock			100	KHz	2

Table 4 : AC Operating Conditions

1. Pixel Clock = $^{CKIN}/_{2}$
2. Serial Interface clock must be generated by host processor.

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
I_{DCC}	Digital supply current		10		mA	1
I_{ADD}	Analog supply current		25		mA	1
I_{DD}	Overall supply current		35		mA	1
V_{REF2V7}	Internal voltage reference		2.700		Volts	
V_{BG}	Internal bandgap reference		1.22		Volts	
V_{OH}	Output Voltage Logic "1"	2.4			Volts	I_{OH} = 2mA
V_{OL}	Output Voltage Logic "0"			0.6	Volts	I_{OL} = -2mA
I_{ILK}	Input Leakage current	-1			µA	V_{IH} on input
				1	µA	V_{IL} on input

Table 5 : Electrical Characteristics

Typical conditions, V_{DD} = 5.0 V, T_A = 27^{o}C

1. Digital and Analogue outputs unloaded - add output current.

Parameter	min.	typ.	max.	units	Note
Dark Current Signal		50		mV/Sec	Modal pixel voltage due to photodiode leakage under zero illumination with Gain=1 (V_{dark} = (V_{t1} - V_{t2})/(t1-t2), calculated over two different frames
Sensitivity		6		V/Lux·Sec	V_{Ave}/Lux·10ms, where Lux gives 50% saturation with Gain=1 and Exposure=10ms
Min. Illumination		0.5		Lux	Minimum detectable illumination with Standard CCIR clock

Note: Devices are normaly not 100% tested for the above characterisation parameters, other than Dark Current Signal.

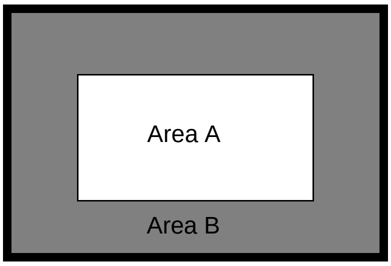
Table 6 : Operating characteristics

2.2 Defect Specification

A Defect is an area of pixels that produces output significantly different from its surrounding pixels for the same illumination level. The definition of a Defect Pixel varies according to testing conditions as follows:

Test	Exposure	Illumination	Defective Pixel output definition
Black Image Test	Minimum	Black	Differing more than ±8%. from modal value.
Light Image Test	Mid range	66% Sat.	Differing more than ±4% from modal value.

The pixel area of the sensor is divided into the following areas to qualify the defect specification:



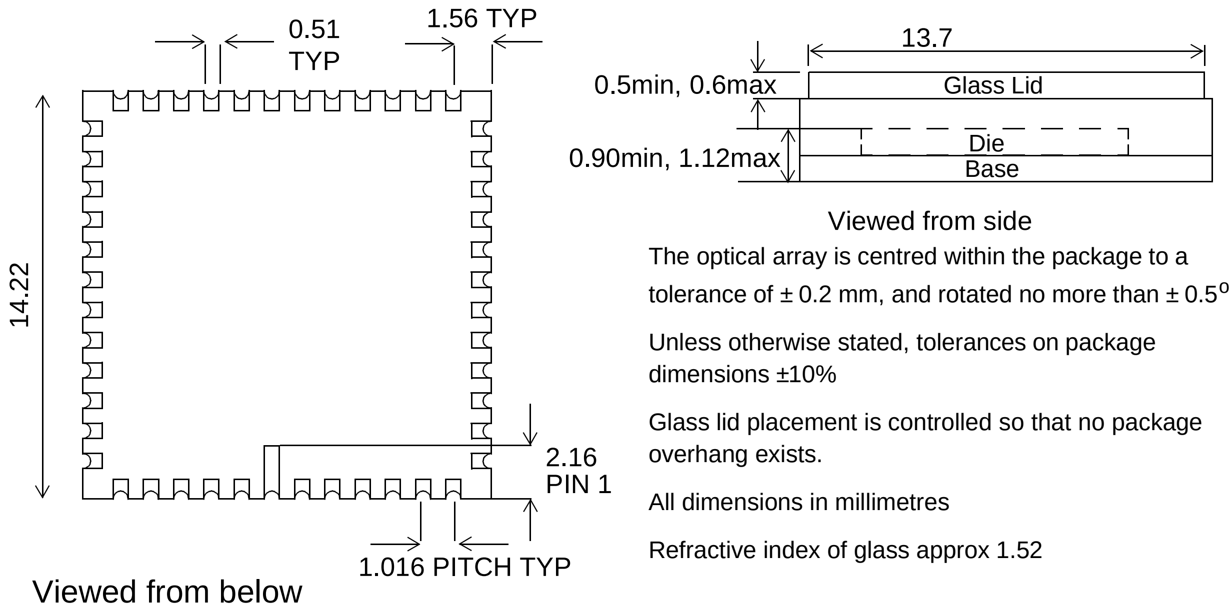
Where Area A is the inner 50% of the image area

The defect specification is then defined as follows:

Image Area	Max. No. of Defectes	Notes
Area A	0	This is the most critical image area
Area B	4	Unconnected single pixels
	1	Of up to four connected pixels (2x2 max.)

3. Device Details

3.1 Package Details



The optical array is centred within the package to a tolerance of ± 0.2 mm, and rotated no more than ± 0.5°

Unless otherwise stated, tolerances on package dimensions ±10%

Glass lid placement is controlled so that no package overhang exists.

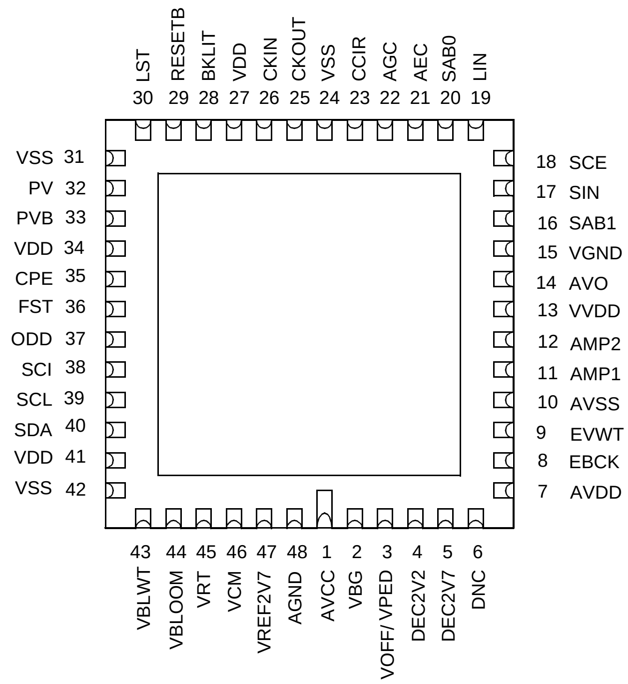
All dimensions in millimetres

Refractive index of glass approx 1.52

3.2 Pinout Diagram

48 Pin LCC

Viewed from top of package



3.3 Pin List

Pin	Signal Name	Typ e	Description
POWER SUPPLIES			
1	AVCC	PWR	Core analogue power and reference supplies.
7	AVDD	PWR	Output stage power. AVDD3 output stage logic.
10	AVSS	GND	Output stage ground. AVSS3 output stage logic.
13	VVDD	PWR	75ohm buffer supply.
15	VGND	GND	75ohm buffer ground.
24,31	VSS	GND	Digital padring & logic ground.
27,34	VDD	PWR	Digital padring & logic power.
41	DVDD	PWR	Core digital power.
42	DVSS	GND	Core digital ground.
48	AGND	GND	Core analogue ground and reference supplies.
ANALOGUE VOLTAGE REFERENCES			
2	VBG	OA	Internal bandgap reference voltage (1.22V nominal). Requires external 0.1uF capacitor.
3	VOFF/VPED	IA	Pedestal DAC & offset comp. DAC bias. Connect to VBG or external reference.
4	DEC2V2	OA	Decouple 2.2V reference. Requires external 0.1uF capacitor.
5	DEC2V7	OA	Decouple 2.7V reference. Requires external 0.1uF capacitor.
6	-	DNC	Do NOT connect - for test use only
8	EBCK	IA	External black level bias. Internally generated. Decouple to VGND
9	EVWT	IA	External white pixel threshold for exposure control. Decouple to VGND
43	VBLWT	IA	Defines white level for clamp circuitry. Requires external 0.1uF capacitor.
44	VBLOOM	OA	Anti-blooming voltage reference. Requires external 0.1uF capacitor.
45	VRT	IA	Pixel reset voltage. Connect to VREF2V7 or external reference.
46	VCM	IA	Offset DAC common mode input. Connect to VREF2V7.
47	VREF2V7	OA	Internally generated 2.7V reference. Requires external 4.7uF capacitor.
ANALOGUE OUTPUTS			
14	AVO	OA	Buffered Analogue video out. Can drive a doubly terminated 75ohm load.
SYSTEM CLOCKS			
25	CKOUT	OD	Oscillator output. Connect Crystal for standard timing.
26	CKIN	ID	Oscillator input. Connect Crystal for standard timing.
IMAGE CAPTURE TIMING SIGNALS			

Pin	Signal Name	Type	Description
30	LST	OD	Line start. Active high pulse (start of active video lines).
32	PV	OD	Pixel sample clock. Qualifies video output for external image capture.
33	PVB	OD	Pixel sample clock bar. Inverse of PV.
35	CPE	ID↓	Pixel sample clock enable. Default CPE = 0 i.e. PV/PVB disabled.
36	FST	OD	Field start. Synchronises external image capture.
37	ODD	OD	Odd/even field signal. (ODD = 1 for odd fields, ODD = 0 for even)
DIGITAL CONTROL SIGNALS			
16	SAB1	ID↓	Higher bit of two least significant bits of device address on serial interface.
17	SIN	ID↓	Used to reset video timing control logic without resetting any other part of VV5430. Resets video logic on the falling edge of the SIN pulse.
18	SCE	ID↓	Scan mode enable - only relevant to test mode.
19	LIN	ID↓	Gamma corrected or Linear output. LIN = 0, gamma corrected output, LIN = 1, linear output. Default is gamma. LIN = 0 can be overridden via serial interface.
20	SAB0	ID↓	Lower bit of two least significant bits of device address on serial interface.
21	AEC	ID↑	Automatic exposure control. AEC = 1, auto exposure is enabled; AEC = 0 auto exposure **and** auto gain control are disabled. AEC = 1 can be overridden via serial interface.
22	AGC	ID↑	Automatic gain control enable. AGC = 1, auto-gain is enabled (if AEC = 1); AGC = 0, auto-gain is disabled. AGC can be overridden via serial interface.
23	CCIR	ID↑	Select default video mode for power-on. CCIR = 1 for CCIR video. EIA video mode is selected when CCIR = 0. Default is CCIR if unconnected
28	BKLIT	ID↓	Normal or Backlit exposure control mode. BKLIT = 0, normal mode. BKLIT = 1, backlit mode. Default is normal. BKLIT state can be overridden via serial interface. See Exposure Control for details.
29	RESETB	ID↑	Active low camera reset. All camera systems are reset to power-on state.
38	SCI	ID↓	Scan chain input - only relevant to test mode.
39	SCL	ID↑	Serial bus clock (input only). Must be generated by comms. host.
40	SDA	BI↑	Serial bus data (bidirectional, open drain).

Key:

OA- Analogue output
OD- Digital output
OD↓-Digital output with internal pull-down
BI - Bidirectional

IA - Analogue input
ID - Digital input
ID↑ - Digital input with internal pull-up

4. Video Standards

The VV5430 has 2 different video format modes, producing CCIR or EIA standard composite Monochrome video output. Line standards and frequencies are as follows:

Video Mode	Format	Image (Pixels)	Crystal Frequency	CCIR pin
CCIR	4:3	384 x 287	14.7456 MHz	1
EIA	4:3	320 x 243	12.0000 MHz	0

Table 7 : VV5430 Video Modes

4.1 Video Signal Characteristics

The following table summarises the composite video output levels (AVO) for the two standards, which are graphically illustrated on the following pages:

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{Sync}	CCIR, EIA Sync. level		0.3		V	
V_{blank}	CCIR, EIA Blanking level		0.9		V	DC reference level
V_{black}	CCIR Black level		0.9		V	
	EIA Black level		1.0		V	
V_{Sat}	CCIR Saturation level		2.3		V	Peak White; AVO clipped at this level
	EIA Saturation level		2.4		V	

Table 8 : Video Timing Parameters

Note: All measurements are made with AVO driving one 75Ω load.

CCIR Timing Diagram

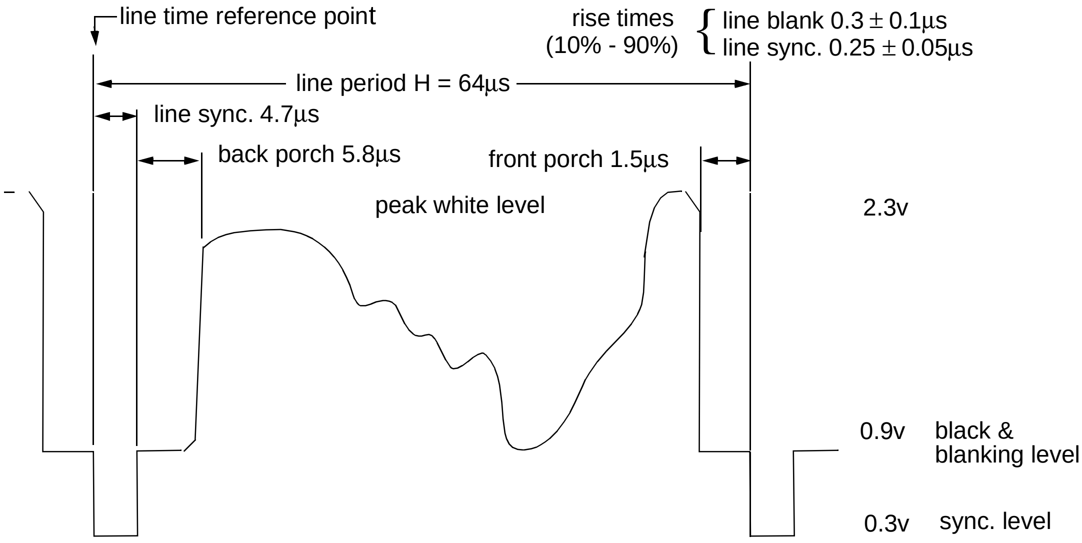


Figure 2 : CCIR composite video line-level timing

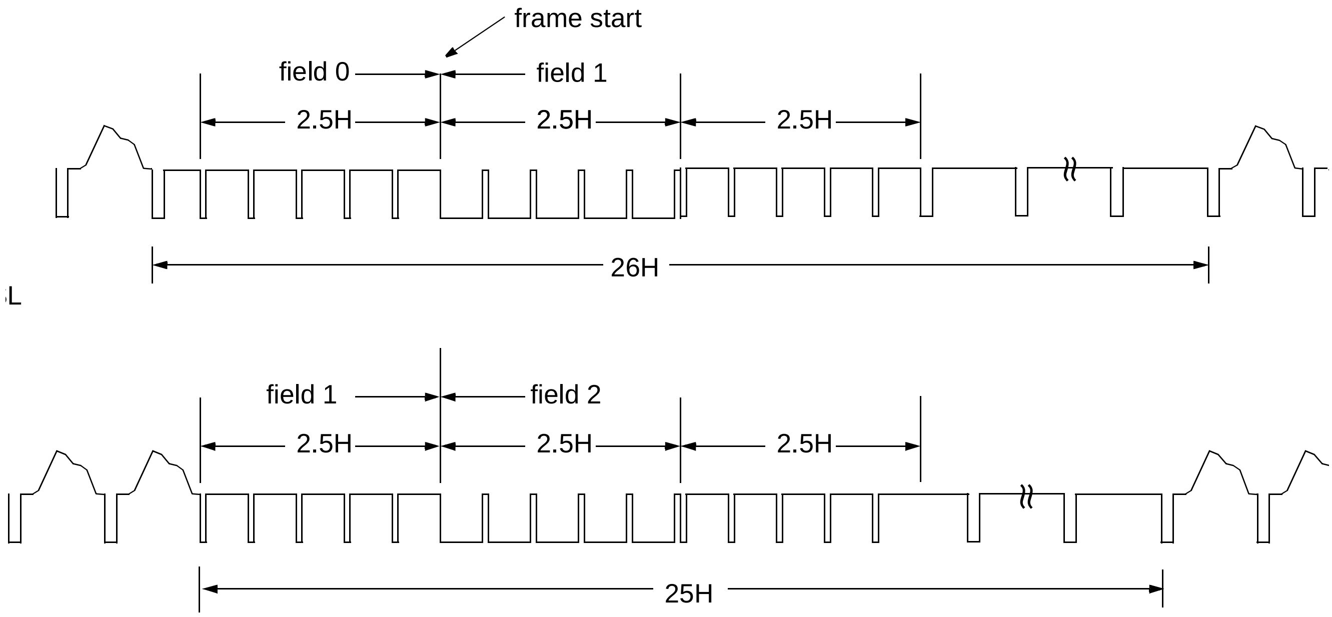


Figure 3 : CCIR composite video signal - field level timing

EIA Timing Diagrams

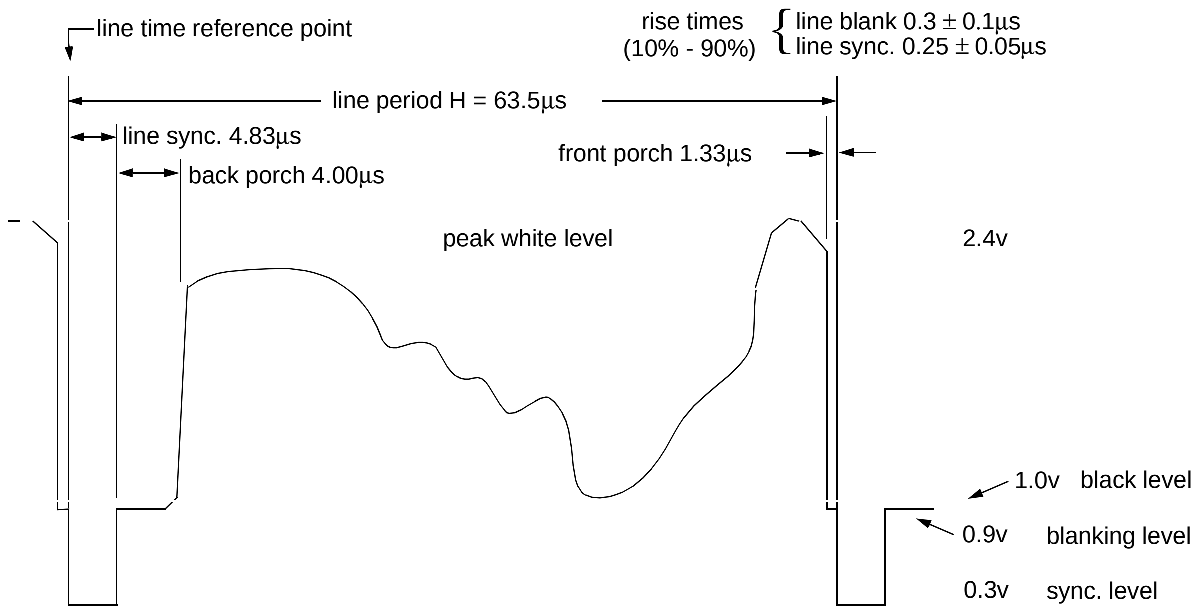


Figure 4 : EIA composite video signal - line level timing

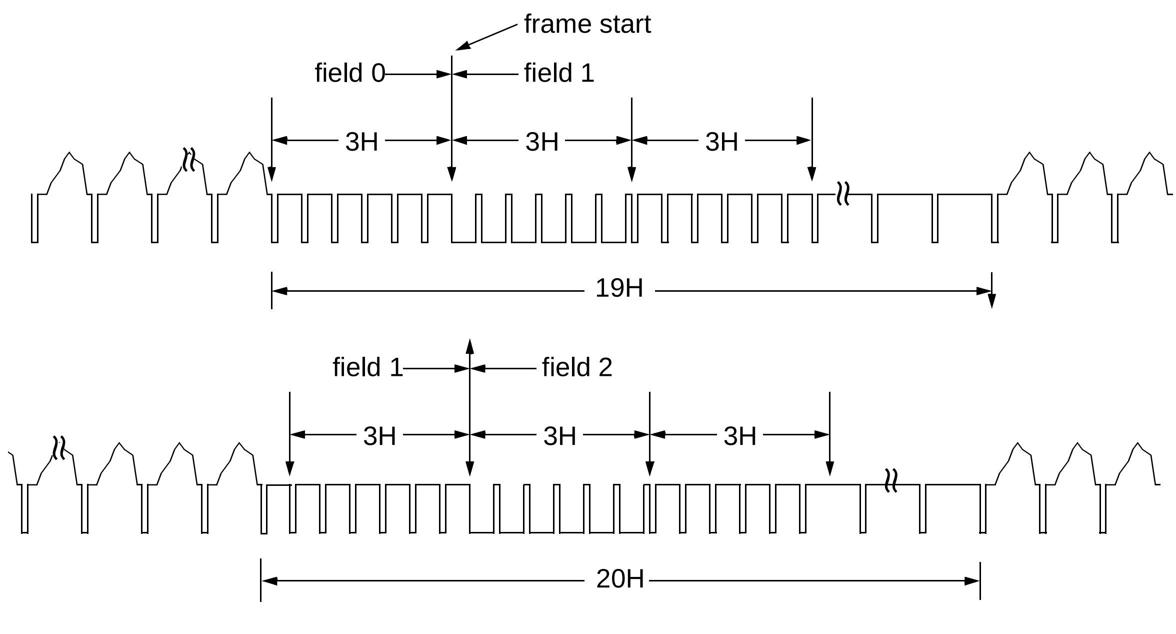


Figure 5 : EIA composite video signal - field level timing

5. Control Signals for Image Digitisation

The VV5430 sensor can be used with an Analog-to-Digital Converter (ADC) and the necessary logic to form an image capture and processing system. The camera provides an analogue video output together with digital signals to qualify this output and synchronise image capture.

The signals provided for image capture are the following:-

- PV,PVB: (Pixel Valid, PV Bar) Complementary signals, their leading edges qualify valid pixel levels.
- LST: (Line STart) The rising edge signals the start of a visible line.
- FST: (Field STart) The rising edge signals the start of a field.
- ODD: Identifies an odd field within a frame.
- CPE (Clock Pulse Enable): Disables generation of PV/PVB and LST signals. The state of this pin is sampled only during a system reset. Its state after reset can be overridden via the serial interface using Set-up Code_2.

The following diagram illustrates the relative timing of the image capture signals. Scale is not actual but edge succession is preserved.

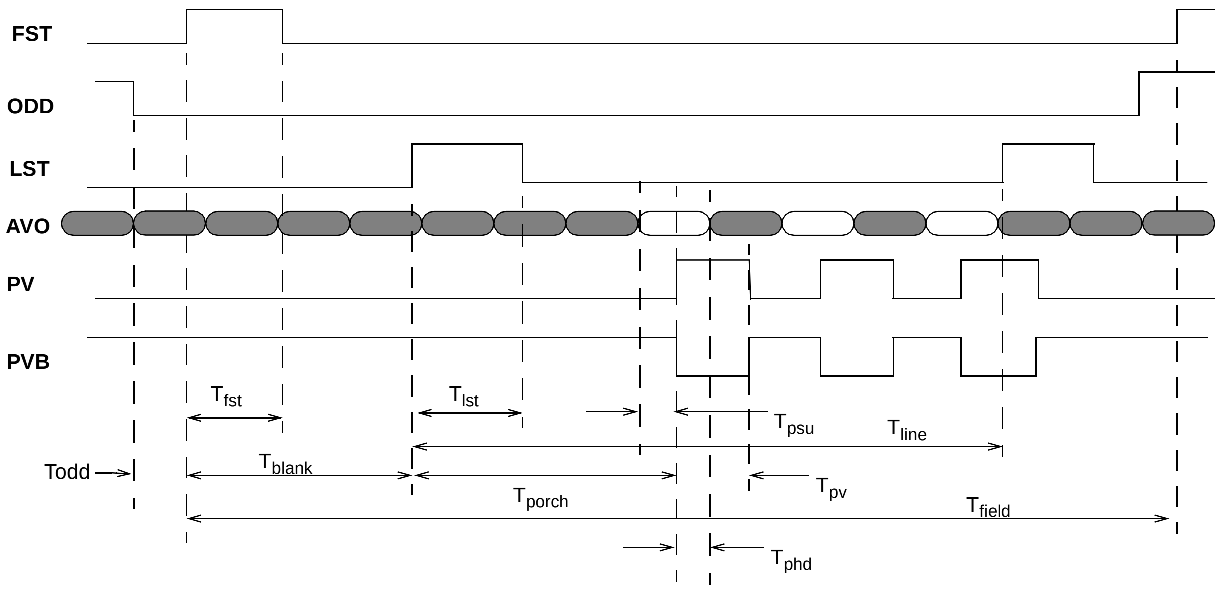


Figure 6 : Frame Capture signal timing

5.1 Image Capture Control Signal Timing

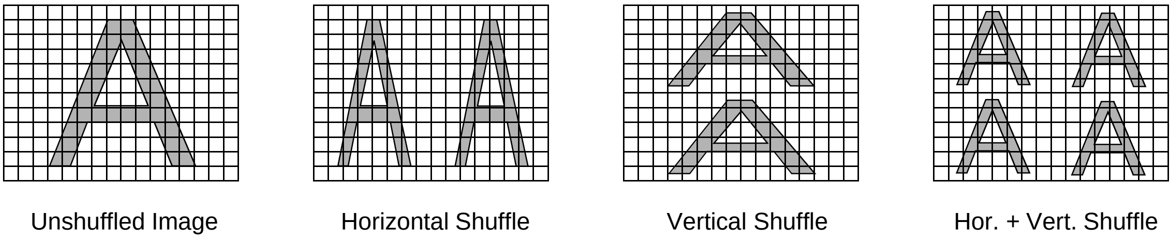
The time intervals given are correct for the recommended crystals:

Name	CCIR	EIA
Crystal Frequency (F_{CKIN})	14.7456 MHz	12.0000 MHz
Pixel clock period ($T_{pck} = 2/F_{CKIN}$)	135.63 nsec	166.67nsec
PV (Pixel clock) mark:space	1:1	1:1
PV high period ($T_{pv} = T_{pck}/2$)	67.82 nsec	83.34 nsec
Even (first) field period (T_{field})	20.032 msec (313 x T_{line})	16.7005 msec (263 x T_{line})
Odd (second) field period (T_{field})	19.968 msec (312 x T_{line})	16.637 msec (262 x T_{line})
FST duration (T_{FST})	7.73 µsec (57 x T_{pck})	6.1 µsec (45 x T_{pck})
Line period (T_{line})	64.0 usec (472 x T_{pck})	63.5 µsec (381 x T_{pck})
LST duration (T_{LST})	4.61 µsec (34 x T_{pck})	4.66 µsec (28 x T_{pck})
First visible line delay (T_{blank})	704.949 µsec (11xT_{line} + 7xTpck)	762.833µsec (12xT_{line} + T_{pck})
First visible pixel delay (T_{porch})	10.58 µsec (78 x T_{pck})	8.833 µsec (53 x T_{pck})
Visible line period	52.083 µsec (384 x T_{pck})	53.333 µsec (320 x T_{pck})
Max AVO to PV setup time (T_{psu})	33.9 nsec	41.7nsec
Min. PV to AVO hold time (T_{phd})	30nsec	40nsec
ODD to FST rise (TODD)	21.700 msec (160 x Tpck)	11.500 msec (69 x Tpck)

Table 9 : Signal Timing

6. Shuffle Modes

The pixels in the VV5430 sensor array can be output to AVO as alternate columns and rows by setting bits 5 and 6 in the Setup Code_1 register (header code 0001 - see Serial Interface for details). This has the effect of generating two, or four, identical low resolution images in one field:



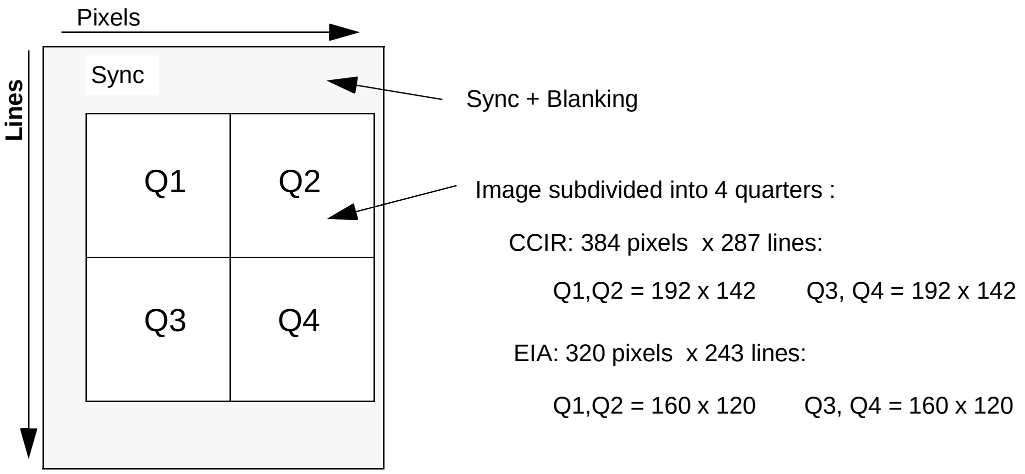
When this facility is combined with AVO Enable selected for the appropriate quarter, it is possible to display the images from four separate cameras on one monitor.

In order to achieve four identical images in one frame (from one sensor), bits 5 and 6 of Setup Code_1 must both be set via the serial interface, that is HSHUFFLE=1 and VSHUFFLE=1. The former interleaves odd and even pixel lines in the image, and the latter interleaves pixel columns. OE[0..2] can then Enable AVO output for any one quarter of the display field.

6.1 Quarter mode output

The VV5430 video output can be Enabled in different parts of the standard field by programming bits 9..11 of Setup Code_2, that is CE[0..2]; when not enabled, the AVO output is Tristated, that is floating at high impedance. Thus, a number of different sensor AVO outputs can be connected together and selectively enabled. This feature, together with bus addressing of up to four VV5430s on one serial link, is intended for multi-sensor systems that, in conjunction with bits 5,6 of Setup Code_1, enable the images from up to four cameras to be displayed on a single monitor.

By programming CE[0..2] different areas of the field can be enabled:.



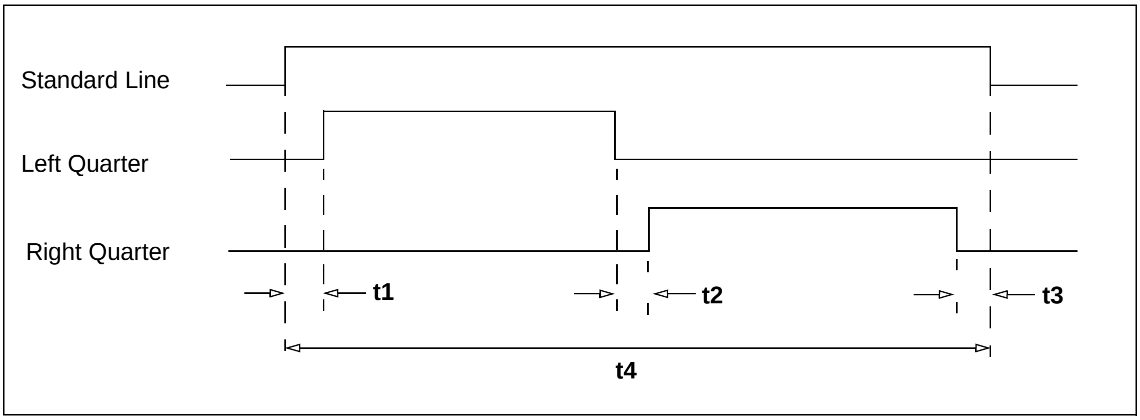
The effect of OE[0..2] on AVO output is summarised in the following table:

OE[2]	OE[1]	OE[0]	Regions where AVO is enabled
0	0	0	All (Normal operation)
0	0	1	None (AVO permanently tristate)
0	1	0	Sync only
0	1	1	Sync plus Q1 image
1	0	0	Q1
1	0	1	Q2
1	1	0	Q3
1	1	1	Q4

Table 10 : AVO Enable selection

Since each of the horizontal ‘halves’ of the frame is only 142 lines (CCIR) or 120 lines (EIA), there is a ‘black band’ of three lines separating the top half from the bottom half. Similarly, for timing purposes, there is a two pixel vertical black band separating the left and right halves of the frame. (See the timing diagram below.)

6.2 Quarter mode line timing.



Pixel timings for AVO 1/4 Mode:

Description	#t	CCIR		EIA	
		pck cycles	Time (us)	pck cycles	Time (us)
Left quarter Line Delay	t1	1	0.1356	1	0.1667
Duration of left quarter line		190	25.4928	158	26.0052

Table 11 : Pixel Timings for 1/4 mode

Description	#t	CCIR		EIA	
		pck cycles	Time (us)	pck cycles	Time (us)
Inter-quarter Interval	t2	2	0.2713	2	0.3333
Duration of right quarter line		190	25.4928	158	26.0052
Right quarter border	t3	1	0.1356	1	0.1667
Duration of standard SI	t4	384	52.0704	320	53.3440

Table 11 : Pixel Timings for 1/4 mode

In addition there are line level signals to identify the top and bottom half of the active video area of the field: .

Description	Start line		Number of lines	
	CCIR	EIA	CCIR	EIA
Top half of field	First active line	First active line	142	120
Bottom half of field	Active line 145	Active line 124	142	120

Table 12 : Line Timings for 1/4 mode

There is a 'black band' of three video lines between the valid lines in the top half of the field and the valid lines in the bottom half of the field. This ensures that both halves of the field are the same size and provides a horizontal frame line. The line level timing described above also provides a two pixel vertical black line, hence the four quarters appear to be 'framed' in the display.

7. Exposure Control

Automatic exposure and gain control ensure operation of the VV5430 over a wide range of lighting conditions. Automatic black level control and optional 'Backlit' mode further ensure consistent picture quality. The devices control exposure over a range of 99,000:1 in EIA mode and 146,000:1 in CCIR mode, and operates at illumination levels as low as 0.5 lux.

Note: The System Clock can be divided by up to eight times to further increase sensitivity by extending the exposure time. This, of course, also reduces the frame rate to non-standard values.

Automatic exposure and gain control are enabled with AEC=1 (pin 21) and AGC=1 (pin22), but can be inhibited via the serial interface (Setup Code_1). However, If AEC is inhibited by pin 21, AGC is also inhibited and the serial interface has no control. Inhibiting AEC or AGC via the serial interface, or by taking pin 21 or 22 low, freezes the current value(s) for these, which can then be altered by writing to the exposure and gain control registers. (See Serial Interface for details.)

Note: The timing of exposure and gain control messages on the serial interface is very important. External values for exposure and gain are only applied at the start of a frame, and the serial interface must be paused until the new values are installed—no further communications will be accepted during this time.

7.1 Automatic Exposure Control (AEC)

Automatic exposure control is achieved by varying pixel current integration time according to the average light level on the sensor. This integration time can vary from one pixel clock period to one frame period.

Pixels above a threshold white level are counted every frame, and the number at the end of the frame defines the image as overexposed, above average, correctly exposed, below average or underexposed. If the image is other than correctly exposed, a new value for integration time is calculated and applied for the next frame. Corrections are either ±1/8 or ±1/64, depending upon the degree of over or under exposure. If the exposure value is close to its limit (12% below max. or 25% above min.), then gain is increased or decreased by one step and exposure is set to midway in its range. Exposure is then controlled as normal.

7.2 Automatic Gain Control (AGC)

The VV5430 automatically increases the system gain of its output stage if with the current gain setting and maximum exposure the image is too dark. Gain can be varied from x1 to x16 in times-two steps, giving five different gain settings.

If the scene is too dark and the integration period has almost reached its maximum value, the gain value is incremented by one step (times two). In the same frame period the exposure value is divided by two, halving the integration period. The exposure controller then increases the exposure value as necessary. Similarly if the image is too bright and the integration period is short then gain will be reduced by one step (divide by two) and the exposure value will be doubled. The exposure controller can then adjust the exposure value as necessary to provide a correctly exposed image.

Increasing gain is limited to a programmable upper limit, for which the default value is x8. The gain upper limit is programmed by setting bits [0..3] with header code 0101, when AGC=1. If Automatic Gain Control is inhibited (AGC=0), these registers are used instead to select a gain setting up to x16.

7.3 Backlit Mode

The VV5430 can be configured to operate in two auto-exposure modes, selected by the BKLIT pin (pin28) state, or via the serial interface (Setup Code_1, bit 0). The default mode (BKLIT = 0) provides exposure control for normally illuminated scenes. For scenes where a bright background can cause the foreground subject to be severely under exposed, the 'Backlit' mode (BKLIT = 1) offers superior performance.

'Backlit Mode' (BKLIT=1) operates by using a higher threshold level for the exposure control comparator over the central area of an image, which is therefore exposed for longer and so enhanced. The area in which the higher comparator threshold is used when BKLIT=1 is illustrated below:

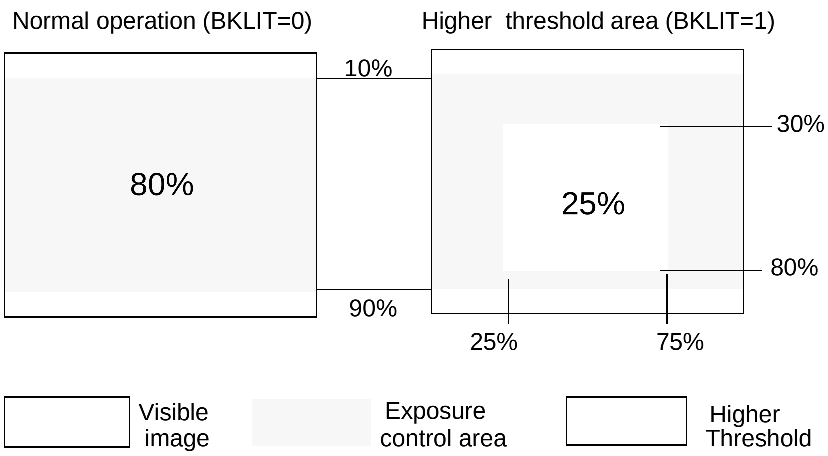


Figure 7 : Backlit exposure region

Note: The threshold level used for the central area is a preset mutiple of the normal mode reference level, and is not alterable. In some circumstances this may not be sufficient difference to cause a noticable effect on the overall exposure of the image.

8. Serial Communication

The VV5430 includes a full duplex (two-wire) serial interface, and can be controlled and configured by a host processor. The base bus address for the VV5430 is 20_H, but the two least significant bits of the address (SAB0, SAB1) can be selected by hard-wiring pins 20 and 16. This allows up to four separate camera devices to be controlled on one serial link, which, for example, makes multiplexing of camera outputs possible.

The serial interface reads or writes data to a set of Registers that define the characterisation of the sensor, and control certain operations.

8.1 Serial Communication Protocol

The host must perform the role of a communications master and the camera acts as either a slave receiver or transmitters communication between host and camera takes the form of three or five byte messages of 8-bit data, with a maximum serial clock (SCL) frequency of 100kHz. Since the serial clock is generated by the host, the host determines the data transfer rate.

The host processor initiates a message by forcing both Serial Data (SDA) and Serial Clock (SCL) low. The first byte addresses the required device, and defines either a READ message (four bytes to follow) or a WRITE message (two bytes to follow). After the camera has acknowledged a valid address (ACK, bit 9 of SCL), the host then either reads four bytes of data from the camera or transmits a further two bytes to the camera. The data transfer protocol on the bus is illustrated below:

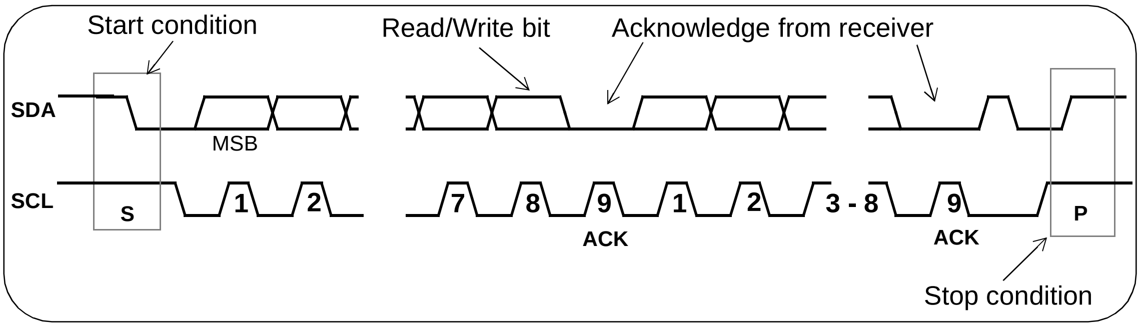
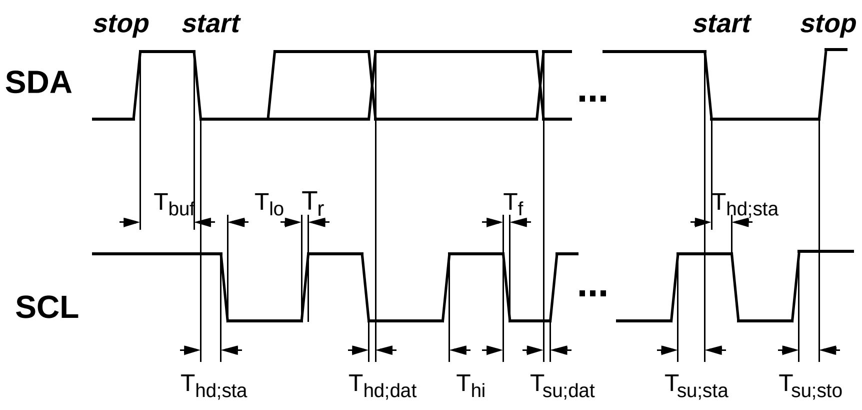


Figure 8 : Data Transfer Protocol



Note: All values referred to the minimum input level (high) = 3.5V, and maximum input level (low) = 1.5V

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	F_{scl}	0	100	kHz
Bus free time between a stop and a start	T_{buf}	4.7	-	µs
Hold time for a repeated start	$T_{hd;sta}$	4.0	-	µs
LOW period of SCL	T_{lo}	4.7	-	µs
HIGH period of SCL	T_{hi}	4.0	-	µs
Set-up time for a repeated start	$T_{su;sta}$	4.7	-	µs
Data hold time	$T_{hd;dat}$	0[1]	-	µs
Data Set-up time	$T_{su;dat}$	250	-	ns
Rise time of SCL, SDA	T_r	-	1000	ns
Fall time of SCL, SDA	T_f	-	300	ns
Set-up time for a stop	$T_{su;sto}$	4.0	-	µs
Capacitive load of each bus line (SCL, SDA)	C_b	-	100	pF

1. The VV5430 internally provides a hold time of at least 300ns for the SDA signal (referred to the minimum input level (high) of the SCL signal) to bridge the undefined region of the falling edge of SCL

Table 13 : Serial Interface Timing Characteristics

9. Read data from camera

Information describing the current configuration and the current exposure values can be read from the camera. The data is formed into four bytes of 8 bits. Each pair of bytes is considered to be a data word and is read out msb first.

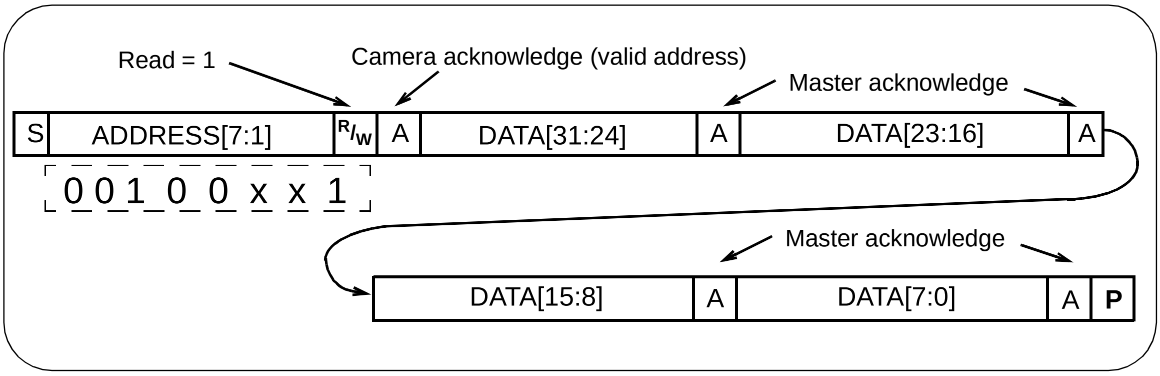


Figure 9 : Read Data Format

The following tables defines the information contained in the read messages. By default, the Primary Read Data is accessed; only if a Secondary Read Select bit is set in Setup Code_2 (header code 0010) is the Secondary information read.

Primary Read Data:

Bit	Function
31 - 23	Coarse Exposure Value (9 bits)
22 - 14	Fine Exposure Value (9 bits)
13 - 10	Gain Value (4 bits)
9	Auto Exposure Control on/off
8	Internal Black Calibration on/off
7	Auto Gain Control on/off
6	Gamma or Linear Video Output
5	Normal or Backlit mode[1]
4	Undefined
3 - 0	Camera Type ID Code (4 bits)

Secondary Read Data:

Bit	Function
31 - 18	Undefined
17	Black Level monitor in progress
16 - 0	White Pixel count (17 bits)

1. Bit 5 of the Primary Read message only reflects the state of the BKLIT pin, not the combined result of the pin and the serial interface BKLIT control bit.

10. Write to Camera

Information to be communicated from host to camera consists of configuration data (for example automatic gain control ON), and parametric information (for example sensor integration time). The write data is formed into two bytes. A 4-bit Header Code in the first byte is used by the camera to determine the destination of the 12-bit message following the header.

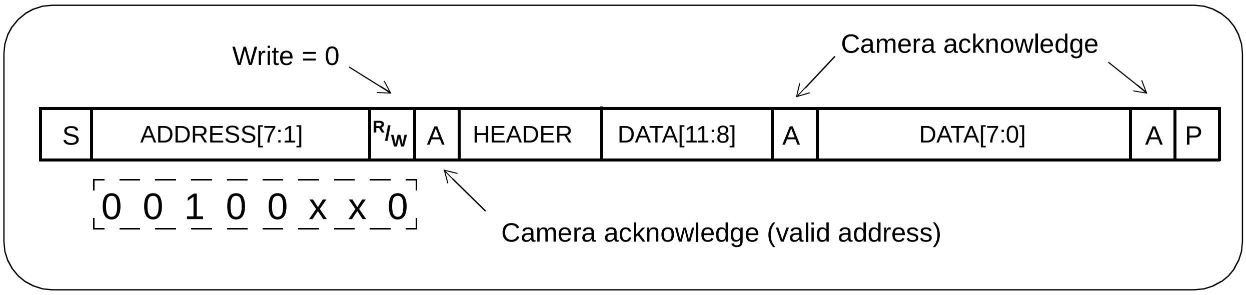


Figure 10 : Receive Data Format

After the camera acknowledges the receipt of a valid address the host transfers the first data byte which the camera acknowledges by pulling SDA low. The second byte is then sent followed by a final acknowledge from the camera. A stop condition is produced by the host after the second message byte. As with the read procedure, the stop condition is not absolutely necessary as the camera's serial interface will reset automatically after two bytes have been received.

The valid Header Codes and their data structures are fully described in the following pages.

10.1 Timing Protocol

When an exposure or gain value has been written to the camera it is held in the interface until the camera is ready to consume the new data. For correct operation, there should be no further read or write accesses to the camera during this hold period. Normal communication between other modules connected to the serial interface will not cause problems. The minimum length of the wait period is **40ms** in EIA mode and **34ms** in CCIR mode from the end of the data transfer.

10.2 Header Codes

The message can be a configuration word, an exposure, gain or calibration value. The camera's interpretation of the header code and the set-up code message are given in the table below. Defaults for each control bit are built in to the camera's reset cycle, and may be changed on-the-fly under host control.

Code	Interpretation	Comment
0000	Invalid	
0001	Set-up code_1 (9 bits)	Basic funtionality options
0010	Set-up code_2 (9 bits)	Pixel control & Read Data
0011	Coarse exposure value (9 bits)	Set AEC=0 to enable
0100	Fine exposure value (9 bits)	Set AEC=0 to enable
0101	Gain control value (4 bits)	Set AGC=0 to enable
0110	Unused	
0111	Unused	
1000	Exposure control T1 threshold (9 bit)	
1001	Exposure control T2 threshold (9 bit)	
1010	Analogue control register (8 bit)	
1011	Reserved	Not applicable to normal use
1100	Reserved	Not applicable to normal use
1101	Reserved	Not applicable to normal use
1110	Set-up code_3 (6 bits)	Pixel synchronisation
1111	Test mode select	Not applicable to normal use

Table 14 : Header Codes

10.3 Message content

The following Tables contain details of the data associated with each header code, and the number of valid data bits in each of the registers. In all cases the full 12 bit message tail can be sent, the valid bits being packed to the lsb. (Normally, the unused bits would be assigned zeroes.)

Setup Code_1

Header Code = 0001

Valid data bits: 11

The code_1 setup register is used to select different basic operating modes:

Bit	Function	Default	Comment
0	Normal/Backlit	0	Selects between normal and backlit exposure modes. The power-on default is normal mode. See Exposure Control for full description
1	Linear Correction enable	0	Selects between a linear (LIN=1) or gamma corrected video signal on AVO. The power-on default is gamma corrected.
2	Auto gain control enable	1	Allows automatic gain control to be inhibited. The current gain value selected is frozen. With AGC=0 a new gain value can be written to the gain register via the serial interface (header code 0101).
3	Inhibit black calibration	0	Allows automatic black calibration to be inhibited.
4	Auto exposure control enable	1	Allows automatic exposure control to be inhibited. The current exposure value selected is frozen. Note that if automatic exposure control is inhibited then automatic gain control is also disabled. With AEC=0 a new exposure value can be selected by writing to the coarse and fine exposure registers via the serial interface (header codes 0011 & 0100).
5	Horizontal shuffle enable	0	Shuffles the read out of the horizontal shift register. Even columns read out together then odd columns.
6	Vertical shuffle enable	0	Shuffles the readout of the vertical shift register. Even lines read out together then odd lines.
7	Force black calibration	1	Requests a re-calibration of the black level while bit is low.
8	Clock divisor DIV0	0	System clock division: (see Note) 0,0=1; 0,1=÷2; 1,0=÷4; 1,1=÷8
9	Clock divisor DIV1	0	
10	Internal Register	0	This bit must be set to 0 for correct sensor operation
11	Not used	0	

Table 15 : Set-up code_1

Note: Decreasing the system clock rate proportionately increases sensor sensitivity (by increasing exposure time), but also decreases frame frequency. System Clock must be x1 for standard CCIR or EIA framing.

Setup Code_2

Header Code = 0010

Valid data bits: 12

The code_2 setup register is used to select read data, valid pixels and video output operating modes:

Bit	Function	Default	Comment
0	Primary read mode (A) enable	0	Select Primary read mode A or B. Note: bits 0,1 are mutually exclusive.
1	Secondary read mode (B) enable	0	
2	Pixel sample clock select (SEL0)	CPE	Pixel sample clock mode (PV/PVB). See below.
3	Pixel sample clock select (SEL1)	0	
4	Not used	0	MUST be set to 0
5	Enable free running pixel clock	0	Overrides SEL0 & SEL1.
6	Enable external pixel thresholds	0	Use external algorithm thresholds in exposure controller
7	Not used	0	MUST be set to 0
8	Not used	0	MUST be set to 0
9	OE[0]	0	AVO output enable control bits [0..2]. See Shuffle Modes above for explanation.
10	OE[1]	0	
11	OE[2]	0	

Table 16 : Setup Code_2

The table below shows the function of SEL0 and SEL1 (Bit 2 and Bit 3); the default value of SEL0 is set by the CPE pin level:

Bit 3	Bit 2	Pixel Clock (PV/PVB pins) function
0	0	Disable pixel clock output
0	1	Qualify full image area (as defined for CCIR or EIA)
1	0	Qualify central 256 x 256 pixels (CCIR only)
1	1	PV/PVB active only during interline periods of visible image lines. Note. This mode is required for digitisation of standard video output.

Table 17 : SEL0 and SEL1 bits

Coarse and Fine Exposure Values.

Header Code (coarse) = 0011

Valid data bits: 9

Header Code (fine) = 0100

Valid data bits: 9

The 18 bit exposure control value is formed from two 9-bit values, coarse (9 msb's) and fine (9 lsb's). For external exposure control (AEC = 0) the exposure value can be set via the serial interface (header codes 0011 and 0100). Values written that exceed the mode dependant maxima will be ignored and the maximum will be used.

Bit	Function	CCIR min	CCIR max	EIA min	EIA max	Comments
0-8	Coarse exposure value	0	310	0	260	Header code 0011
0-8	Fine exposure value	0	404	0	325	Header code 0100
9-11	Unused					

Table 18 : Exposure Values

Exposure Control Thresholds T1 and T2

Header Code (T1) = 1000

Valid data bits: 9

Header Code (T2) = 1001

Valid data bits: 9

The lower and upper pixel count thresholds are used by the automatic exposure controller. The power-on default values for T1 and T2 are exposure mode and video mode dependant. If the external pixel threshold control bit (bit 6 in Setup Code_2 register) is set the internal default values for T1 and T2 are overridden by the serial interface values. Note that only the most significant nine bits of each seventeen bit threshold can be controlled.

Bit	DAC	Comments
0 - 8	Lower Exposure control threshold (T1)	Header Code 1000
0 - 8	Upper Exposure control threshold (T2)	Header Code 1001
9 - 11	Unused	

Table 19 : Pixel Count Thresholds (T1,T2)

Gain and Gain Ceiling

Header Code = 0101

Valid data bits: 4

This register is used to select an external gain value when automatic gain control is inhibited (AGC = 0) and to set the gain ceiling while automatic gain control is active (AGC = 1).

Bit	Function	Default	Comment
0	Gain value G[0]	0	Default gain value
1	Gain value G[1]	0	
2	Gain value G[2]	0	
3	Gain Value G[3]	0	Default gain ceiling
4-11	Unused		

Table 20 : Gain Register

The table below shows the valid gain codes.

G[3]	G[2]	G[1]	G[0]	Gain	Comment
0	0	0	0	1	Default gain value
0	0	0	1	2	
0	0	1	1	4	
0	1	1	1	8	Default gain ceiling
1	1	1	1	16	

Table 21 : Gain Values

Analogue Control Register

Header Code = 1010

Valid data bits: 10

A number of parameters that are used to define internal operations can be altered by the serial interface:

Bit	Function	Default	Comments
0	Internal	1	Must be set(=1) for normal op.
1	Internal	0	Must be 0 for normal op.
2	Internal	0	Must be 0 for normal op.
3	Disable anti-blooming protection	0	
4	Internal	0	Must be 0 for normal op.
5	Internal	0	Must be 0 for normal op.
6	Enable external black reference	0	
7	Enable external white threshold	0	
8	Internal	0	Must be 0 for normal op.
9	Enable binarisation of AVO output	0	AVO output level is either V_{BLACK} or V_{WHITE} for each pixel (see Note)l

Table 22 : Control Register

Note: The Threshold Level above which a pixel is deemed to be WHITE is set via the serial interface, Header Codes 1001 and 1000 (Upper and Lower Exposure Control Thresholds).

Setup Code_3

Header Code = 1110

Valid data bits: 7

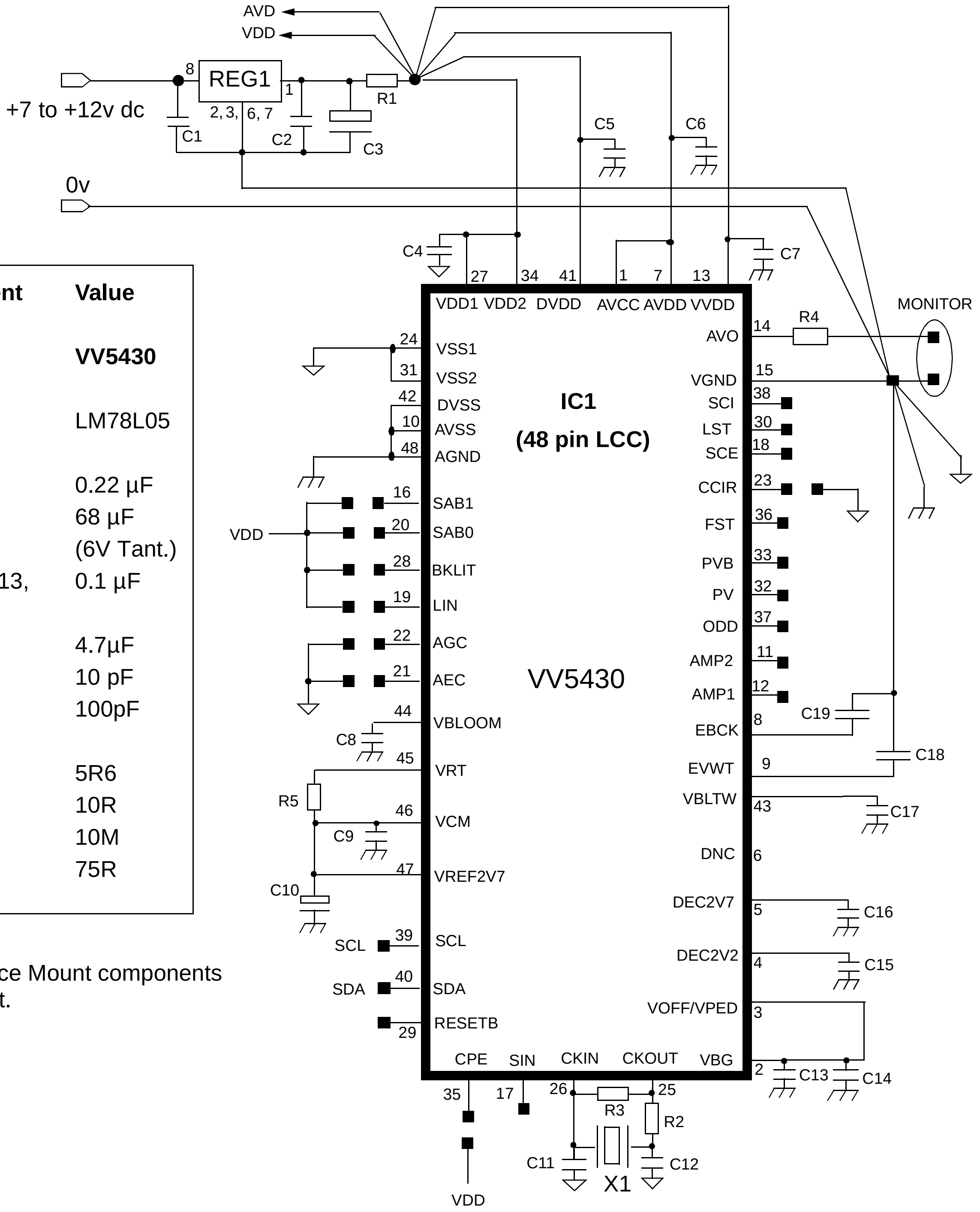
This register stores data used during sensor synchronisation and when the pixel counter in the video timing logic is reset, either at the end of a video line or when the sensor is forced to synchronise externally.

Bit	Function	Default	Comment
5:0	Video timing pixel counter offset	3	Variable offset that is added to the fixed pixel counter preset value when the counter is reset, at the end of a video line or when an external synchronisation is applied
6	Enable SNO	0	Synchronising signal to other cameras in multi-camera applications (see Note)
11:7	Not used	0	

Table 23 : Set-Up Code_3

Note: Enable SNO adjusts the timing of the FST signal (output on pin 36) to correctly synchronise external slave cameras. Alternatively, the synchronising signal for all cameras can be generated externally, which may be more useful in image processing applications.

11. Example Support Circuit



Component	Value
IC1	**VV5430**
REG1	LM78L05
C1,C2	0.22 µF
C3	68 µF (6V Tant.)
C4 - C9,C13, C15 - C19	0.1 µF
C10	4.7µF
C11, C12	10 pF
C14	100pF
R1	5R6
R2	10R
R3	10M
R4	75R

Use Surface Mount components throughout.

1. Keep nodes Supply and Ground pins low impedance and independent
2. Video output should be referred to VGND.
3. Keep circuit components close to chip pins (especially de-coupling capacitors)

12. Ordering Details

STMicroelectronics recommends using their Evaluation Kits for initial evaluation of sensors. For the VV5430 sensors the Evaluation Kit comprises a lensed board camera attached to an embedded microcontroller, and an LCD display in a plastic case. Buttons are provided to control the different options of the sensor in real time. In addition software is provided to allow cont rol of the sensor from a PC running Windows95, via the serial port.

Part Number	Description	Defect specification
VV5430C001	CCIR/EIA Enhanced Mono-chrome Analog Video Image Sensor, 48 pin LCC package	As per Defect Specification, Section 2.2
EVK-5430-001	CCIR Evaluation Kit for VV5430 sensor	As per Defect Specification, Section 2.2
EVK-5430-002	EIA Evaluation Kit for VV5430 sensor	As per Defect Specification, Section 2.2

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