

January 1997

# CD74FCT861A

## BiCMOS FCT Interface Logic, 10-Bit Bus Transceiver, Three-State

### Features

- Buffered Inputs
- Typical Propagation Delay: 6.0ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$
- CD74FCT861A
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and

**NOT RECOMMENDED  
FOR NEW DESIGNS**  
Use CMOS Technology

### Circuit Design

- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at  $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to  $V_{CC}$
- BiCMOS Technology with Low Quiescent Power

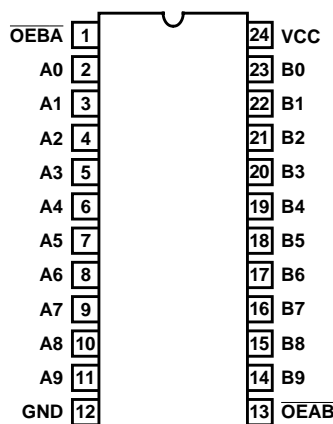
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT861AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

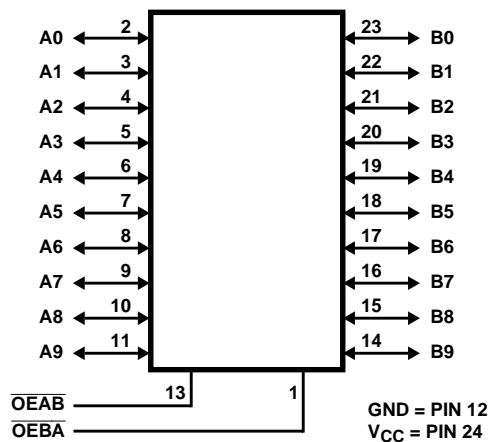
### Pinout

CD74FCT861A  
(SOIC)  
TOP VIEW



CD74FCT861A

Functional Diagram



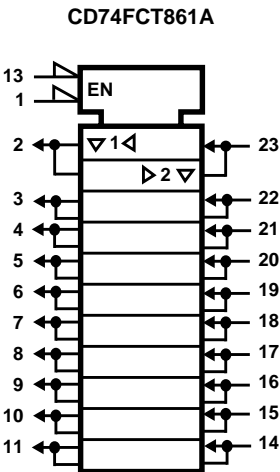
TRUTH TABLE (Note 1)

INPUTS				OUTPUTS		FUNCTION
OEBA	OEAB	B	A	B	A	
L	H	L	N/A	N/A	L	B Data to A Bus
L	H	H	N/A	N/A	H	B Data to A Bus
H	L	N/A	L	L	N/A	A Data to B Bus
H	L	N/A	H	H	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

NOTE:

- 1. H= HIGH Voltage Level
- L = LOW Voltage Level
- N/A = Not Applicable
- X = Immaterial
- Z = HIGH Impedance

IEC Logic Symbol



# CD74FCT861A

## Absolute Maximum Ratings

DC Supply Voltage ( $V_{CC}$ ) . . . . . -0.5V to 6V  
 DC Diode Current,  $I_{IK}$  (For  $V_I < -0.5V$ ) . . . . . -20mA  
 DC Output Diode Current,  $I_{OK}$  (for  $V_O < -0.5V$ ) . . . . . -50mA  
 DC Output Sink Current per Output Pin,  $I_O$  . . . . . 70mA  
 DC Output Source Current per Output Pin,  $I_O$  . . . . . -30mA  
 DC  $V_{CC}$  Current ( $I_{CC}$ ) . . . . . 264mA  
 DC Ground Current ( $I_{GND}$ ) . . . . . 500mA

## Thermal Information

Thermal Resistance (Typical, Note 2)  $\theta_{JA}$  ( $^{\circ}C/W$ )  
 SOIC Package . . . . . 75  
 Maximum Junction Temperature . . . . . 150 $^{\circ}C$   
 Maximum Storage Temperature Range . . . . . -65 $^{\circ}C$  to 150 $^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) . . . . . 300 $^{\circ}C$   
 (Lead Tips Only)

## Operating Conditions

Operating Temperature Range,  $T_A$  . . . . . 0 $^{\circ}C$  to 70 $^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$  . . . . . 4.75V to 5.25V  
 DC Input Voltage,  $V_I$  . . . . . 0 to  $V_{CC}$   
 DC Output Voltage,  $V_O$  . . . . . 0 to  $\leq V_{CC}$   
 Input Rise and Fall Slew Rate,  $dt/dv$  . . . . . 0 to 10ns/V

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$ , $V_{CC}$ Max = 5.25V, $V_{CC}$ Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> )				UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		25°C		0°C TO 70°C		
					MIN	MAX	MIN	MAX	
High Level Input Voltage	V <sub>IH</sub>			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	48	Min	-	0.55	-	0.55	V
High Level Input Current	I <sub>IH</sub>	V <sub>CC</sub>		Max	-	0.1	-	1	μA
Low Level Input Current	I <sub>IL</sub>	GND		Max	-	-0.1	-	-1	μA
Three State Leakage Current	I <sub>OZH</sub>	V <sub>CC</sub>		Max	-	0.5	-	10	μA
	I <sub>OZL</sub>	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V <sub>IK</sub>	V <sub>CC</sub> or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I <sub>OS</sub>	V <sub>O</sub> = 0 V <sub>CC</sub> or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI <sub>CC</sub>	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at  $V_{CC}$  or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70 $^{\circ}C$ .

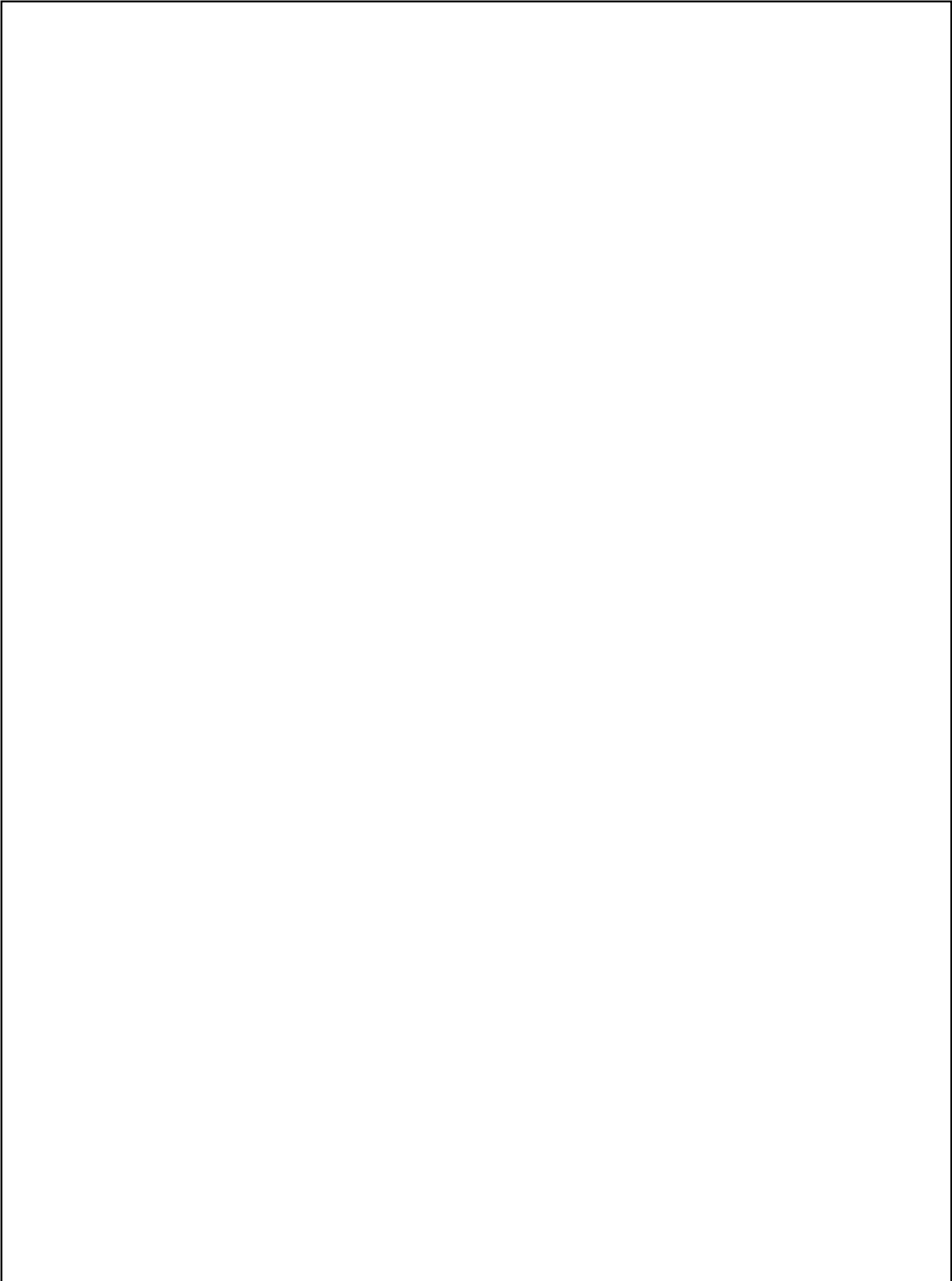
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## Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$ , $C_L = 50\text{pF}$ , $R_L$ (Figure 1)

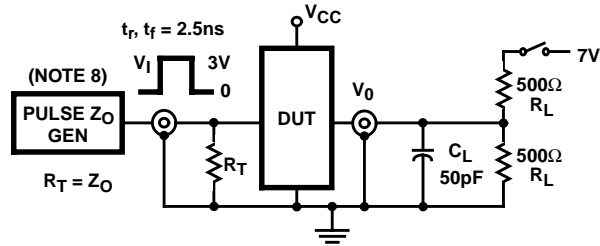
PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays						
Data to Outputs	$t_{PLH}, t_{PHL}$	5 (Note 6)	6	1.5	8	ns
Output Enable to Output	$t_{PZL}, t_{PZH}$	5	9	1.5	12	ns
Output Disable to Output	$t_{PLZ}, t_{PHZ}$	5	7.5	1.5	10	ns
Power Dissipation Capacitance	$C_{PD}$ (Note 7)	-	-	-	-	pF
Minimum (Valley) $V_{OHV}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$	5	0.5	-	-	V
Maximum (Peak) $V_{OLP}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$	5	1	-	-	V
Input Capacitance	$C_I$	-	-	-	10	pF
Three-State Output Capacitance	$C_O$	-	-	-	15	pF

### NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7.  $C_{PD}$ , measured per flip-flop, is used to determine the dynamic power consumption.  
 $P_D$  (per package) =  $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$  where:  
 $V_{CC}$  = supply voltage  
 $\Delta I_{CC}$  = flow through current x unit load  
 $C_L$  = output load capacitance  
 $D$  = duty cycle of input high  
 $f_O$  = output frequency  
 $f_I$  = input frequency



## Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{\text{OUT}} \leq 50\Omega$ ;  
 $t_r, t_f \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

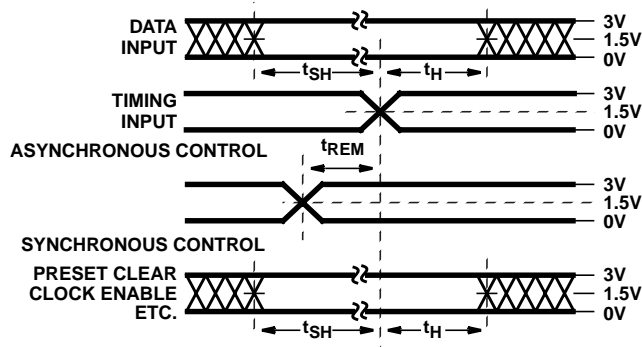


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

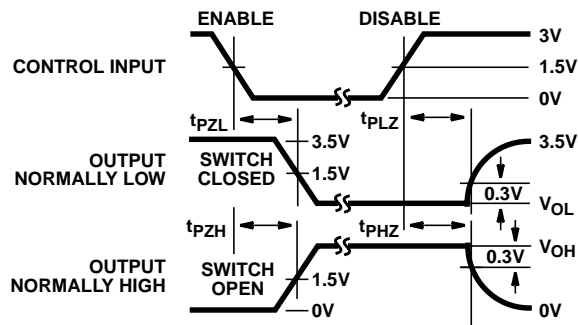


FIGURE 4. ENABLE AND DISABLE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{\text{PLZ}}, t_{\text{PZL}}, \text{Open Drain}$	Closed
$t_{\text{PHZ}}, t_{\text{PZH}}, t_{\text{PLH}}, t_{\text{PHL}}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.

$R_T$  = Termination resistance, should be equal to  $Z_{\text{OUT}}$  of the Pulse Generator.

$V_{\text{IN}} = 0\text{V}$  to  $3\text{V}$ .

Input:  $t_r = t_f = 2.5\text{ns}$  (10% to 90%), unless otherwise specified

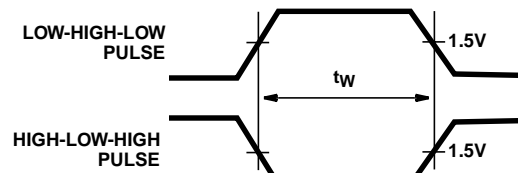


FIGURE 3. PULSE WIDTH

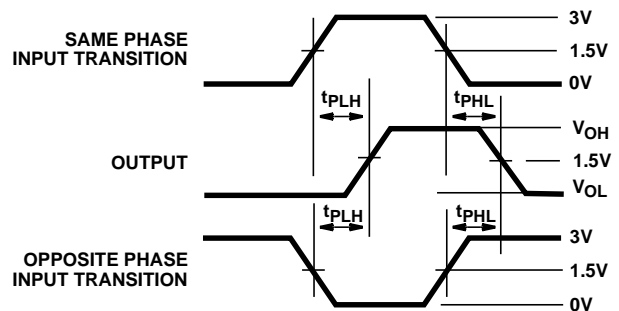
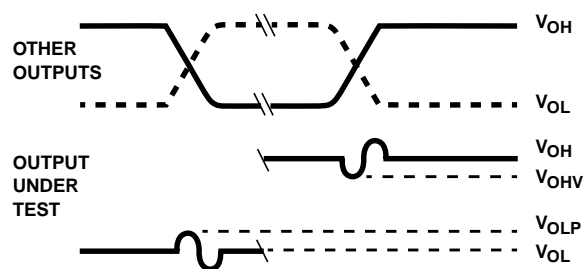


FIGURE 5. PROPAGATION DELAY

## Test Circuits and Waveforms (Continued)



### NOTES:

9.  $V_{OLP}$  is measured with respect to a ground reference near the output under test.  $V_{OHV}$  is measured with respect to  $V_{OH}$ .
10. Input pulses have the following characteristics:  
 $P_{RR} \leq 1\text{MHz}$ ,  $t_r = 2.5\text{ns}$ ,  $t_f = 2.5\text{ns}$ , skew  $1\text{ns}$ .
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with  $0.1\mu\text{F}$  capacitor. Scope and probes require 700MHz bandwidth.

**FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS**

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