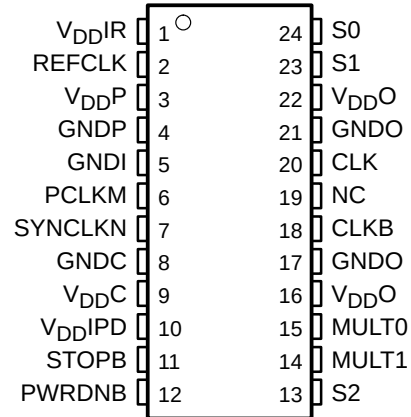


- 533-MHz Differential Clock Source for Direct Rambus™ Memory Systems for an 1066-MHz Data Transfer Rate
- Synchronizes the Clock Domains of the Rambus Channel With an External System or Processor Clock
- Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications
- Operates From a Single 3.3-V Supply and 120 mW at 300 MHz (Typ)
- Packaged in a Shrink Small-Outline Package (DBQ)
- Supports Frequency Multipliers: 4, 6, 8, 16/3
- No External Components Required for PLL
- Supports Independent Channel Clocking
- Spread Spectrum Clocking Tracking Capability to Reduce EMI
- Designed for Use With TI's 133-MHz Clock Synthesizers CDC924 and CDC921
- Cycle-Cycle Jitter Is Less Than 40 ps at 533 MHz
- Certified by Gigatest Labs to Exceed the Rambus DRCG Validation Requirement
- Supports Industrial Temperature Range of –40°C to 85°C

DBQ PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on a desktop, workstation, server, and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLKM = SYNCLKN, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLKM and SYNCLKN and adjusts the phase of BUSCLK such that the skew between PCLKM and SYNCLKN is minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 533 MHz with clock references ranging from 33 MHz to 100 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.

The CDCFR83 is characterized for operation over free-air temperatures of –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



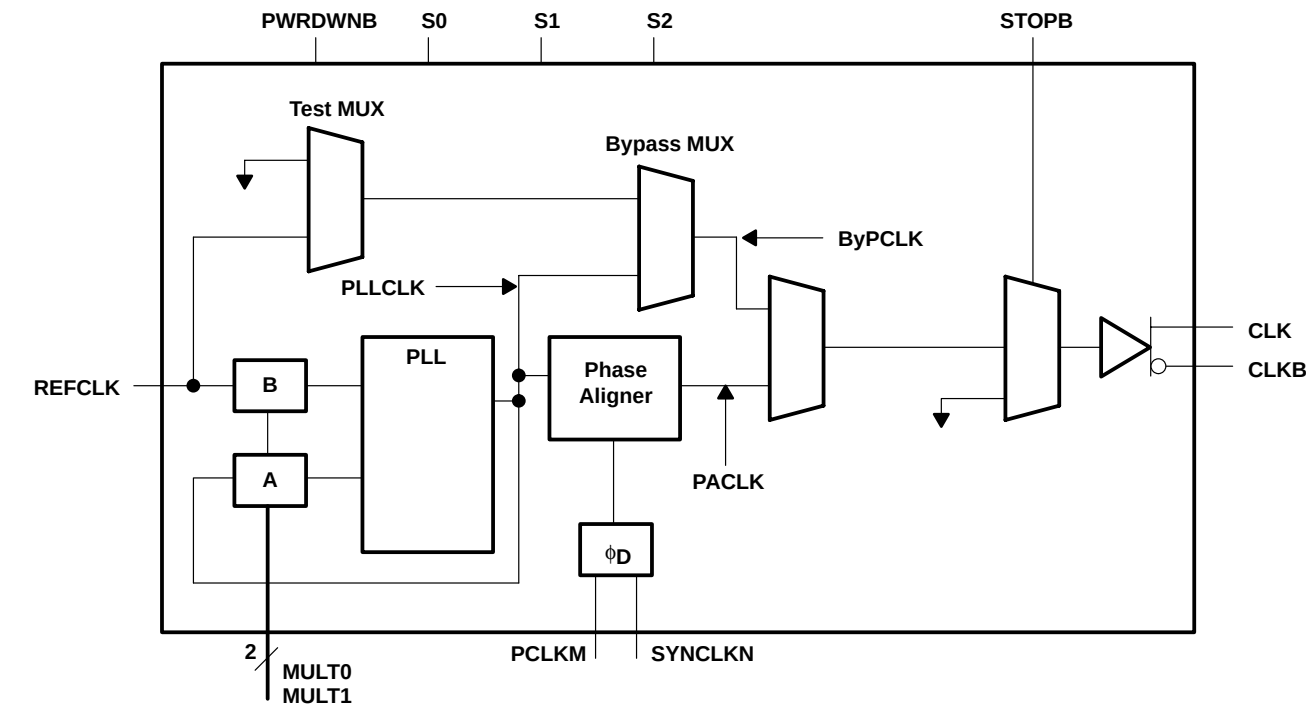
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CDCFR83  
DIRECT RAMBUS™ CLOCK GENERATOR

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functional block diagram



FUNCTION TABLE†

| MODE             | S0 | S1 | S2 | CLK                 | CLKB                  |
|------------------|----|----|----|---------------------|-----------------------|
| Normal           | 0  | 0  | 0  | Phase aligned clock | Phase aligned clock B |
| Bypass           | 1  | 0  | 0  | PLLCLK              | PLLCLKB               |
| Test             | 1  | 1  | 0  | REFCLK              | REFCLKB               |
| Output test (OE) | 0  | 1  | X  | Hi-Z                | Hi-Z                  |
| Reserved         | 0  | 0  | 1  | —                   | —                     |
| Reserved         | 1  | 0  | 1  | —                   | —                     |
| Reserved         | 1  | 1  | 1  | Hi-Z                | Hi-Z                  |

† X = don't care, Hi-Z = high impedance

### Terminal Functions

| TERMINAL<br>NAME   | NO.    | I/O | DESCRIPTION                                           |
|--------------------|--------|-----|-------------------------------------------------------|
| CLK                | 20     | O   | Output clock                                          |
| CLKB               | 18     | O   | Output clock (complement)                             |
| GNDC               | 8      |     | GND for phase aligner                                 |
| GNDI               | 5      |     | GND for control inputs                                |
| GNDO               | 17, 21 |     | GND for clock outputs                                 |
| GNDP               | 4      |     | GND for PLL                                           |
| MULT0              | 15     | I   | PLL multiplier select                                 |
| MULT1              | 14     | I   | PLL multiplier select                                 |
| NC                 | 19     |     | Not used                                              |
| PCLKM              | 6      | I   | Phase detector input                                  |
| PWRDNB             | 12     | I   | Active low power down                                 |
| REFCLK             | 2      | I   | Reference clock                                       |
| S0                 | 24     | I   | Mode control                                          |
| S1                 | 23     | I   | Mode control                                          |
| S2                 | 13     | I   | Mode control                                          |
| STOPB              | 11     | I   | Active low output disable                             |
| SYNCLKN            | 7      | I   | Phase detector input                                  |
| V <sub>DDC</sub>   | 9      |     | V <sub>DD</sub> for phase aligner                     |
| V <sub>DDIPD</sub> | 10     |     | Reference voltage for phase detector inputs and STOPB |
| V <sub>DDIR</sub>  | 1      |     | Reference voltage for REFCLK                          |
| V <sub>DDO</sub>   | 16, 22 |     | V <sub>DD</sub> for clock outputs                     |
| V <sub>DDP</sub>   | 3      |     | V <sub>DD</sub> for PLL                               |

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## PLL divider selection

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 533 MHz) and (33 MHz < REFCLK < 100 MHz).

**Table 1. REFCLK and BUSCLK Frequencies**

| MULT0 | MULT1 | REFCLK (MHz) | MULTIPLY RATIO | BUSCLK (MHz) |
|-------|-------|--------------|----------------|--------------|
| 0     | 0     | 67           | 4              | 267          |
| 0     | 1     | 50           | 6              | 300          |
| 0     | 1     | 67           | 6              | 400          |
| 1     | 1     | 33           | 8              | 267          |
| 1     | 1     | 50           | 8              | 400          |
| 1     | 1     | 67           | 8              | 533          |
| 1     | 0     | 67           | 16/3           | 356          |

**Table 2. Clock Output Driver States**

| STATE     | PWRDNB | STOPB | CLK                      | CLKB                        |
|-----------|--------|-------|--------------------------|-----------------------------|
| Powerdown | 0      | X     | GND                      | GND                         |
| CLK stop  | 1      | 0     | V <sub>X</sub> , STOP    | V <sub>X</sub> , STOP       |
| Normal    | 1      | 1     | PACLK/PLLCLK/<br>REFCLK† | PACCLKB/PLLCLKB/<br>REFCLKB |

† Depending on the state of S0, S1, and S2

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V<sub>DD</sub> (see Note 1) ..... –0.5 V to 4 V  
 Output voltage range, V<sub>O</sub>, at any output terminal ..... –0.5 V to V<sub>DD</sub> + 0.5 V  
 Input voltage range, V<sub>I</sub>, at any input terminal ..... –0.5 V to V<sub>DD</sub> + 0.5 V  
 Continuous total power dissipation ..... see Dissipation Rating Table  
 Operating free-air temperature range, T<sub>A</sub> ..... –40°C to 85°C  
 Storage temperature range, T<sub>stg</sub> ..... –65°C to 150°C  
 Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

**DISSIPATION RATING TABLE**

| PACKAGE | T <sub>A</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C‡ | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|---------------------------------------|-------------------------------------------------|---------------------------------------|---------------------------------------|
| DBQ     | 1400 mW                               | 11 mW/°C                                        | 905 mW                                | 740 mW                                |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



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### recommended operating conditions

|                                                                                 | MIN                                               | NOM | MAX   | UNIT |
|---------------------------------------------------------------------------------|---------------------------------------------------|-----|-------|------|
| Supply voltage, $V_{DD}$                                                        | 3.135                                             | 3.3 | 3.465 | V    |
| High-level input voltage, $V_{IH}$ (CMOS)                                       | $0.7 \times V_{DD}$                               |     |       | V    |
| Low-level input voltage, $V_{IL}$ (CMOS)                                        | $0.3 \times V_{DD}$                               |     |       | V    |
| Initial phase error at phase detector inputs (required range for phase aligner) | $-0.5 \times t_{c(PD)}$ to $0.5 \times t_{c(PD)}$ |     |       |      |
| REFCLK low-level input voltage, $V_{IL}$                                        | $0.3 \times V_{DDIR}$                             |     |       | V    |
| REFCLK high-level input voltage, $V_{IH}$                                       | $0.7 \times V_{DDIR}$                             |     |       | V    |
| Input signal low voltage, $V_{IL}$ (STOPB)                                      | $0.3 \times V_{DDIPD}$                            |     |       | V    |
| Input signal high voltage, $V_{IH}$ (STOPB)                                     | $0.7 \times V_{DDIPD}$                            |     |       | V    |
| Input reference voltage for (REFCLK) ( $V_{DDIR}$ )                             | 1.235                                             |     | 3.465 | V    |
| Input reference voltage for (PCLKM and SYSCLKN) ( $V_{DDIPD}$ )                 | 1.235                                             |     | 3.465 | V    |
| High-level output current, $I_{OH}$                                             |                                                   |     | -16   | mA   |
| Low-level output current, $I_{OL}$                                              |                                                   |     | 16    | mA   |
| Operating free-air temperature, $T_A$                                           | -40                                               |     | 85    | °C   |

### timing requirements

|                                                     | MIN | MAX  | UNIT |
|-----------------------------------------------------|-----|------|------|
| Input cycle time, $t_{c(in)}$                       | 10  | 40   | ns   |
| Input cycle-to-cycle jitter                         |     | 250  | ps   |
| Input duty cycle over 10,000 cycles                 | 40% | 60%  |      |
| Input frequency modulation, $f_{mod}$               | 30  | 33   | kHz  |
| Modulation index, nonlinear maximum 0.5%            |     | 0.6% |      |
| Phase detector input cycle time (PCLKM and SYNCLKN) | 30  | 100  | ns   |
| Input slew rate, SR                                 | 1   | 4    | V/ns |
| Input duty cycle (PCLKM and SYNCLKN)                | 25% | 75%  |      |

# CDCFR83

## DIRECT RAMBUS™ CLOCK GENERATOR

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                |                                                         |                                                                  | TEST CONDITIONS†                                            |            | MIN                     | TYP‡ | MAX  | UNIT |
|--------------------------|---------------------------------------------------------|------------------------------------------------------------------|-------------------------------------------------------------|------------|-------------------------|------|------|------|
| V <sub>O(STOP)</sub>     | Output voltage during CLK Stop (STOPB = 0)              |                                                                  | See Figure 1                                                |            | 1.1                     |      | 2    |      |
| V <sub>O(X)</sub>        | Output crossing-point voltage                           |                                                                  | See Figure 1 and Figure 6                                   |            | 1.3                     |      | 1.8  | V    |
| V <sub>O</sub>           | Output voltage swing                                    |                                                                  | See Figure 1                                                |            | 0.4                     |      | 0.6  | V    |
| V <sub>IK</sub>          | Input clamp voltage                                     |                                                                  | V <sub>DD</sub> = 3.135 V, I <sub>I</sub> = −18 mA          |            |                         |      | −1.2 | V    |
| V <sub>OH</sub>          | High-level output voltage                               |                                                                  | See Figure 1                                                |            |                         |      | 2    | V    |
|                          |                                                         |                                                                  | V <sub>DD</sub> = min to max, I <sub>OH</sub> = −1 mA       |            | V <sub>DD</sub> − 0.1 V |      |      |      |
|                          |                                                         |                                                                  | V <sub>DD</sub> = 3.135 V, I <sub>OH</sub> = −16 mA         |            | 2.4                     |      |      |      |
| V <sub>OL</sub>          | Low-level output voltage                                |                                                                  | See Figure 1                                                |            | 1                       |      |      | V    |
|                          |                                                         |                                                                  | V <sub>DD</sub> = min to max, I <sub>OL</sub> = 1 mA        |            | 0.1                     |      |      |      |
|                          |                                                         |                                                                  | V <sub>DD</sub> = 3.135 V, I <sub>OL</sub> = 16 mA          |            | 0.5                     |      |      |      |
| I <sub>OH</sub>          | High-level output current                               |                                                                  | V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1 V             |            | −32                     | −52  |      | mA   |
|                          |                                                         |                                                                  | V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V            |            | −51                     |      |      |      |
|                          |                                                         |                                                                  | V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 3.135 V         |            | −14.5                   | −21  |      |      |
| I <sub>OL</sub>          | Low-level output current                                |                                                                  | V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1.95 V          |            | 43                      | 61.5 |      | mA   |
|                          |                                                         |                                                                  | V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V            |            | 65                      |      |      |      |
|                          |                                                         |                                                                  | V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 0.4 V           |            | 25.5                    | 36   |      |      |
| I <sub>OZ</sub>          | High-impedance-state output current                     |                                                                  | S0 = 0, S1 = 1                                              |            |                         |      | ±10  | μA   |
| I <sub>OZ(STOP)</sub>    | High-impedance-state output current during CLK stop     |                                                                  | Stop = 0, V <sub>O</sub> = GND or V <sub>DD</sub>           |            |                         |      | ±100 | μA   |
| I <sub>OZ(PD)</sub>      | High-impedance-state output current in power-down state |                                                                  | PWRDNB = 0, V <sub>O</sub> = GND or V <sub>DD</sub>         |            | −10                     |      | 100  | μA   |
| I <sub>IH</sub>          | High-level input current                                | REFCLK, PCLKM, SYNCLKN, STOPB                                    | V <sub>DD</sub> = 3.465 V, V <sub>I</sub> = V <sub>DD</sub> |            |                         |      | 10   | μA   |
|                          |                                                         | PWRDNB, S0, S1, S2, MULT0, MULT1                                 | V <sub>DD</sub> = 3.465 V, V <sub>I</sub> = V <sub>DD</sub> |            |                         |      | 10   |      |
| I <sub>IL</sub>          | Low-level input current                                 | REFCLK, PCLKM, SYNCLKN, STOPB                                    | V <sub>DD</sub> = 3.465 V, V <sub>I</sub> = 0               |            |                         |      | −10  | μA   |
|                          |                                                         | PWRDNB, S0, S1, S2, MULT0, MULT1                                 | V <sub>DD</sub> = 3.465 V, V <sub>I</sub> = 0               |            |                         |      | −10  |      |
| Z <sub>O</sub>           | Output impedance                                        | High state                                                       | R <sub>I</sub> at I <sub>O</sub> −14.5 mA to −16.5 mA       |            | 15                      | 35   | 50   | Ω    |
|                          |                                                         | Low state                                                        | R <sub>I</sub> at I <sub>O</sub> 14.5 mA to 16.5 mA         |            | 11                      | 17   | 35   |      |
|                          | Reference current                                       | V <sub>DD</sub> I <sub>R</sub> , V <sub>DD</sub> I <sub>PD</sub> | V <sub>DD</sub> = 3.465 V                                   | PWRDNB = 0 |                         |      | 50   | μA   |
|                          |                                                         |                                                                  |                                                             | PWRDNB = 1 |                         |      | 0.5  | mA   |
| C <sub>I</sub>           | Input capacitance                                       |                                                                  | V <sub>I</sub> = V <sub>DD</sub> or GND                     |            |                         |      | 2    | pF   |
| C <sub>O</sub>           | Output capacitance                                      |                                                                  | V <sub>O</sub> = V <sub>DD</sub> or GND                     |            |                         |      | 3    | pF   |
| I <sub>DD(PD)</sub>      | Supply current in power-down state                      |                                                                  | REFCLK = 0 MHz to 100 MHz, PWDNB = 0, STOPB = 1             |            |                         |      | 100  | μA   |
| I <sub>DD(CLKSTOP)</sub> | Supply current in CLK stop state                        |                                                                  | BUSCLK configured for 533 MHz                               |            |                         |      | 45   | mA   |
| I <sub>DD(NORMAL)</sub>  | Supply current in normal state                          |                                                                  | BUSCLK = 533 MHz                                            |            |                         |      | 100  | mA   |

†  $V_{DD}$  refers to any of the following;  $V_{DD}$ ,  $V_{DD}I_{PD}$ ,  $V_{DD}I_R$ ,  $V_{DD}O$ ,  $V_{DD}C$ , and  $V_{DD}P$

‡ All typical values are at  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



**switching characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                       |                                                                                                      |                                      |          | TEST CONDITIONS                  | MIN  | TYP <sup>†</sup> | MAX  | UNIT |
|---------------------------------|------------------------------------------------------------------------------------------------------|--------------------------------------|----------|----------------------------------|------|------------------|------|------|
| t <sub>c(out)</sub>             | Clock output cycle time                                                                              |                                      |          |                                  | 1.87 |                  | 3.75 | ns   |
| t <sub>(jitter)</sub>           | Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles                                             | Infinite and stopped phase alignment | 267 MHz  | See Figure 3                     |      |                  | 80   | ps   |
|                                 |                                                                                                      |                                      | 300 MHz  |                                  |      |                  | 70   |      |
|                                 |                                                                                                      |                                      | 356 MHz  |                                  |      |                  | 60   |      |
|                                 |                                                                                                      |                                      | 400 MHz  |                                  |      |                  | 50   |      |
|                                 |                                                                                                      |                                      | 533 MHz§ |                                  |      |                  | 40   |      |
| t <sub>(phase)</sub>            | Phase detector phase error for distributed loop                                                      |                                      |          | Static phase error <sup>‡</sup>  | –100 |                  | 100  | ps   |
| t <sub>(phase, SSC)</sub>       | PLL output phase error when tracking SSC                                                             |                                      |          | Dynamic phase error <sup>‡</sup> | –100 |                  | 100  | ps   |
| t <sub>(DC)</sub>               | Output duty cycle over 10,000 cycles                                                                 |                                      |          | See Figure 4                     | 45%  |                  | 55%  |      |
| t <sub>(DC, err)</sub>          | Output cycle-to-cycle duty cycle error                                                               | Infinite and stopped phase alignment | 267 MHz  | See Figure 5                     |      |                  | 80   | ps   |
|                                 |                                                                                                      |                                      | 300 MHz  |                                  |      |                  | 70   |      |
|                                 |                                                                                                      |                                      | 356 MHz  |                                  |      |                  | 60   |      |
|                                 |                                                                                                      |                                      | 400 MHz  |                                  |      |                  | 50   |      |
|                                 |                                                                                                      |                                      | 533 MHz  |                                  |      |                  | 50   |      |
| t <sub>r</sub> , t <sub>f</sub> | Output rise and fall times (measured at 20%–80% of output voltage)                                   |                                      |          | See Figure 7                     | 160  |                  | 400  | ps   |
| Δt                              | Difference between rise and fall times on a single device (20%–80%)  t <sub>f</sub> – t <sub>r</sub> |                                      |          | See Figure 7                     |      |                  | 100  | ps   |

<sup>†</sup> All typical values are at V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> Assured by design

<sup>§</sup> Jitter measurement according to Rambus validation specification

**state transition latency specifications**

| PARAMETER                 |                                                                                          | FROM            | TO       | TEST CONDITIONS | MIN | TYP <sup>†</sup> | MAX | UNIT   |
|---------------------------|------------------------------------------------------------------------------------------|-----------------|----------|-----------------|-----|------------------|-----|--------|
| t <sub>(powerup)</sub>    | Delay time, PWRDNB↑ to CLK/CLKB output settled (excluding t <sub>(DISTLOCK)</sub> )      | Powerdown       | Normal   | See Figure 8    |     |                  | 3   | ms     |
|                           | Delay time, PWRDNB↑ to internal PLL and clock are on and settled                         |                 |          |                 |     |                  | 3   |        |
| t <sub>(VDDpowerup)</sub> | Delay time, power up to CLK/CLKB output settled                                          | V <sub>DD</sub> | Normal   | See Figure 8    |     |                  | 3   | ms     |
|                           | Delay time, power up to internal PLL and clock are on and settled                        |                 |          |                 |     |                  | 3   |        |
| t <sub>(MULT)</sub>       | MULT0 and MULT1 change to CLK/CLKB output resettled (excluding t <sub>(DISTLOCK)</sub> ) | Normal          | Normal   | See Figure 9    |     |                  | 1   | ms     |
| t <sub>(CLKON)</sub>      | STOPB↑ to CLK/CLKB glitch-free clock edges                                               | CLK Stop        | Normal   | See Figure 10   |     |                  | 10  | ns     |
| t <sub>(CLKSETL)</sub>    | STOPB↑ to CLK/CLKB output settled to within 50 ps of the phase before STOPB was disabled | CLK Stop        | Normal   | See Figure 10   |     |                  | 20  | cycles |
| t <sub>(CLKOFF)</sub>     | STOPB↓ to CLK/CLKB output disabled                                                       | Normal          | CLK Stop | See Figure 10   |     |                  | 5   | ns     |

<sup>†</sup> All typical values are at V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C.

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## state transition latency specifications (continued)

| PARAMETER                | FROM                                                                                                                           | TO       | TEST CONDITIONS | MIN           | TYP† | MAX | UNIT |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------|-----------------|---------------|------|-----|------|
| $t_{(\text{powerdown})}$ | Delay time, PWRDNB↓ to the device in the power-down mode                                                                       | Normal   | Powerdown       | See Figure 8  |      | 1   | ms   |
| $t_{(\text{STOP})}$      | Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)                                                  | STOPB    | Normal          | See Figure 10 |      | 100 | μs   |
| $t_{(\text{ON})}$        | Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)                                                  | Normal   | CLK stop        | See Figure 10 | 100  |     | ms   |
| $t_{(\text{DISTLOCK})}$  | Time from when CLK/CLKB output is settled to when the phase error between SYNCCLKN and PCLKM falls within $t_{(\text{phase})}$ | Unlocked | Locked          |               |      | 5   | ms   |

† All typical values are at  $V_{DD} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION

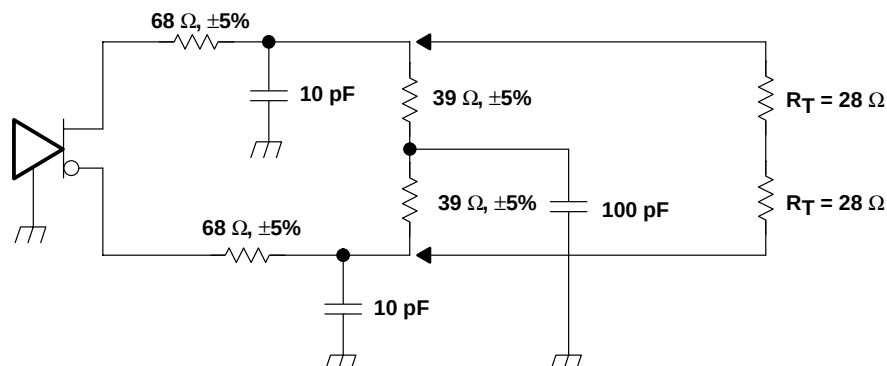
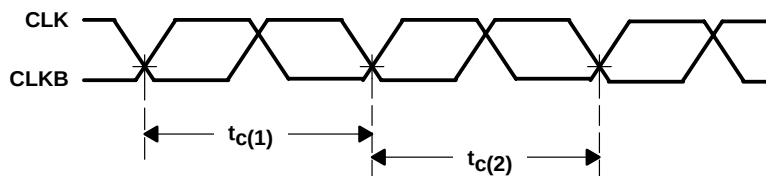


Figure 1. Test Load and Voltage Definitions ( $V_{O(\text{STOP})}$ ,  $V_{O(X)}$ ,  $V_O$ ,  $V_{OH}$ ,  $V_{OL}$ )

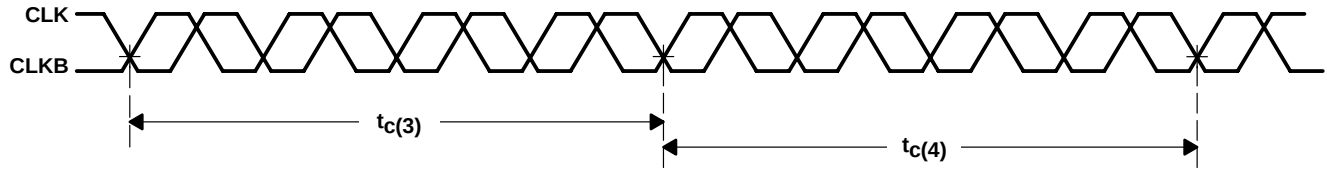


Cycle-to-cycle jitter =  $|t_{c(1)} - t_{c(2)}|$  over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter

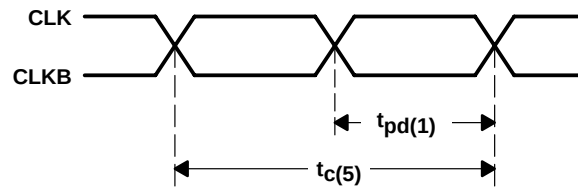


### PARAMETER MEASUREMENT INFORMATION



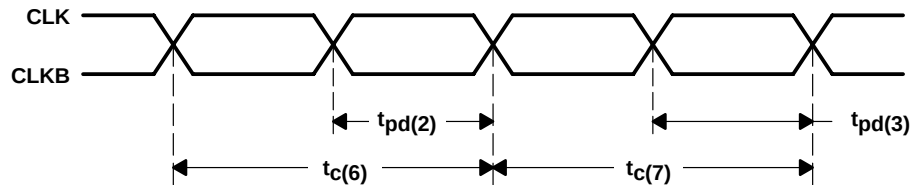
Cycle-to-cycle jitter =  $|t_{c(3)} - t_{c(4)}|$  over 10000 consecutive cycles

**Figure 3. Short Term Cycle-to-Cycle Jitter Over Four Cycles**



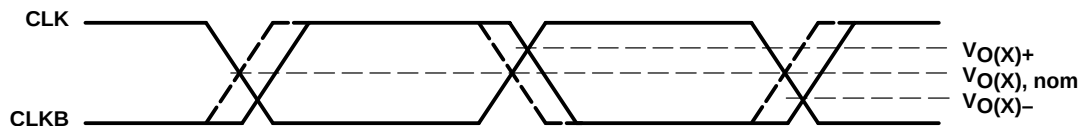
Duty cycle =  $(t_{pd(1)}/t_{c(5)})$

**Figure 4. Output Duty Cycle**



Duty cycle error =  $t_{pd(2)} - t_{pd(3)}$

**Figure 5. Duty Cycle Error (Cycle-to-Cycle)**

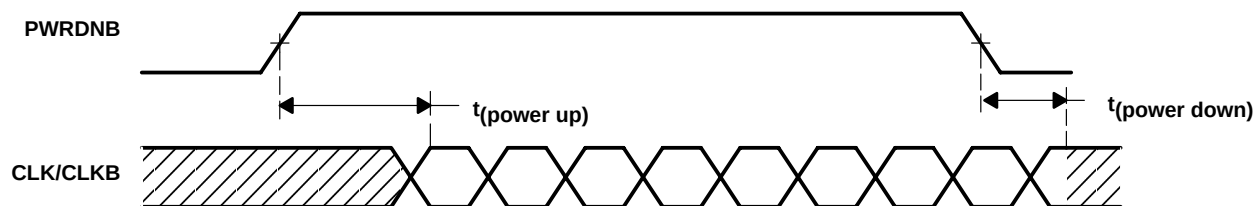


**Figure 6. Crossing-Point Voltage**

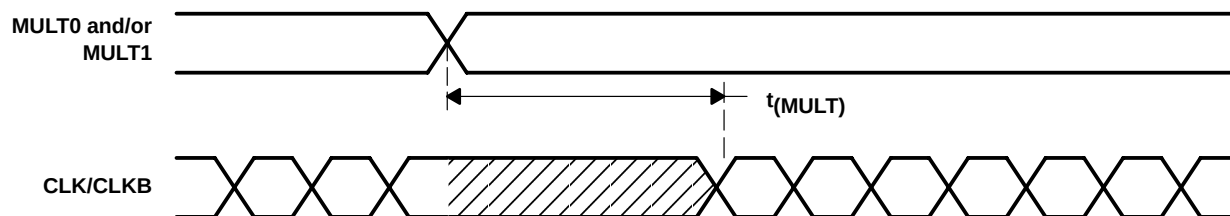


**Figure 7. Voltage Waveforms**

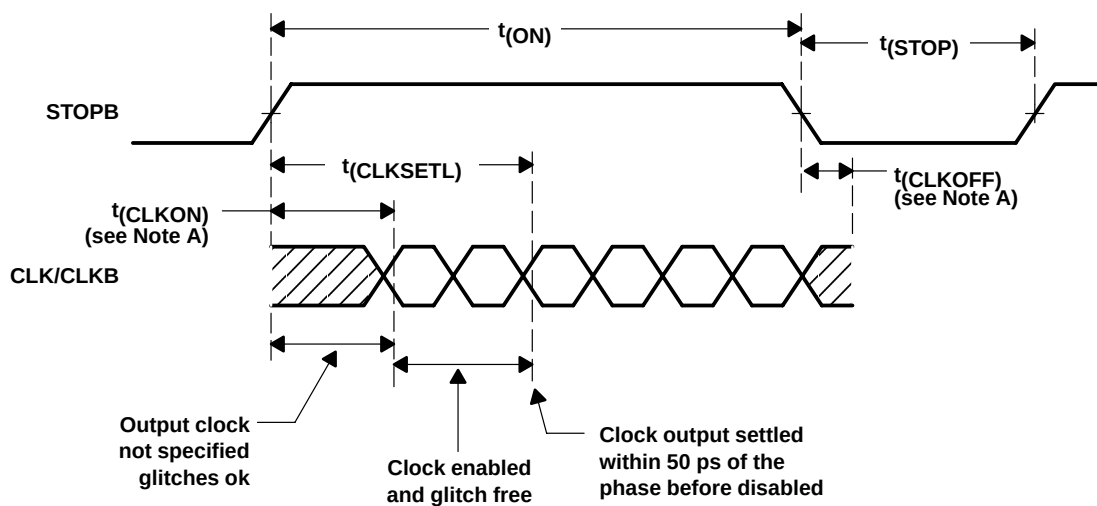
**PARAMETER MEASUREMENT INFORMATION**



**Figure 8. PWRDNB Transition Timings**



**Figure 9. MULT Transition Timings**



NOTE A:  $V_{ref} = V_O \pm 200 \text{ mV}$

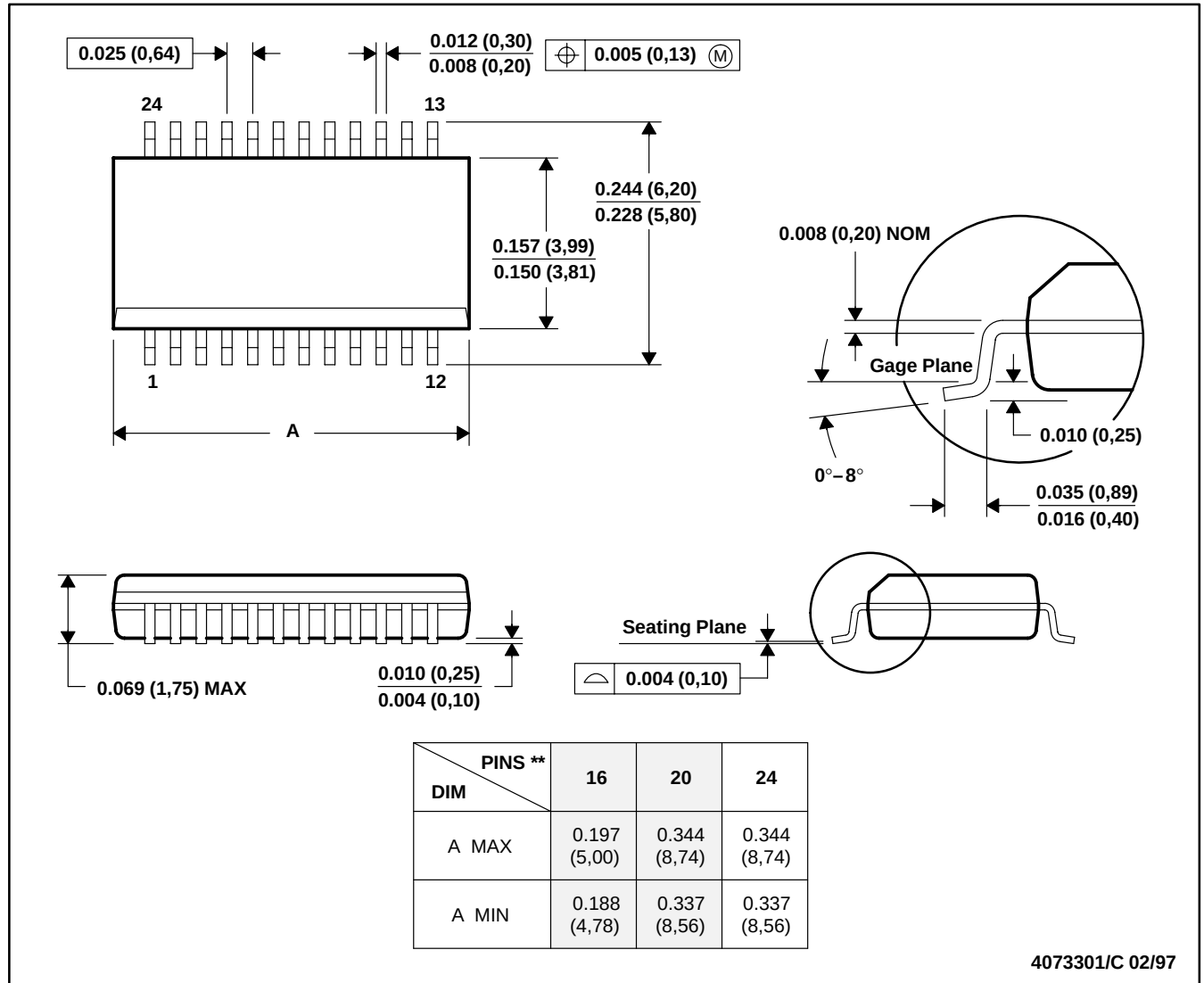
**Figure 10. STOPB Transition Timings**

## MECHANICAL DATA

**DBQ (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**24-PIN SHOWN**



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-137

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Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265