

24-BIT STEREO AUDIO CODEC WITH 96-kHz ADC, 192-kHz DAC, AND SINGLE-ENDED ANALOG INPUT/OUTPUT

FEATURES

- 24-Bit Delta-Sigma ADC and DAC
- Stereo ADC:
 - Single-Ended Voltage Input: 3 V_{p-p}
 - Antialiasing Filter Included
 - 1/128, 1/64 Decimation Filter:
 - Pass-Band Ripple: ±0.05 dB
 - Stop-Band Attenuation: –65 dB
 - On-Chip High-Pass Filter: 0.84 Hz at f_S = 44.1 kHz
 - High Performance:
 - THD+N: –95 dB (Typical)
 - SNR: 100 dB (Typical)
 - Dynamic Range: 102 dB (Typical)
- Stereo DAC:
 - Single-Ended Voltage Output: 3 V_{p-p}
 - Analog Low-Pass Filter Included
 - ×8 Oversampling Digital Filter:
 - Pass-Band Ripple: ±0.03 dB
 - Stop-Band Attenuation: –50 dB
 - High Performance:
 - THD+N: –96 dB (Typical)
 - SNR: 104 dB (Typical)
 - Dynamic Range: 104 dB (Typical)
- Multiple Functions:
 - Digital De-Emphasis: 32 kHz, 44.1 kHz, 48 kHz
 - Power Down: ADC/DAC Simultaneous
 - 16-, 24-Bit Audio Data Formats
- Sampling Rate: 16–96 kHz (ADC), 16–192 kHz (DAC)

- System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S
- Dual Power Supplies: 5 V for Analog and 3.3 V for Digital
- Package: 24-Pin SSOP, Lead-Free Product

APPLICATIONS

- DVD Recorders
- CD Recorders
- PC Audio
- Sound Control System

DESCRIPTION

The PCM3010 is a low-cost single-chip 24-, 16-bit stereo audio codec (ADC and DAC) with single-ended analog voltage input and output. Both the analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) employ delta-sigma modulation with 64-times oversampling. The ADCs include a digital decimation filter with a high-pass filter, and the DACs include an 8-times-oversampling digital interpolation filter. The DACs also include a digital de-emphasis function. The PCM3010 accepts four different audio data formats for the ADC and DAC. The PCM3010 provides a power-down mode, which works on the ADC and DAC simultaneously. The PCM3010 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. The PCM3010 is fabricated using a highly advanced CMOS process and is available in a small 24-pin SSOP package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

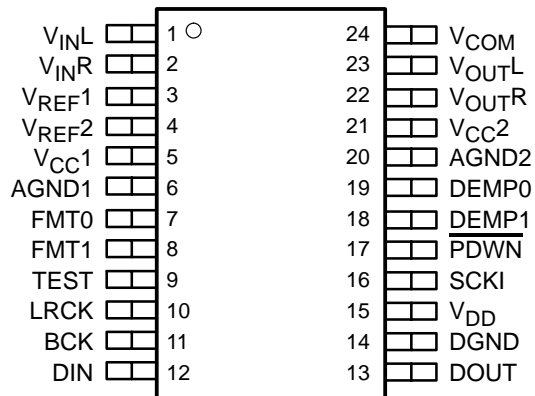


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PCM3010

SLES055 – NOVEMBER 2002

DB PACKAGE (TOP VIEW)



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM3010DB	24-lead SSOP	24DB	-25°C to 85°C	PCM3010	PCM3010DB	Tube
					PCM3010DBR	Tape and reel

block diagram

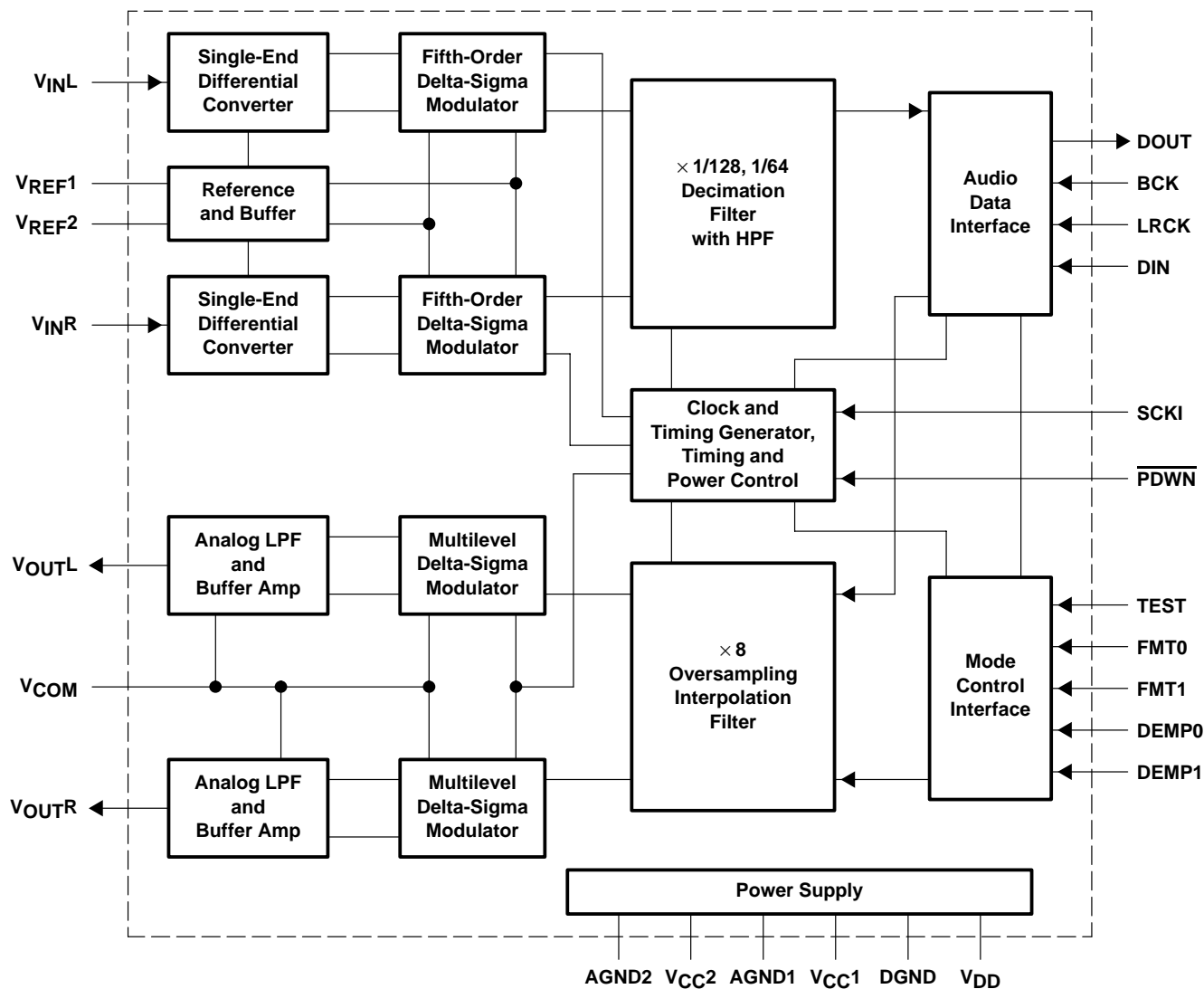
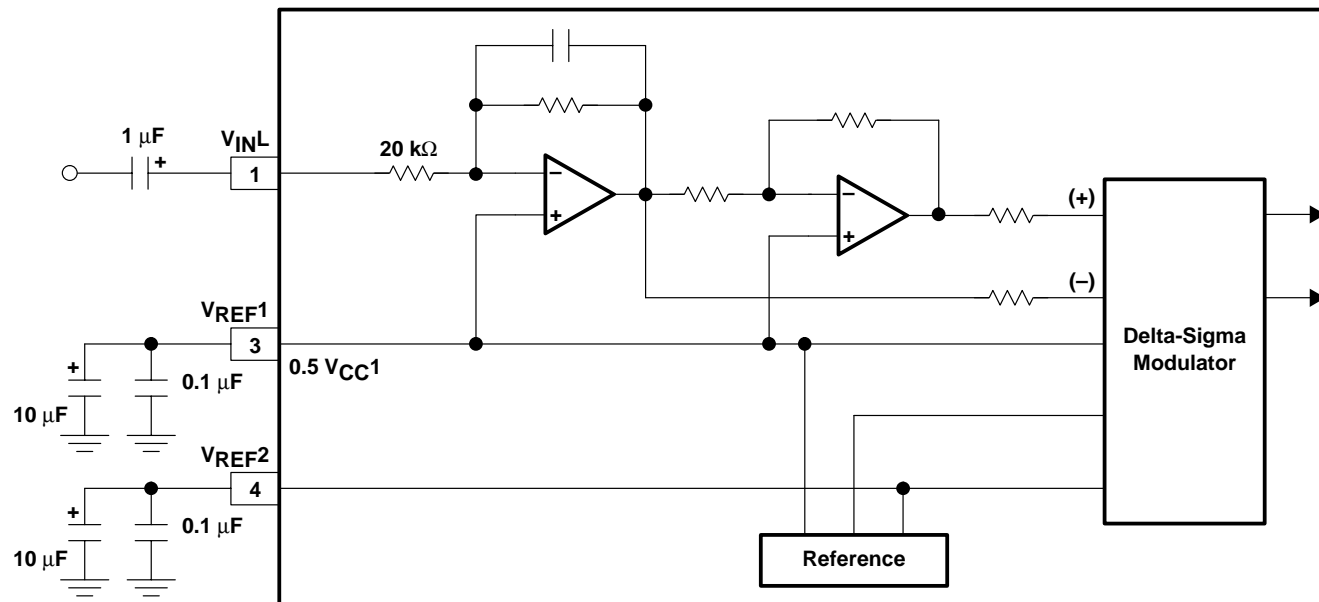


Figure 1. PCM3010 Block Diagram

analog front-end (right-channel)



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTIONS
AGND1	6	–	ADC analog ground
AGND2	20	–	DAC analog ground
BCK	11	I	Audio data bit clock input [‡]
DEMP1	18	I	De-emphasis select input, 1 [†]
DEMP0	19	I	De-emphasis select input, 0 [†]
DGND	14	–	Digital ground
DIN	12	I	Audio data digital input [‡]
DOUT	13	O	Audio data digital output
FMT0	7	I	Audio data format select input, 0 [†]
FMT1	8	I	Audio data format select input, 1 [†]
LRCK	10	I	Audio data latch enable input [‡]
$\overline{\text{PDWN}}$	17	I	ADC and DAC power-down control input, active LOW [†]
SCKI	16	I	System clock input [‡]
TEST	9	I	Test control, must be open or connected to DGND [†]
V _{CC1}	5	–	ADC analog power supply, 5 V
V _{CC2}	21	–	DAC analog power supply, 5 V
V _{COM}	24	–	DAC common voltage decoupling (= 0.5 V _{CC2})
V _{DD}	15	–	Digital power supply, 3.3 V
V _{INL}	1	I	ADC analog input, L-channel
V _{INR}	2	I	ADC analog input, R-channel
V _{OUTL}	23	O	DAC analog output, L-channel
V _{OUTR}	22	O	DAC analog output, R-channel
V _{REF1}	3	–	ADC reference voltage decoupling, 1 (= 0.5 V _{CC1})
V _{REF2}	4	–	ADC reference voltage decoupling, 2

[†] Schmitt-trigger input with 50-k Ω typical internal pulldown resistor, 5-V tolerant.

[‡] Schmitt-trigger input, 5-V tolerant.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{CC1}, V_{CC2}	6.5 V
V_{DD}	4.0 V
Supply voltage differences: V_{CC1}, V_{CC2}	± 0.1 V
Ground voltage differences: AGND1, AGND2, DGND	± 0.1 V
Digital input voltage: PDWN, TEST, FMT0, FMT1, DEMP0, DEMP1, LRCK, BCK, DIN, SCKI	-0.3 V to +6.5 V
Digital input voltage: DOUT	-0.3 V to ($V_{DD} + 0.3$ V)
Analog input voltage, $V_{INL}, V_{INR}, V_{REF1}, V_{REF2}$	-0.3 V to ($V_{CC1} + 0.3$ V)
Analog input voltage, $V_{COM}, V_{OUTL}, V_{OUTR}$	-0.3 V to ($V_{CC2} + 0.3$ V)
Input current (any pins except supplies)	± 10 mA
Ambient temperature under bias	-40°C to 125°C
Storage temperature	-55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5$ V, $V_{DD} = 3.3$ V, $f_S = 44.1$ kHz, SCKI = 384 f_S , 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM3010DB			UNIT
			MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT						
DATA FORMAT						
Audio data interface format			Left-justified, I ² S, right-justified			
Audio data bit length			16, 24			Bits
Audio data format			MSB-first, 2s complement			
f _S	Sampling frequency, ADC		16	44.1	96	kHz
	Sampling frequency, DAC		16	44.1	192	kHz
System clock frequency		128 f _S , 192 f _S , 256 f _S , 384 f _S , 512 f _S , 768 f _S	4		50	MHz
INPUT LOGIC						
V _{IH}	Input logic level (see Notes 1 and 2)		2.0		5.5	VDC
V _{IL}					0.8	VDC
I _{IH}	Input logic current (see Note 2)	V _{IN} = V _{DD}			± 10	μA
I _{IL}		V _{IN} = 0 V			± 10	μA
I _{IH}	Input logic current (see Note 1)	V _{IN} = V _{DD}		65	100	μA
I _{IL}		V _{IN} = 0 V			± 10	μA
OUTPUT LOGIC						
V _{OH}	Output logic level (see Note 3)	I _{OUT} = -4 mA	2.4			VDC
V _{OL}		I _{OUT} = 4 mA			0.4	
ADC CHARACTERISTICS						
Resolution			24			Bits

- NOTES: 1. Pins 7, 8, 9, 17, 18, 19: PDWN, TEST, FMT0, FMT1, DEMP0, DEMP1 (Schmitt-trigger input with 50-k Ω typical internal pulldown resistor, 5-V tolerant).
 2. Pins 10–12, 16: LRCK, BCK, DIN, SCKI (Schmitt-trigger input, 5-V tolerant).
 3. Pin 13: DOUT.

electrical characteristics, all specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $\text{SCKI} = 384 f_S$, 24-bit data (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	PCM3010DB			UNIT
		MIN	TYP	MAX	
ACCURACY					
Gain mismatch, channel-to-channel	1 kHz, full-scale input		± 1	± 6	% of FSR
Gain error	1 kHz, full-scale input		± 2	± 6	% of FSR
DYNAMIC PERFORMANCE (see Note 4)					
THD+N $V_{IN} = -0.5\text{ dB}$	$f_S = 44.1\text{ kHz}$		-95	-86	dB
	$f_S = 96\text{ kHz}$		-92		
THD+N $V_{IN} = -60\text{ dB}$	$f_S = 44.1\text{ kHz}$		-39		dB
	$f_S = 96\text{ kHz}$		-40		
Dynamic range	$f_S = 44.1\text{ kHz}$, A-weighted	97	102		dB
	$f_S = 96\text{ kHz}$, A-weighted		102		
S/N ratio	$f_S = 44.1\text{ kHz}$, A-weighted	95	100		dB
	$f_S = 96\text{ kHz}$, A-weighted		102		
Channel separation	$f_S = 44.1\text{ kHz}$	93	98		dB
	$f_S = 96\text{ kHz}$		100		
ANALOG INPUT					
Input voltage			60% of V_{CC1}		Vp-p
Center voltage			50% of V_{CC1}		V
Input impedance			20		k Ω
Anti-aliasing filter frequency response	-3 dB		300		kHz
DIGITAL FILTER PERFORMANCE					
Pass band			0.454 f_S		Hz
Stop band		0.583 f_S			Hz
Pass-band ripple			± 0.05		dB
Stop-band attenuation		-65			dB
Delay time			17.4/ f_S		sec
HPF frequency response	-3 dB		0.019 f_S		mHz
DAC CHARACTERISTICS					
Resolution			24		Bits
DC ACCURACY					
Gain mismatch, channel-to-channel			± 1.0	± 4.0	% of FSR
Gain error			± 2.0	± 6.0	% of FSR
Bipolar zero error			± 1.0		% of FSR
DYNAMIC PERFORMANCE (see Note 5)					
THD+N, $V_{OUT} = 0\text{ dB}$	$f_S = 44.1\text{ kHz}$		-96	-88	dB
	$f_S = 96\text{ kHz}$		-97		
	$f_S = 192\text{ kHz}$		-97		

NOTES: 4. $f_{IN} = 1\text{ kHz}$, using System Two™ audio measurement system, RMS mode with 20-kHz LPF, 400-Hz HPF in calculation.

5. $f_{OUT} = 1\text{ kHz}$, using System Two audio measurement system, RMS mode with 20-kHz LPF, 400-Hz HPF.

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PCM3010

SLES055 – NOVEMBER 2002

electrical characteristics, all specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $\text{SCKI} = 384 f_S$, 24-bit data (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	PCM3010DB			UNIT	
		MIN	TYP	MAX		
DYNAMIC PERFORMANCE (see Note 5) (Continued)						
THD+N $V_{OUT} = -60\text{ dB}$	$f_S = 44.1\text{ kHz}$		-42		dB	
	$f_S = 96\text{ kHz}$		-43			
	$f_S = 192\text{ kHz}$		-43			
Dynamic range	$f_S = 44.1\text{ kHz}$, EIAJ, A-weighted	98	104		dB	
	$f_S = 96\text{ kHz}$, EIAJ, A-weighted		105			
	$f_S = 192\text{ kHz}$, EIAJ, A-weighted		105			
S/N ratio	$f_S = 44.1\text{ kHz}$, EIAJ, A-weighted	98	104		dB	
	$f_S = 96\text{ kHz}$, EIAJ, A-weighted		105			
	$f_S = 192\text{ kHz}$, EIAJ, A-weighted		105			
Channel separation	$f_S = 44.1\text{ kHz}$	95	102		dB	
	$f_S = 96\text{ kHz}$		102			
	$f_S = 192\text{ kHz}$		103			
ANALOG OUTPUT						
Output voltage			60% of V_{CC2}		Vp-p	
Center voltage			50% of V_{CC2}		V	
Load impedance	AC coupling	5			k Ω	
LPF frequency response	$f = 20\text{ kHz}$		-0.03		dB	
	$f = 44\text{ kHz}$		-0.20			
DIGITAL FILTER PERFORMANCE						
Pass band	$\pm 0.03\text{ dB}$			$0.454 f_S$	Hz	
Stop band				$0.546 f_S$	Hz	
Pass-band ripple				± 0.03	dB	
Stop-band attenuation	$0.546 f_S$	-50			dB	
Delay time				$20/f_S$	sec	
De-emphasis error				± 0.1	dB	
POWER SUPPLY REQUIREMENTS						
V_{CC1} V_{CC2}	Voltage range		4.5	5.0	5.5	VDC
V_{DD}			3.0	3.3	3.6	
I_{CC} ($I_{CC1} + I_{CC2}$)	Supply current	$f_S = 44.1\text{ kHz}$		31	40	mA
		$f_S = 96\text{ kHz}$		32		
		$f_S = 192\text{ kHz}$		9		
I_{DD}		$f_S = 44.1\text{ kHz}$		10	15	mA
		$f_S = 96\text{ kHz}$		20		
		$f_S = 192\text{ kHz}$		14		
Power dissipation, operation		$f_S = 44.1\text{ kHz}$		190	250	mW
		$f_S = 96\text{ kHz}$		230		
		$f_S = 192\text{ kHz}$		90		
Power dissipation, power down (see Note 6)				1	mW	
TEMPERATURE RANGE						
Operating temperature			-25		85	$^\circ\text{C}$
θ_{JA}	Thermal resistance	24-pin SSOP		100		$^\circ\text{C/W}$

NOTES: 5. $f_{OUT} = 1\text{ kHz}$, using System Two audio measurement system, RMS mode with 20-kHz LPF, 400-Hz HPF.

6. Halt SCKI, BCK, LRCK.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (ADC PORTION)

digital filter

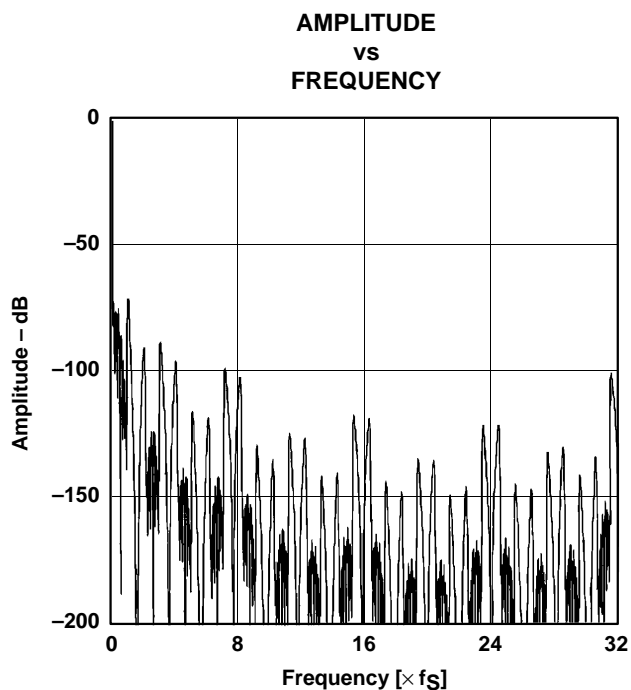


Figure 2. Overall Characteristics

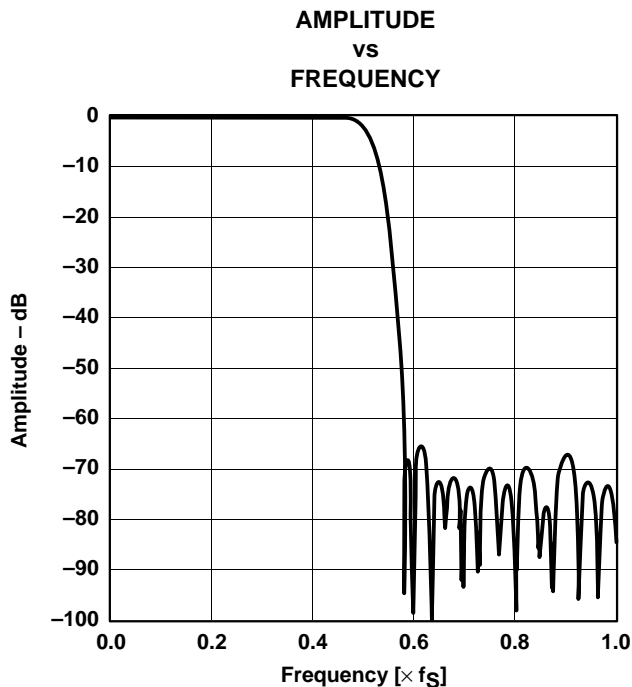


Figure 3. Stop-Band Attenuation Characteristics

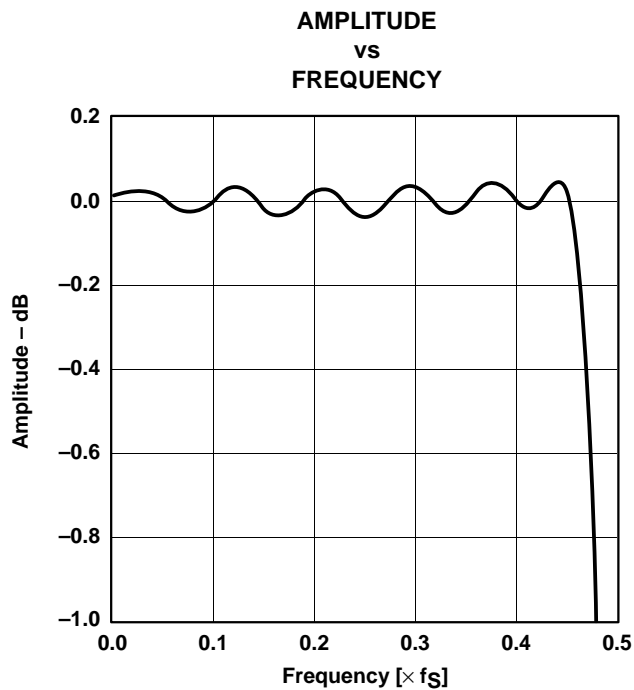


Figure 4. Pass-Band Ripple Characteristics

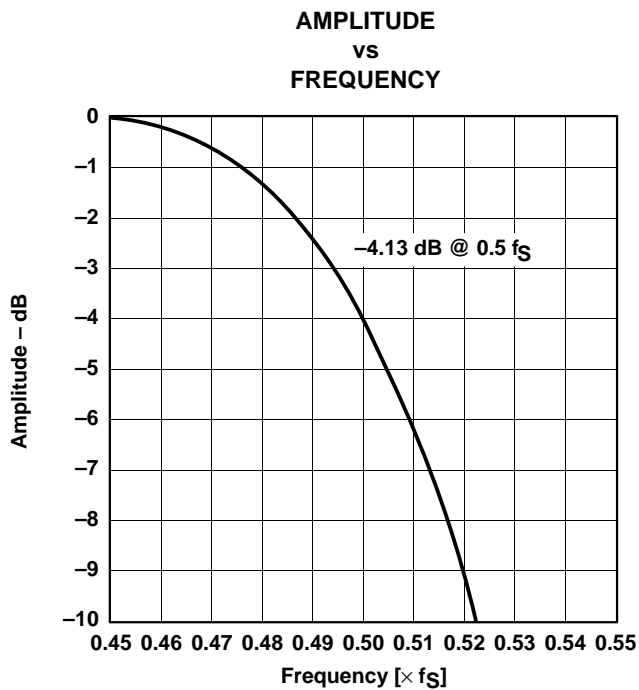


Figure 5. Transient Band Characteristics

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $SCK1 = 384 f_S$, 24-bit data, unless otherwise noted.

digital filter (continued)

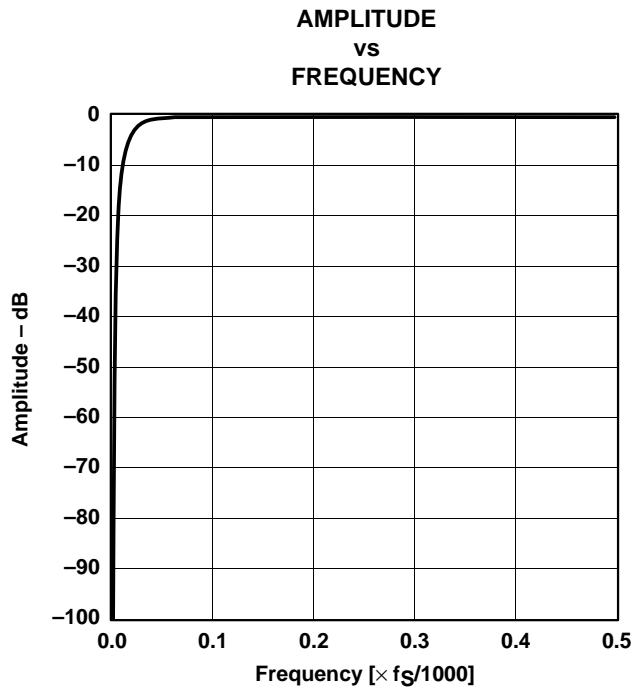


Figure 6. Low-Cut HPF Stop-Band Characteristics

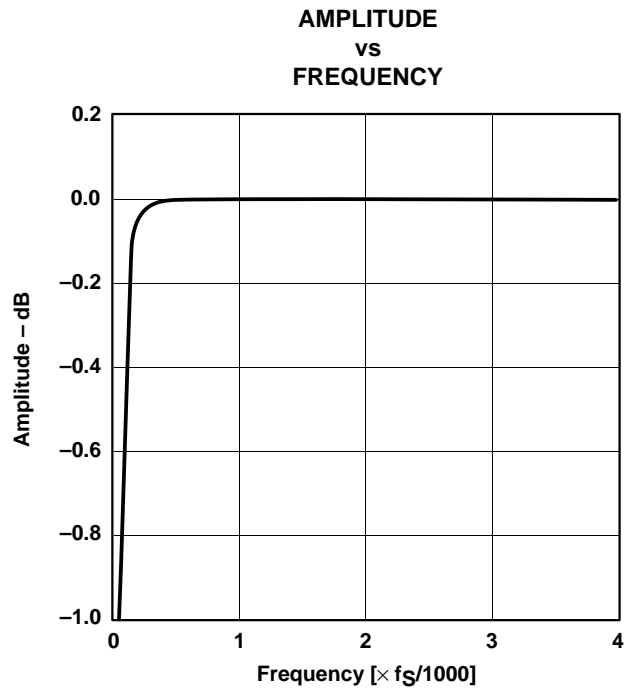


Figure 7. Low-Cut HPF Pass-Band Characteristics

analog filter

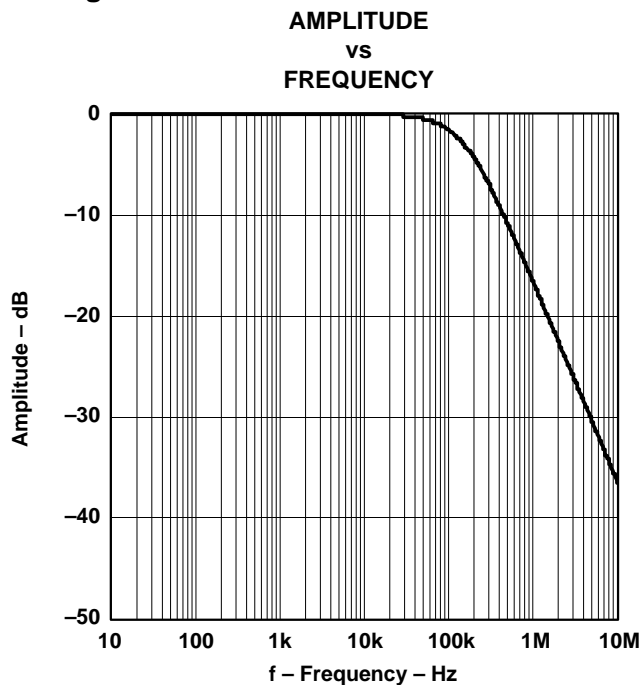


Figure 8. Antialiasing Filter Stop-Band Characteristics

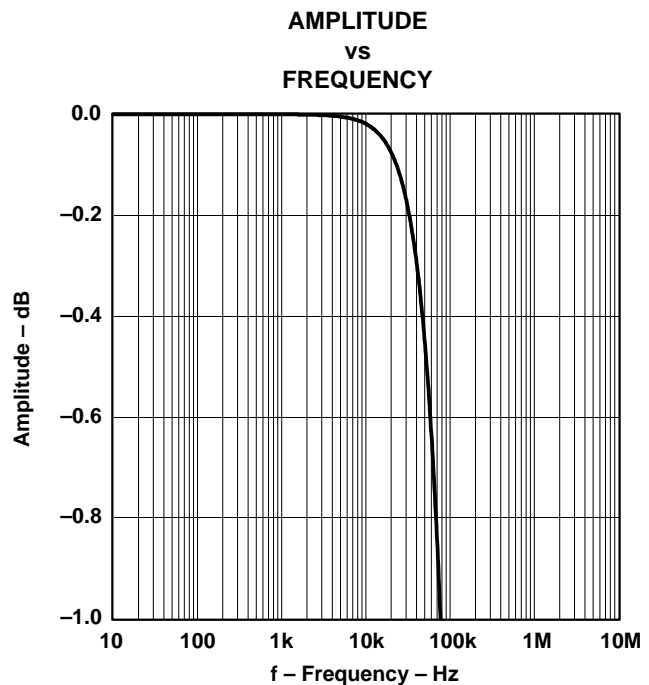


Figure 9. Antialiasing Filter Pass-Band Characteristics

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $SCKI = 384 f_S$, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (DAC PORTION)

digital filter

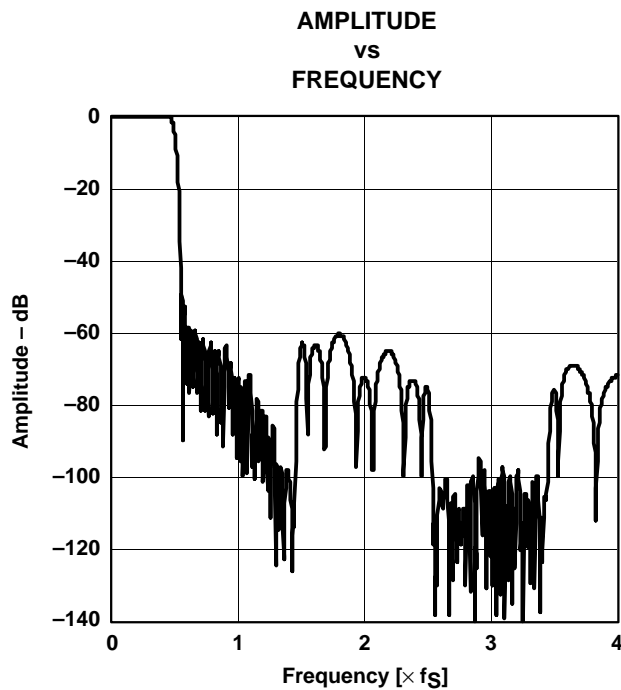


Figure 10. Frequency Response (Sharp Rolloff)

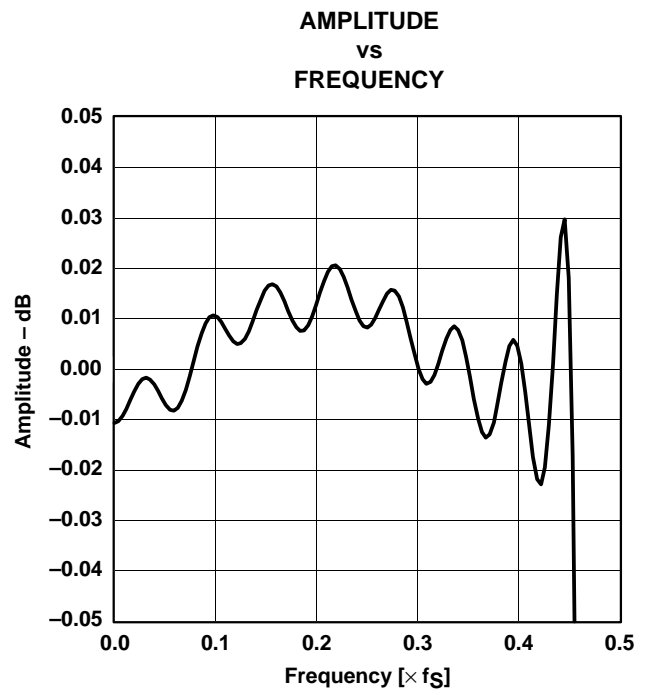


Figure 11. Frequency Response, Pass-Band (Sharp Rolloff)

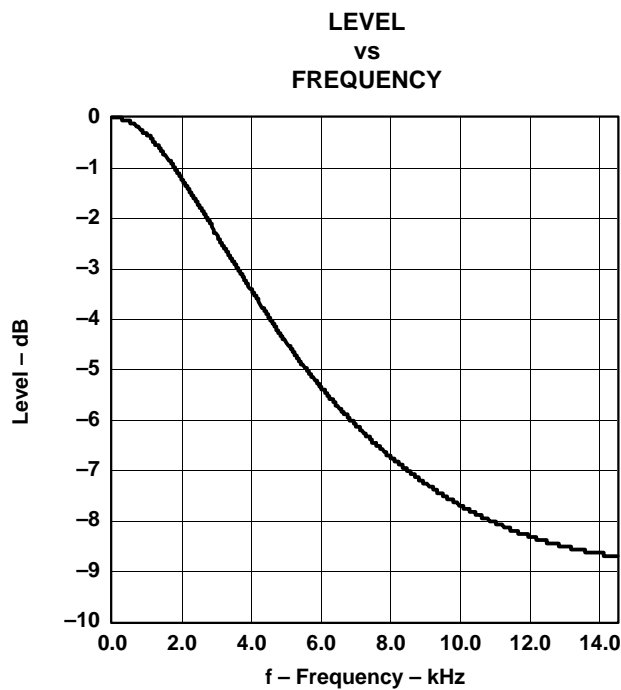


Figure 12. De-Emphasis ($f_S = 32$ kHz)

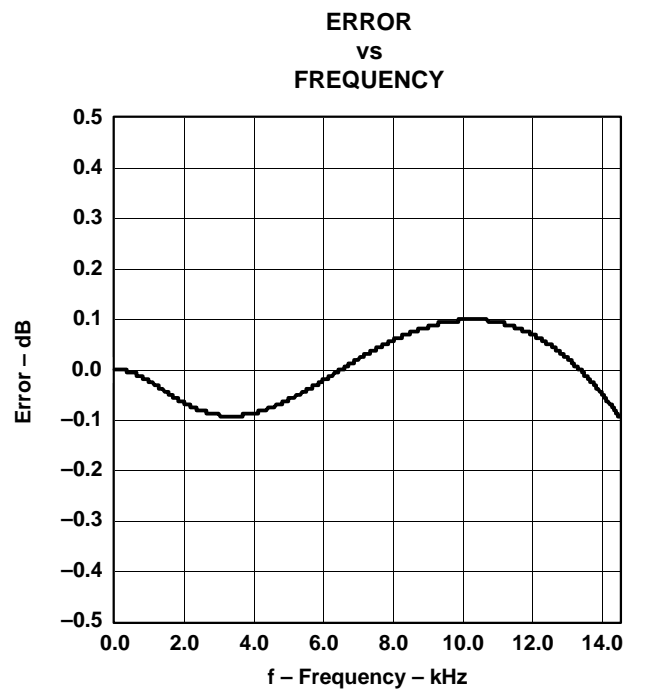


Figure 13. De-Emphasis Error ($f_S = 32$ kHz)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5$ V, $V_{DD} = 3.3$ V, $f_S = 44.1$ kHz, $SCK1 = 384 f_S$, 24-bit data, unless otherwise noted.

digital filter (continued)

LEVEL
vs
FREQUENCY

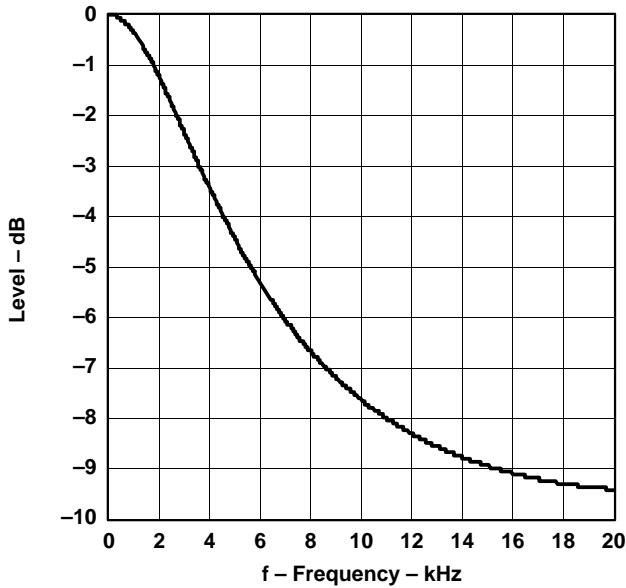


Figure 14. De-Emphasis ($f_S = 44.1$ kHz)

ERROR
vs
FREQUENCY

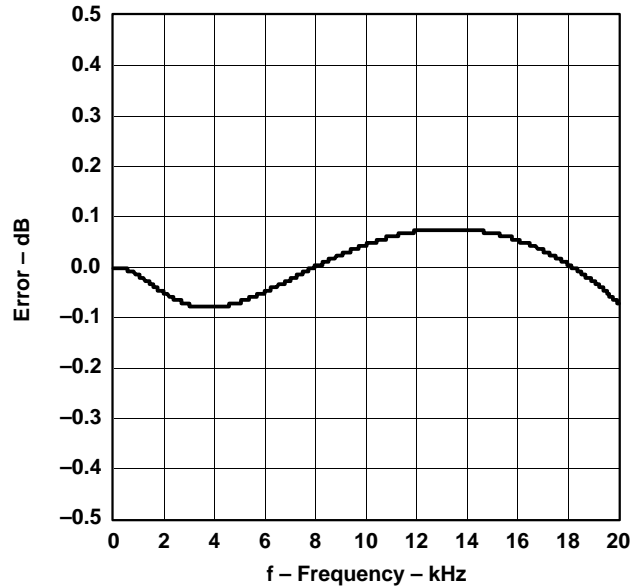


Figure 15. De-Emphasis Error ($f_S = 44.1$ kHz)

LEVEL
vs
FREQUENCY

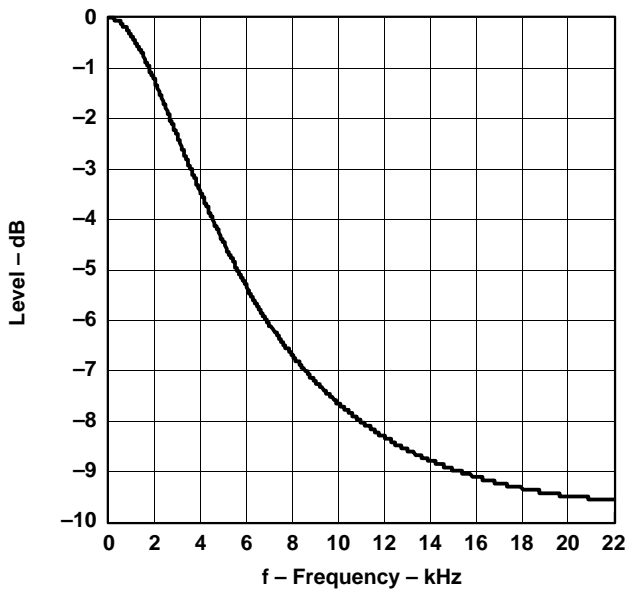


Figure 16. De-Emphasis ($f_S = 48$ kHz)

ERROR
vs
FREQUENCY

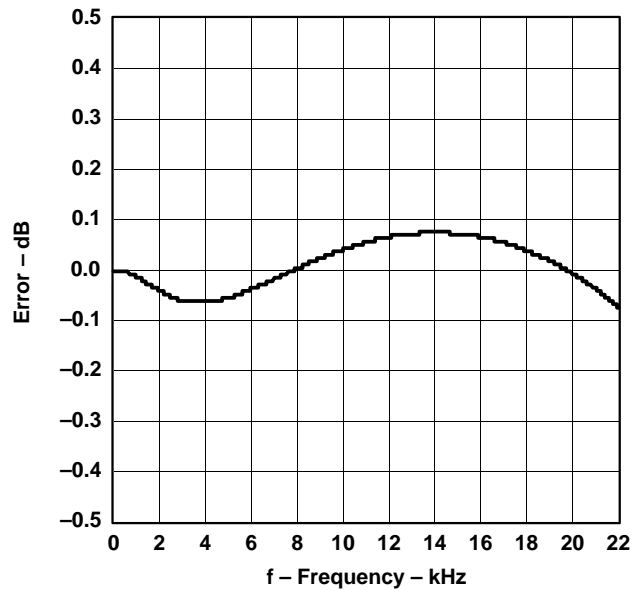


Figure 17. De-Emphasis Error ($f_S = 48$ kHz)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5$ V, $V_{DD} = 3.3$ V, $f_S = 44.1$ kHz, $SCKI = 384 f_S$, 24-bit data, unless otherwise noted.

analog filter

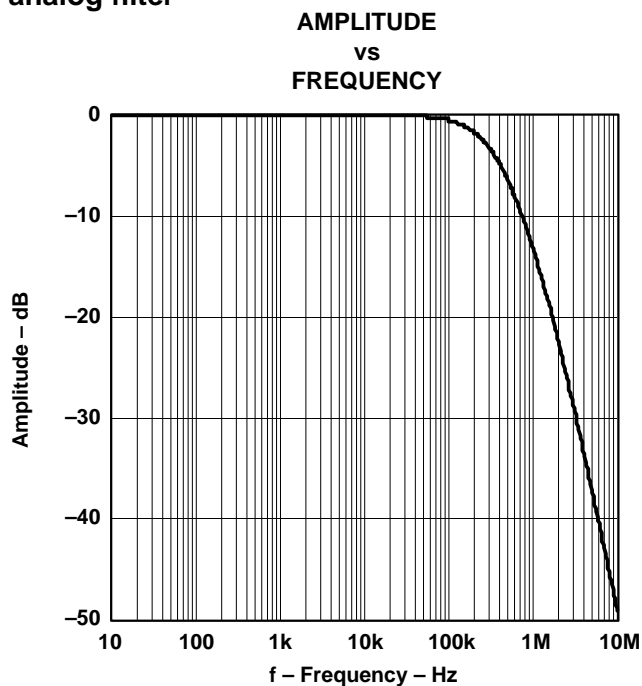


Figure 18. Analog Filter Stop-Band Performance (10 Hz–10 MHz)

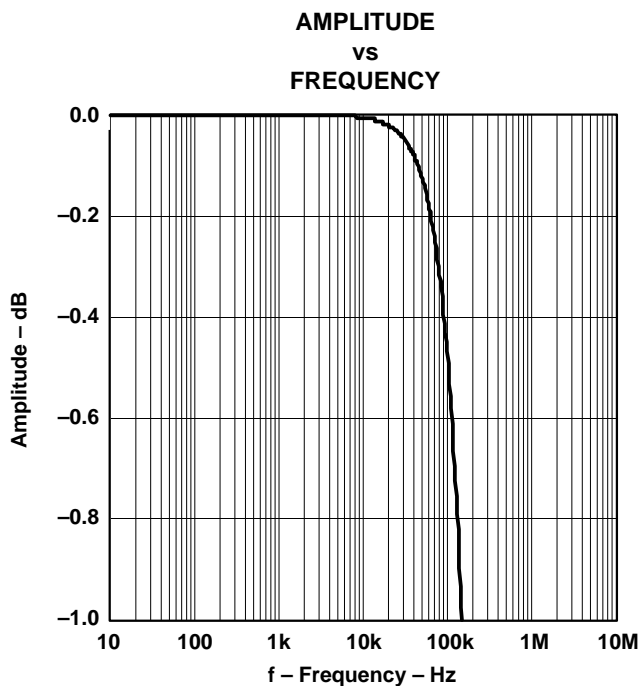


Figure 19. Analog Filter Pass-Band Performance (10 Hz–10 MHz)

TYPICAL PERFORMANCE CURVES (ADC PORTION)

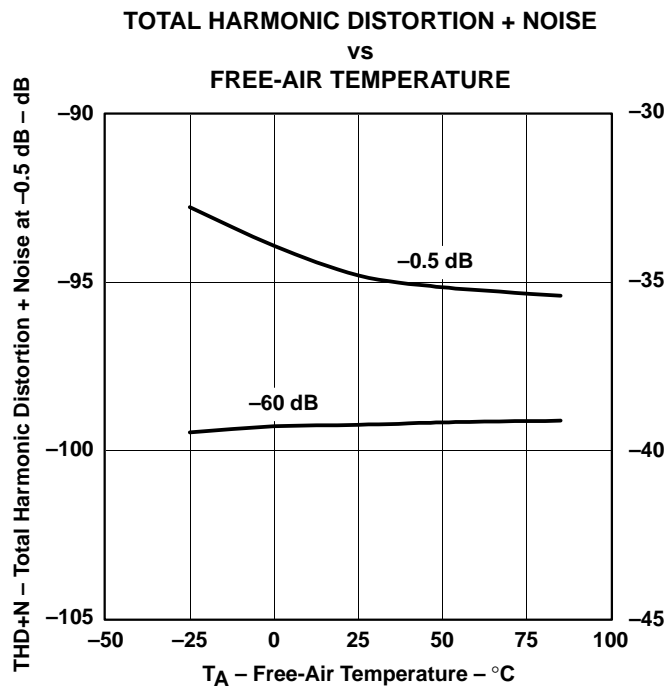


Figure 20

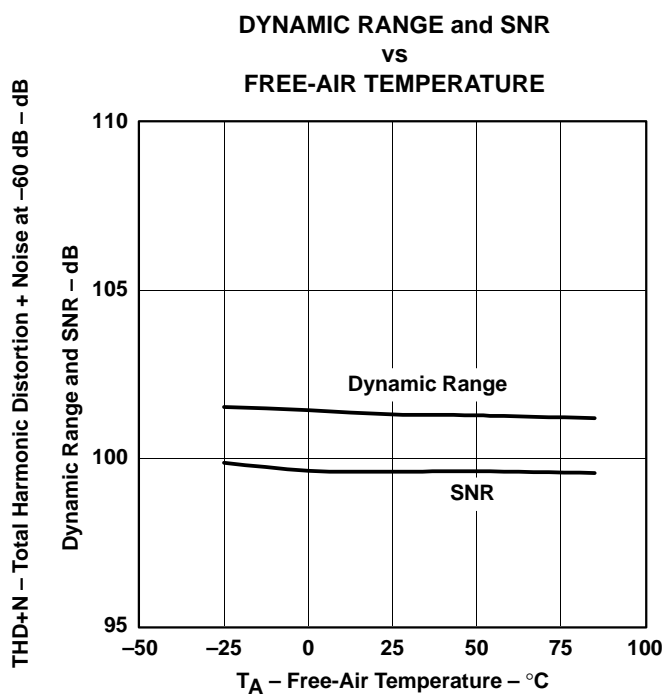


Figure 21

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $SCK1 = 384 f_S$, 24-bit data, unless otherwise noted.

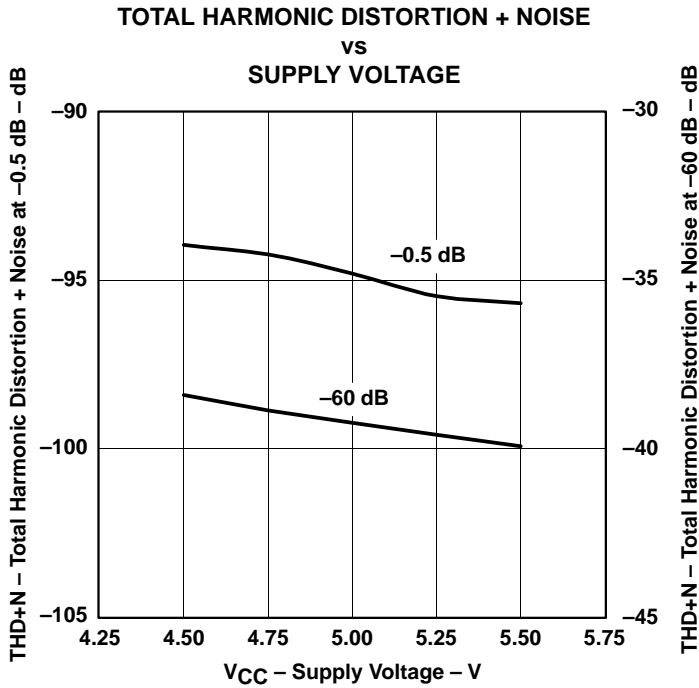


Figure 22

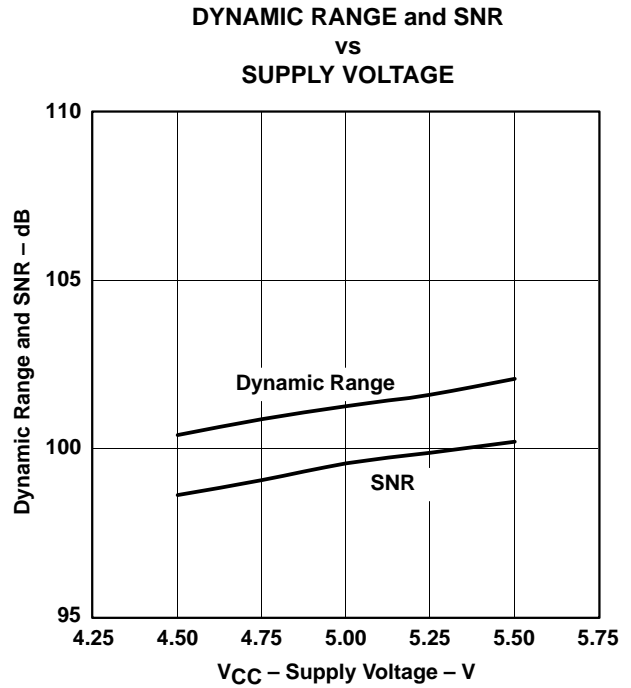


Figure 23

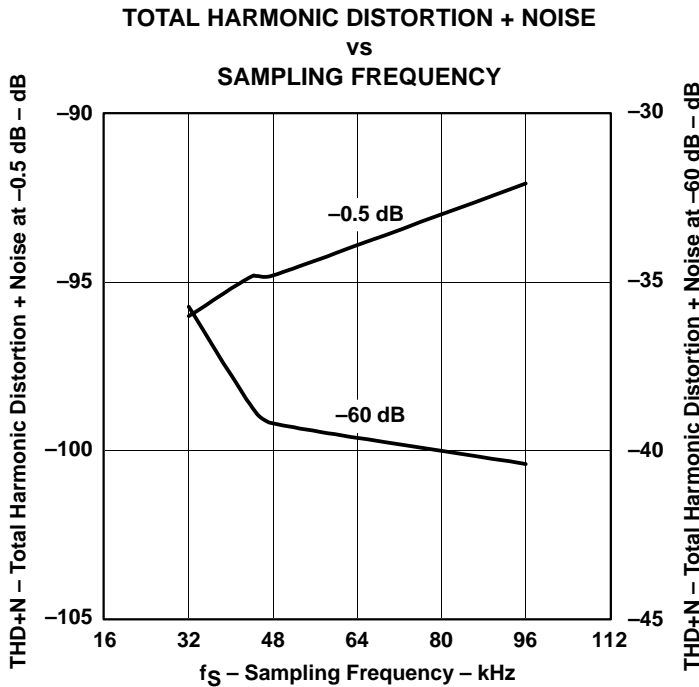


Figure 24

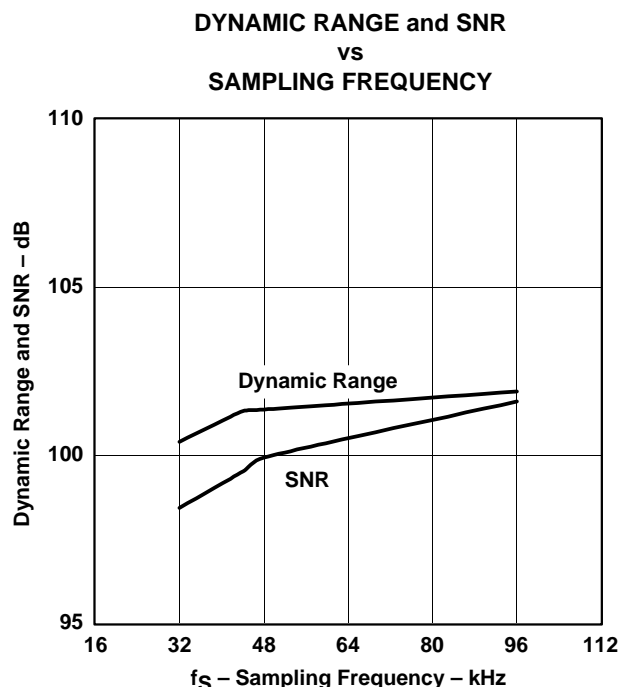
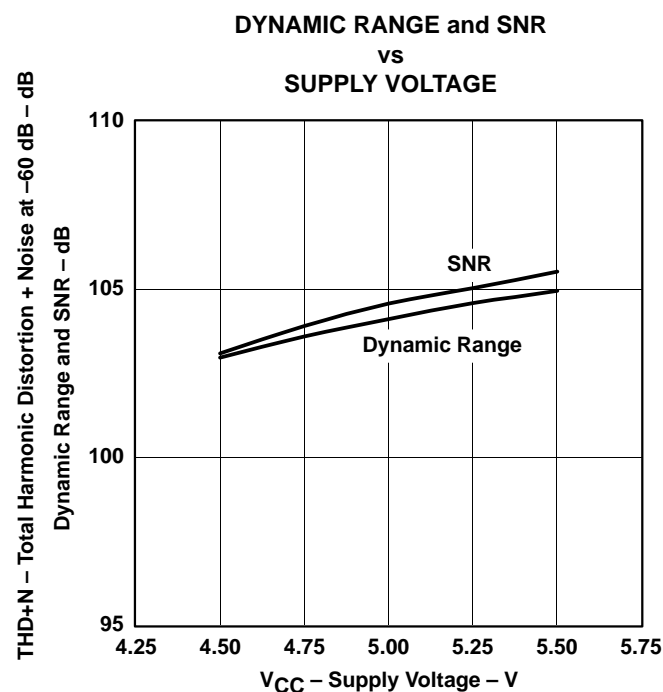
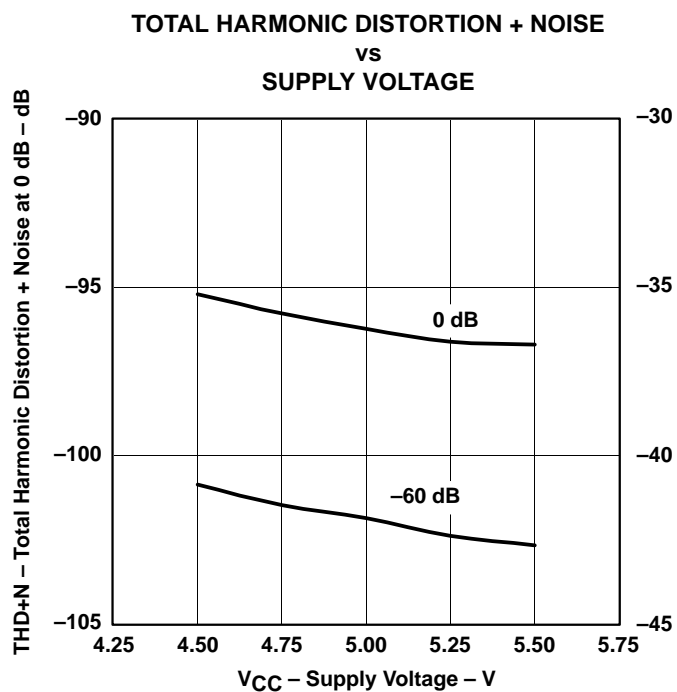
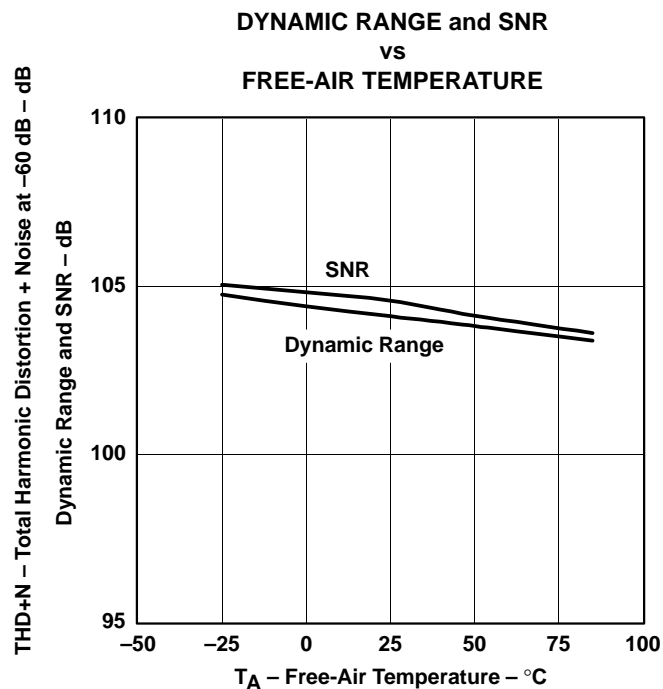
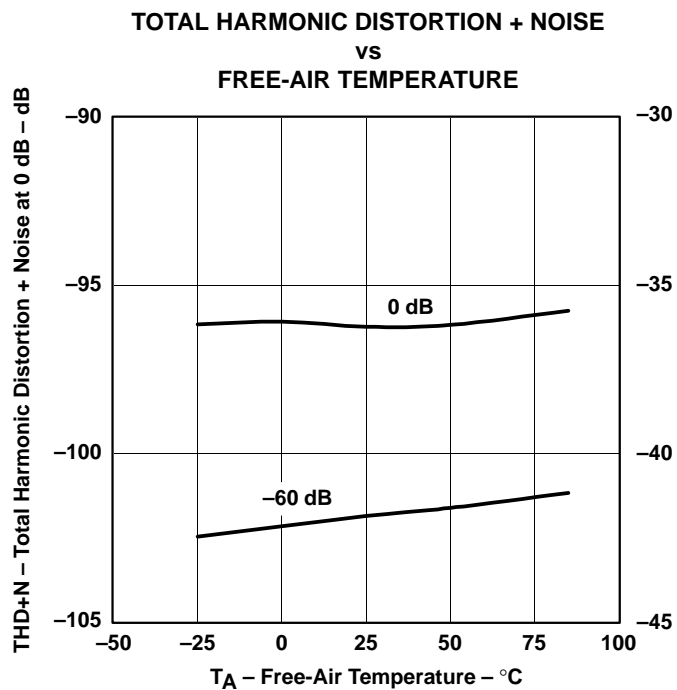


Figure 25

All specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, SCKI = 384 f_S, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES (DAC PORTION)



All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $SCKI = 384 f_S$, 24-bit data, unless otherwise noted.

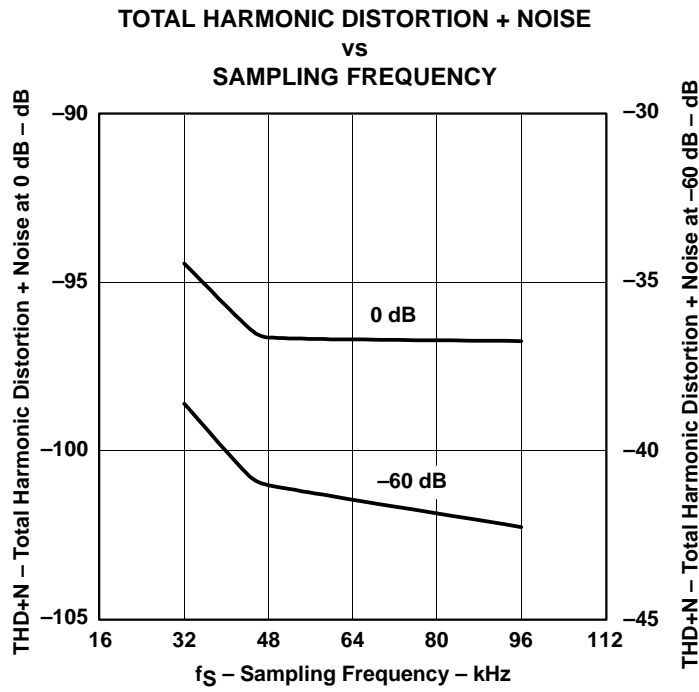


Figure 30

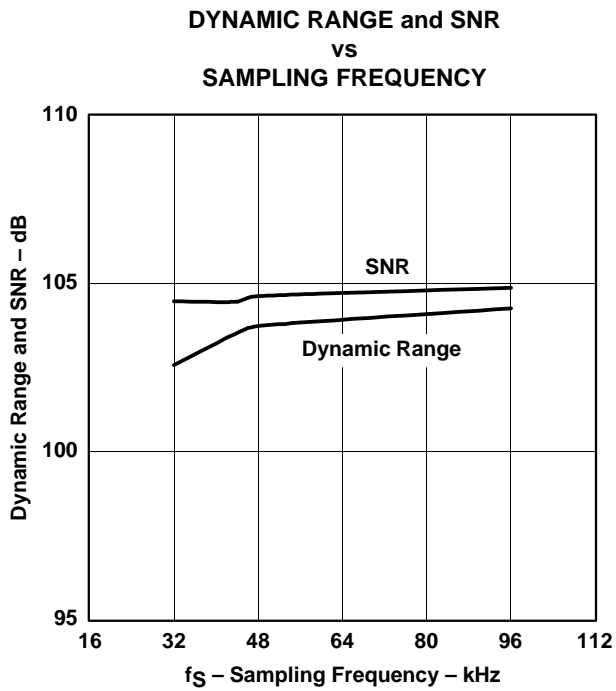


Figure 31

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $SCKI = 384\text{ fS}$, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES

ADC output spectrum

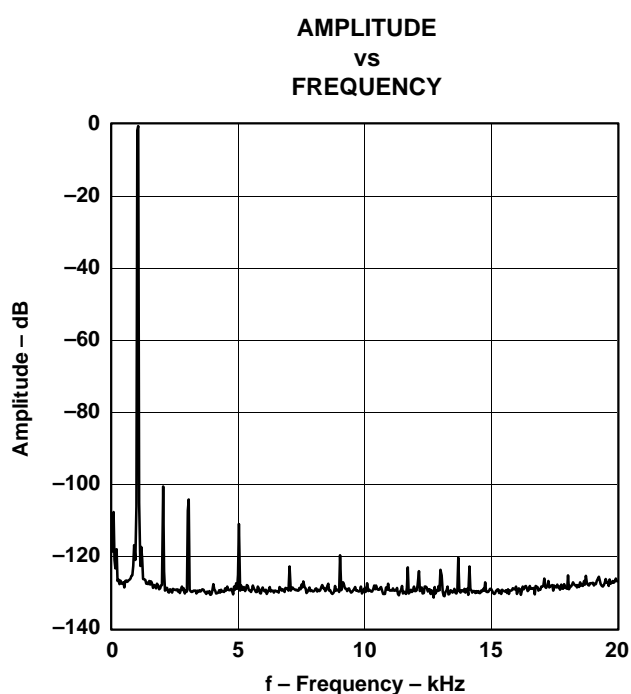


Figure 32. Output Spectrum (-0.5 dB, N = 8192)

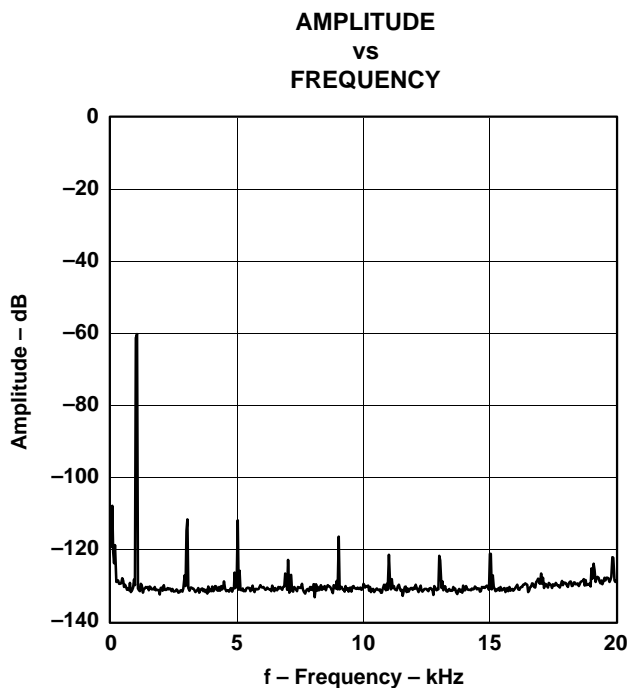


Figure 33. Output Spectrum (-60 dB, N = 8192)

DAC output spectrum

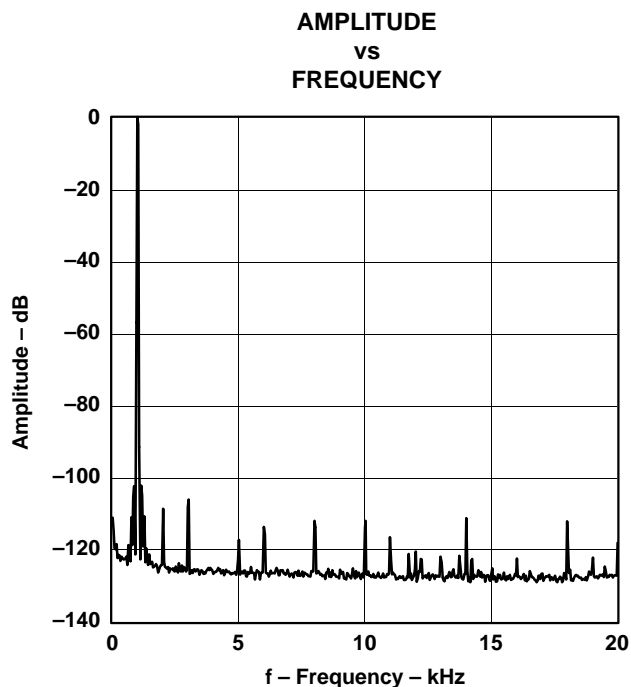


Figure 34. Output Spectrum (0 dB, N = 8192)

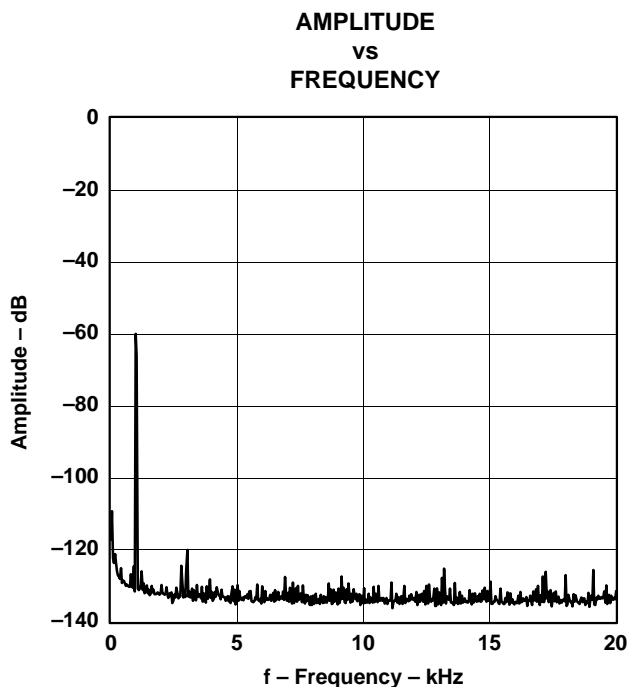


Figure 35. Output Spectrum (-60 dB, N = 8192)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $\text{SCKI} = 384 f_S$, 24-bit data, unless otherwise noted.

supply current

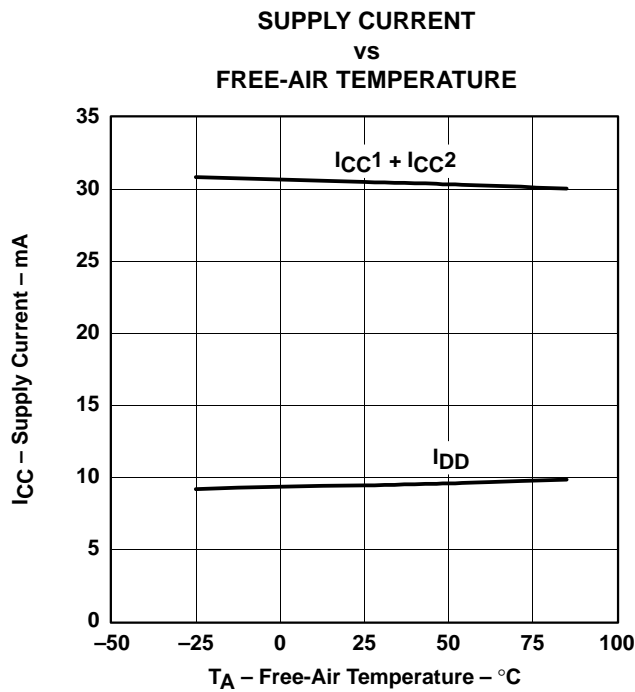


Figure 36

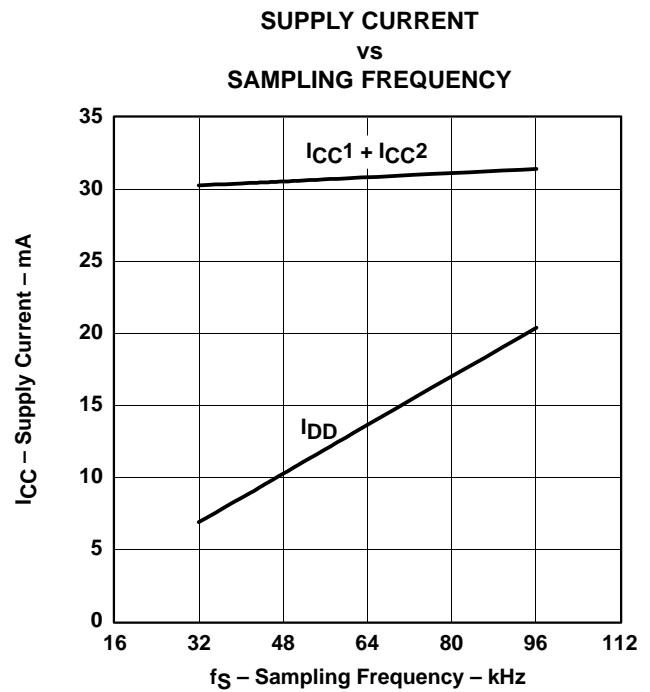


Figure 37. Supply Current vs Sampling Frequency, ADC and DAC Operating

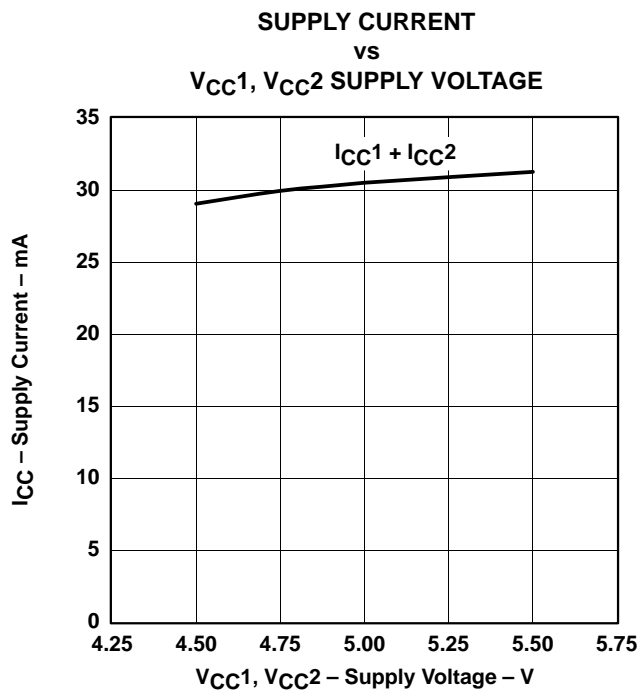


Figure 38

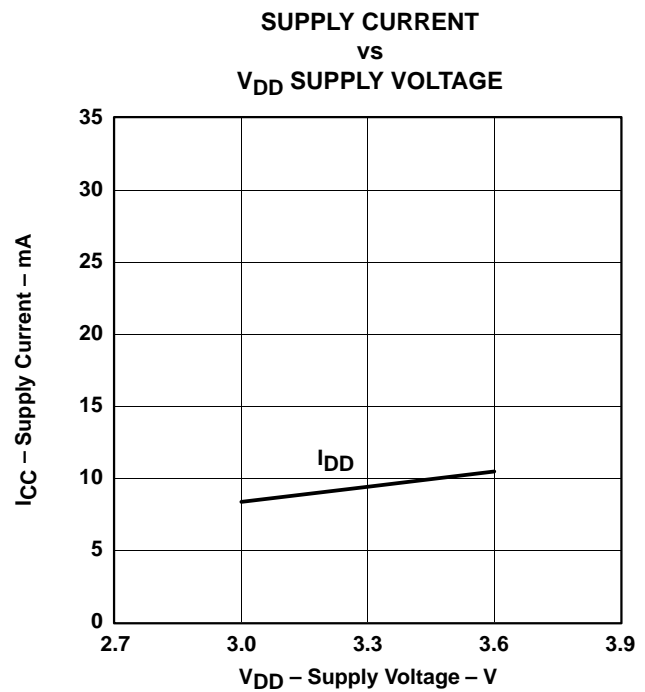


Figure 39

All specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, SCKI = 384 f_S, 24-bit data, unless otherwise noted.

THEORY OF OPERATION

ADC portion

The ADC block consists of a reference circuit, two single-ended to differential converter channels, a fifth-order delta-sigma modulator with full-differential architecture, a decimation filter with low-cut filter, and a serial interface circuit which is also used as a serial interface for the DAC input signal as shown in the block diagram, Figure 1.

The analog front-end diagram illustrates the architecture of the single-ended to differential converter and antialiasing filter. Figure 40 illustrates the block diagram of the fifth-order delta-sigma modulator and transfer function.

An on-chip reference circuit with two external capacitors provides all the reference voltages which are needed in the ADC portion, and defines the full-scale voltage range of both channels.

An on-chip single-ended to differential signal converter saves the design, space, and extra parts cost of an external signal converter.

Full-differential architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at a $\times 64$ oversampling rate, and an on-chip antialiasing filter eliminates the external sample-hold amplifier. A fifth-order delta-sigma noise shaper, which consists of five integrators using a switched capacitor technique followed by a comparator, shapes the quantization noise generated by the comparator and 1-bit DAC outside the audio signal band.

The high order delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level.

The $64\text{-}f_S$, 1-bit stream from the delta-sigma modulator is converted to a $1\text{-}f_S$, 24-bit or 16-bit digital signal by removing the high-frequency noise components with a decimation filter.

The dc component of the signal is removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats.

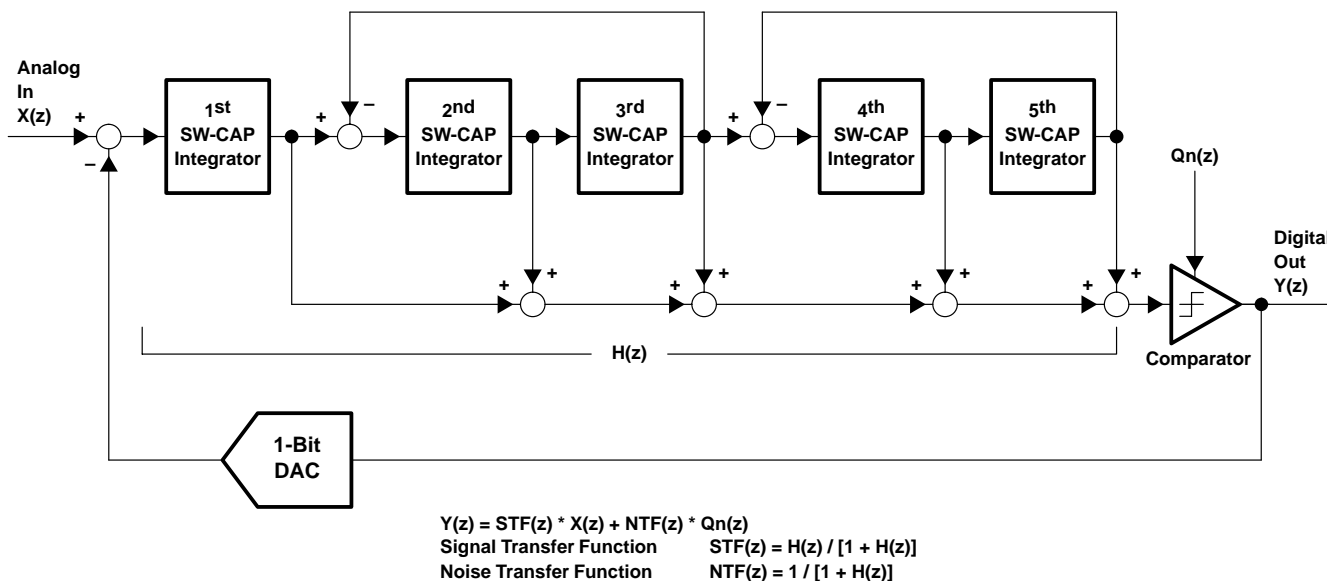


Figure 40. Block Diagram of Fifth-Order Delta-Sigma Modulator

DAC portion

The DAC portion is based on the delta-sigma modulator, which consists of an 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to the 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 41. This 8-level delta-sigma modulator has the advantage of improved stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8x interpolation filter is 64 f_S for all system clocks. The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 42.

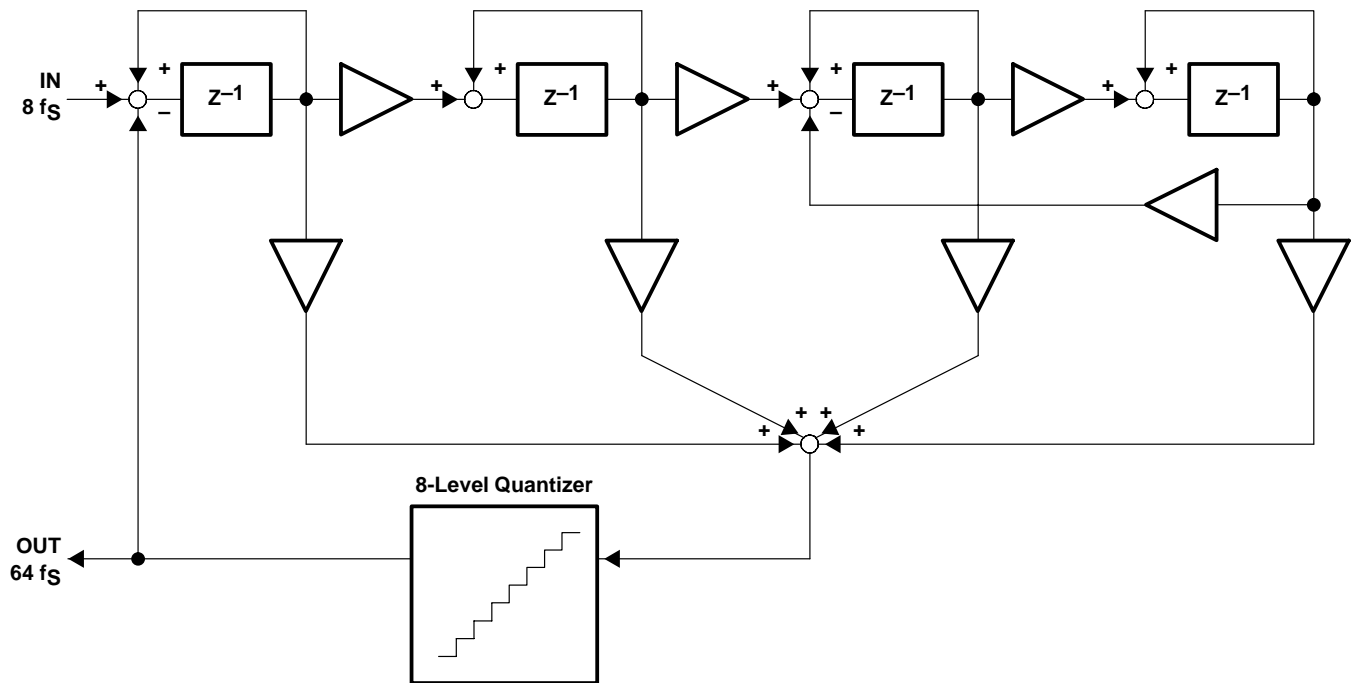


Figure 41. 8-Level Delta-Sigma Modulator Block Diagram

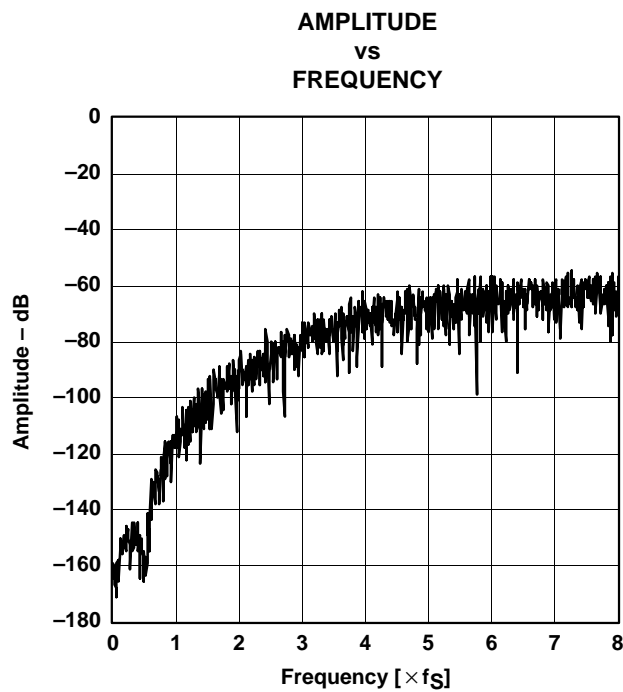


Figure 42. Quantization Noise Spectrum
($\times 64$ Oversampling)

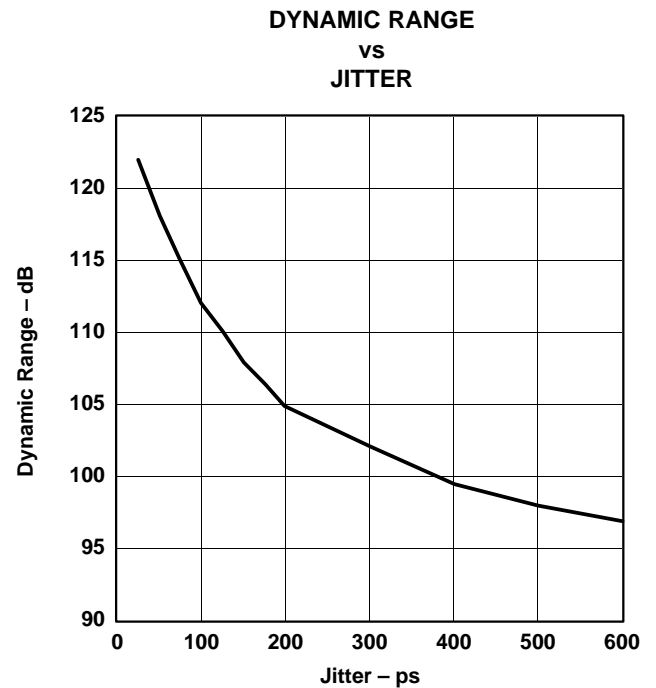


Figure 43. Jitter Dependence
($\times 64$ Oversampling)

system clock

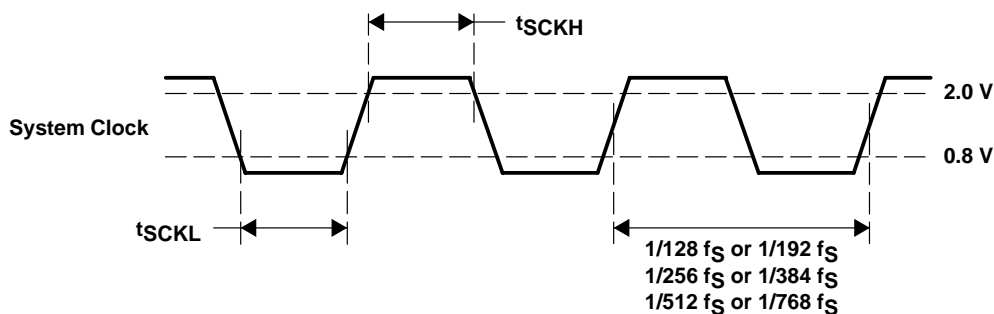
The system clock for the PCM3010 must be $128 f_S$, $192 f_S$, $256 f_S$, $384 f_S$, $512 f_S$ or $768 f_S$, where f_S is the audio sampling rate, 16 kHz to 192 kHz. The PCM3010 detects $128 f_S$, $192 f_S$, $256 f_S$, $384 f_S$, $512 f_S$ or $768 f_S$ automatically with the built-in circuit. Operation at the 192-kHz sampling rate is available on the DAC only, and when a system clock of $128 f_S$ or $192 f_S$ is detected, the ADC is disabled (DOOUT = LOW). Table 1 lists the typical system clock frequency, and Figure 44 illustrates the system clock timing.

Table 1. Typical System Clock

SAMPLING RATE FREQUENCY (f_S) – LRCK	SYSTEM CLOCK FREQUENCY – MHz					
	$128 f_S$	$192 f_S$	$256 f_S$	$384 f_S$	$512 f_S$	$768 f_S$
32 kHz	–	–	8.192	12.288	16.384	24.576
44.1 kHz	–	–	11.2896	16.9344	22.5792	33.8688
48 kHz	–	–	12.288	18.432	24.576	36.864
96 kHz	–	–	24.576	36.864	49.152	–
192 kHz	24.576†	36.864†	–	–	–	–

† DAC only.

system clock (continued)



PARAMETER		MIN	MAX	UNIT
t_{SCKH}	System clock pulse duration HIGH	8		ns
t_{SCKL}	System clock pulse duration LOW	8		ns

Figure 44. System Clock Timing

power supply on, external reset, and power down

The PCM3010 has both an internal power-on reset circuit and an external reset circuit. The sequences for both resets are explained as follows.

Figure 45 is the timing diagram for the internal power-on reset. Two power-on reset circuits are implemented for V_{CC1} and V_{DD} , respectively. Initialization (reset) occurs automatically when V_{CC1} and V_{DD} exceed 4.0 V and 2.2 V, typically.

Internal reset is released 1024 SCKI clock cycles following the release from power-on reset, and the PCM3010 begins normal operation. V_{OUTL} and V_{OUTR} from the DAC are forced to the V_{COM} ($= 0.5 V_{CC2}$) level as V_{CC2} rises. When synchronization between SCKI, BCK and LRCK is obtained while V_{OUTL} and V_{OUTR} go into the fade sequence and provide outputs corresponding to DIN after $t_{DACDLY1} = 2100/f_S$ following release from power-on reset. On the other hand, DOUT from the ADC provides an output corresponding to V_{INL} and V_{INR} after $t_{ADC DLY1} = 4500/f_S$ following release from power-on reset. If the synchronization is not held, the internal reset is not released and device operation remains in the power-down mode. After resynchronization, the DAC performs the fade-in sequence and the ADC resumes normal operation following internal initialization.

Figure 46 is the external-reset timing diagram. External forced reset, driving the \overline{PDWN} pin LOW, puts the PCM3010 in the power-down mode, which is its lowest power-dissipation state.

When \overline{PDWN} transitions from HIGH to LOW while synchronization is maintained between SCKI, BCK, and LRCK, then V_{OUTL} and V_{OUTR} are faded out and forced to the V_{COM} ($= 0.5 V_{CC2}$) level after $t_{DACDLY1} = 2100/f_S$. At the same time as the internal reset becomes LOW, DOUT becomes ZERO, the PCM3010 enters into power-down mode. To enter into normal operation mode again, change \overline{PDWN} to HIGH again. The reset sequence shown in Figure 45 occurs.

Notes:

1. A large popping noise may be generated on V_{OUTL} and V_{OUTR} when the power supply is turned off during normal operation.
2. To switch \overline{PDWN} during fade in or fade out causes an immediate change between fade in and fade out.
3. To switch the control pins on the fly during normal operation can degrade analog performance. It is recommended that changing control pins, changing clocks, stopping clocks, turning power supplies off, etc., be done in the power-down mode.

power supply on, external reset and power down (continued)

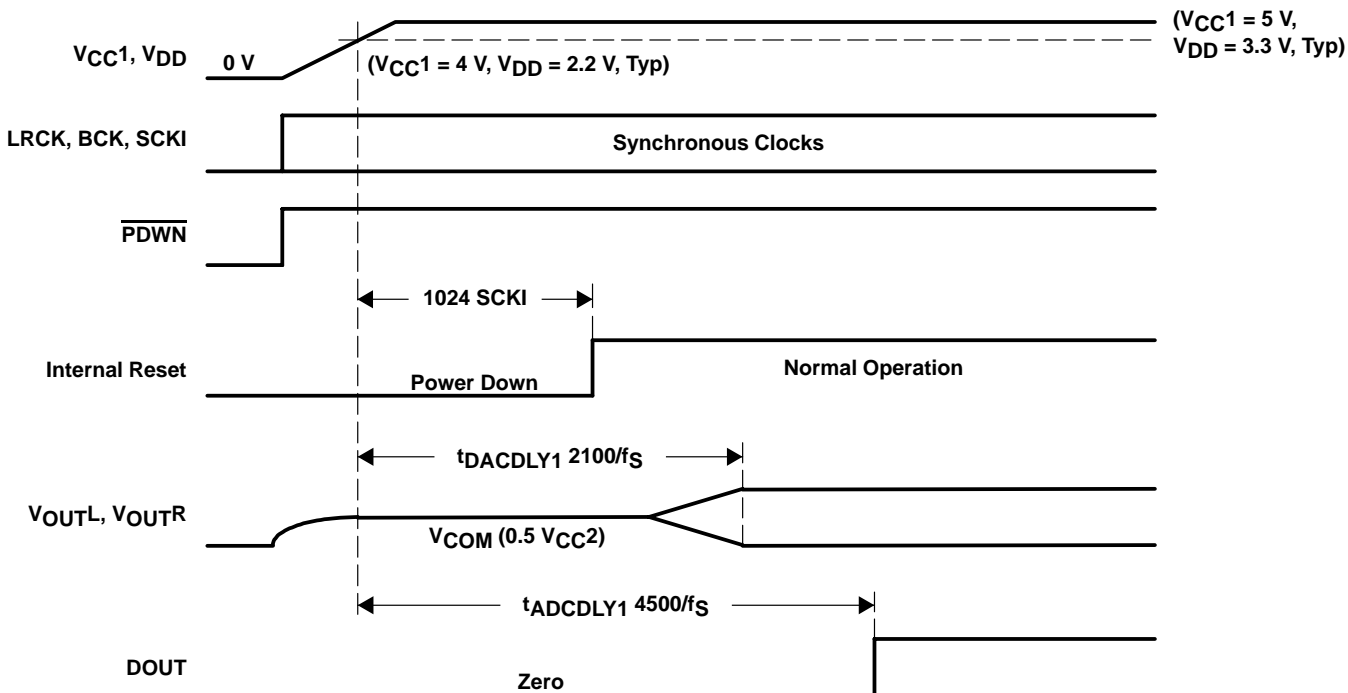


Figure 45. DAC Output and ADC Output for Power-On Reset

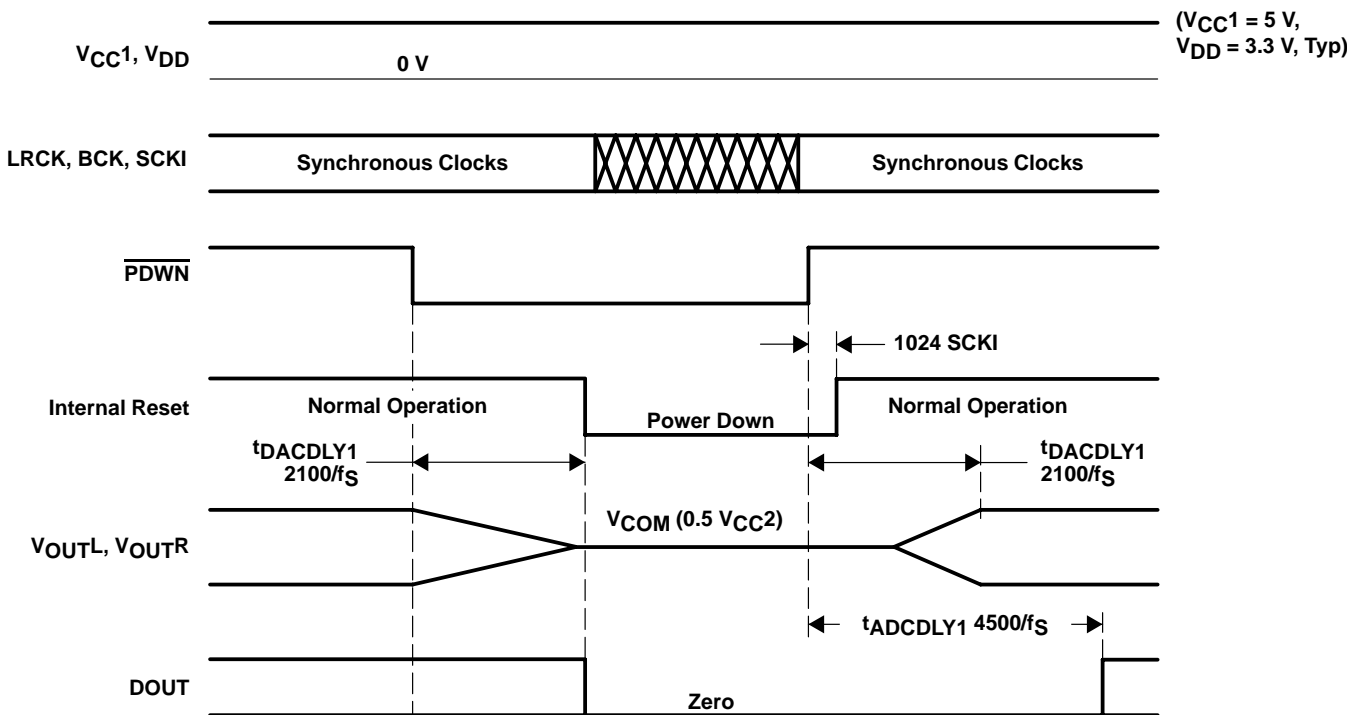


Figure 46. DAC Output and ADC Output for External Reset (\overline{PDWN} Pin)

PCM audio interface

Digital audio data is interfaced to the PCM3010 on LRCK (pin 10), BCK (pin 11), DIN (pin 12), and DOUT (pin 13). The PCM3010 can accept the following 16-bit and 24-bit formats. These formats are selected through FMT0 (pin 7) and FMT1 (pin 8), as shown in Table 2.

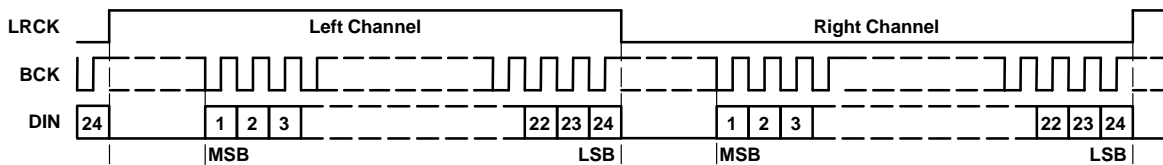
Table 2. Audio Data Format Select

FMT1	FMT0	DAC DATA FORMAT	ADC DATA FORMAT
LOW	LOW	24-bit, MSB-first, right-justified	24-bit, MSB-first, left-justified
LOW	HIGH	16-bit, MSB-first, right-justified	24-bit, MSB-first, left-justified
HIGH	LOW	24-bit, MSB-first, left-justified	24-bit, MSB-first, left-justified
HIGH	HIGH	24-bit, MSB-first, I ² S	24-bit, MSB-first, I ² S

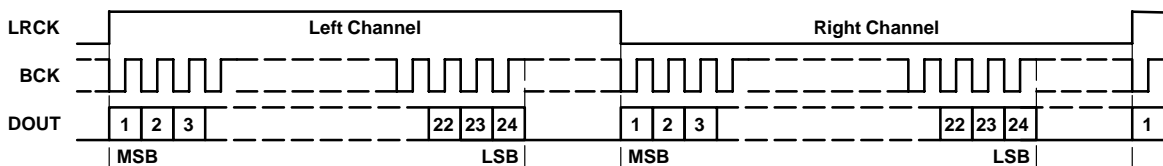
The PCM3010 accepts two combinations of BCK and LRCK, 64 or 48 clocks of BCK in one clock of LRCK. The following figures illustrate audio data input/output format and timing.

FORMAT 0: FMT[1:0] = 00

DAC: 24-Bit, MSB-First, Right-Justified

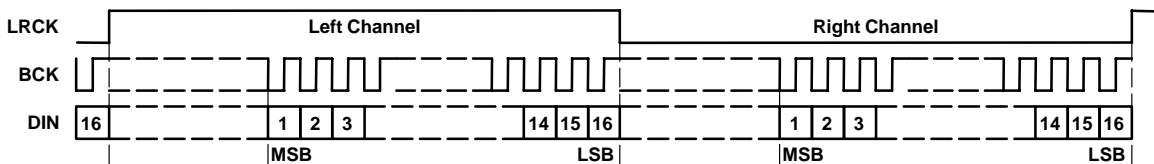


ADC: 24-Bit, MSB-First, Left-Justified



FORMAT 1: FMT[1:0] = 01

DAC: 16-Bit, MSB-First, Right-Justified



ADC: 24-Bit, MSB-First, Left-Justified

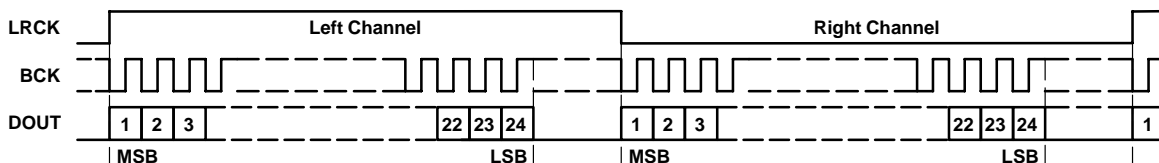
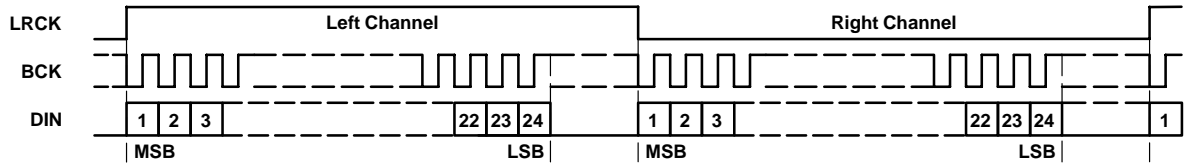


Figure 47. Audio Data Input/Output Format

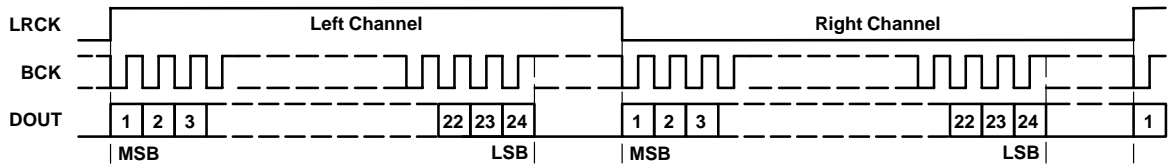
PCM audio interface (continued)

FORMAT 2: FMT[1:0] = 10

DAC: 24-Bit, MSB-First, Left-Justified

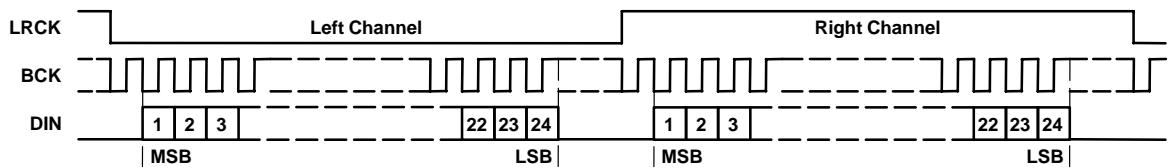


ADC: 24-Bit, MSB-First, Left-Justified



FORMAT 3: FMT[1:0] = 11

DAC: 24-Bit, MSB-First, I²S



ADC: 24-Bit, MSB-First, I²S

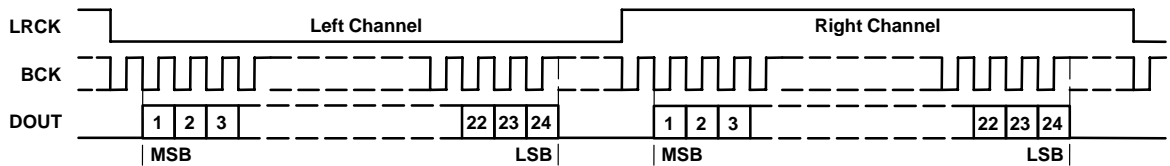
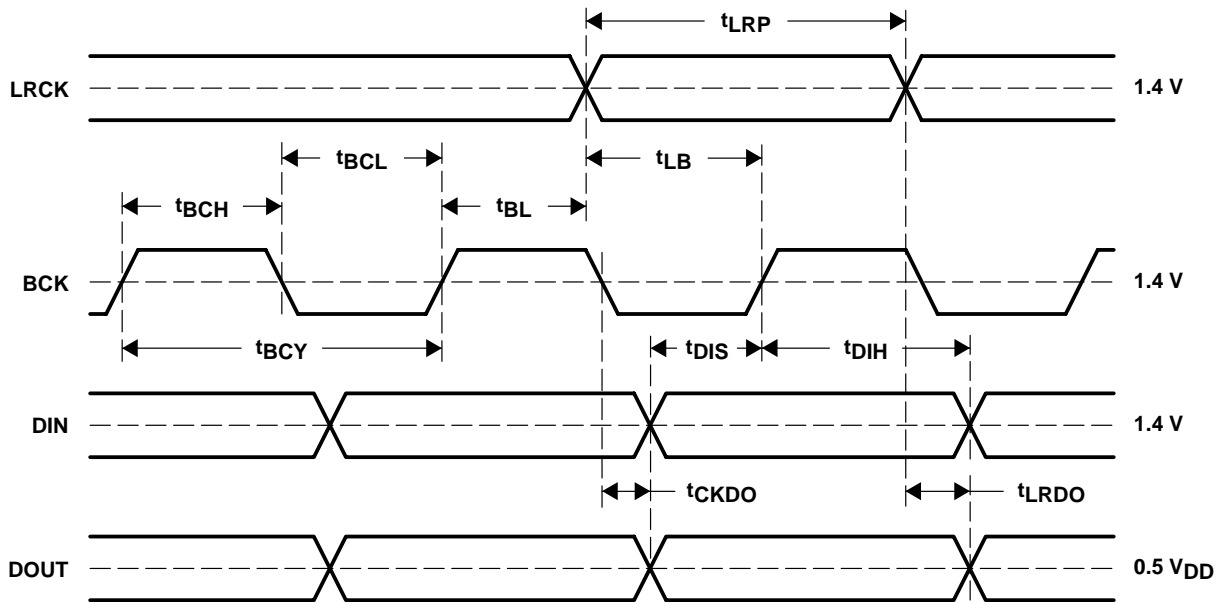


Figure 48. Audio Data Input/Output Format (Continued)

PCM audio interface (continued)



PARAMETER		MIN	MAX	UNIT
t_{BCY}	BCK pulse cycle time	80		ns
t_{BCH}	BCK pulse duration, HIGH	35		ns
t_{BCL}	BCK pulse duration, LOW	35		ns
t_{BL}	BCK rising edge to LRCK edge	10		ns
t_{LB}	LRCK edge to BCK rising edge	10		ns
t_{LRP}	LRCK pulse duration	2.1		μ s
t_{DIS}	DIN setup time	10		ns
t_{DIH}	DIN hold time	10		ns
t_{CKDO}	DOUT delay time from BCK falling edge		20	ns
t_{LRDO}	DOUT delay time from LRCK edge		20	ns
t_R	Rising time of all signals		10	ns
t_F	Falling time of all signals		10	ns

Figure 49. Audio Data Input/Output Timing

synchronization with digital audio system

The PCM3010 operates with LRCK and BCK synchronized to the system clock. The PCM3010 does not need a specific phase relationship between LRCK, BCK and the system clock, but does require the synchronization of LRCK, BCK, and the system clock.

If the relationship between system clock and LRCK changes more than ± 6 BCKs during one sample period due to LRCK jitter, etc., internal operation of DAC halts within $6/f_S$, and the analog output is forced to $0.5 V_{CC2}$ until resynchronization between the system clock, LRCK, and BCK is completed and then $t_{DACDLY2}$ elapses.

Internal operation of the ADC also halts within $6/f_S$, and the digital output is forced to a ZERO code until resynchronization between the system clock, LRCK, and BCK is completed, and then $t_{ADC DLY2}$ elapses.

In the case of changes less than ± 5 BCKs, resynchronization does not occur and the previously described discontinuity in analog/digital output control does not occur.

synchronization with digital audio system (continued)

Figure 50 illustrates the DAC analog output and ADC digital output for loss of synchronization.

During undefined data, some noise may be generated in the audio signal. Also, the transition from normal to undefined data and from undefined or zero data to normal creates a data discontinuity on the analog and digital outputs, which may generate some noise in the audio signal.

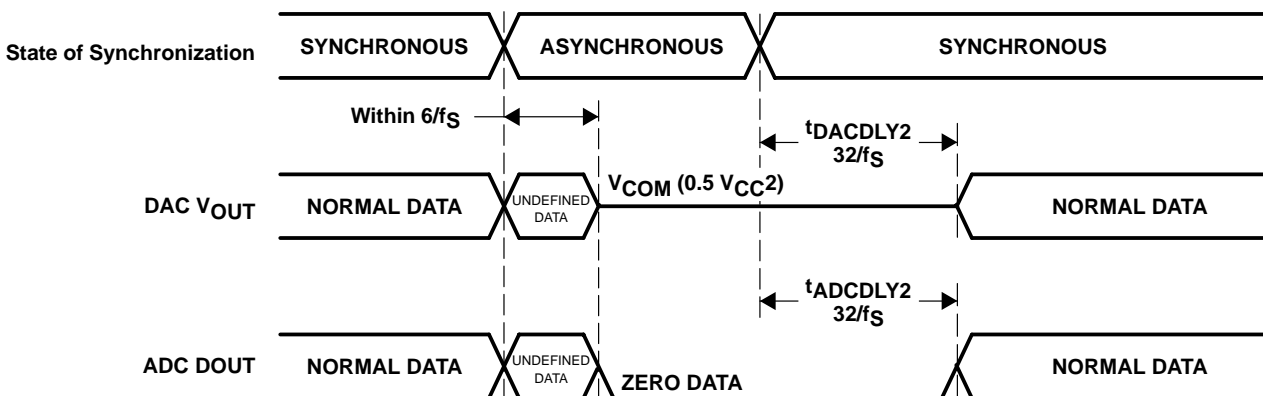


Figure 50. DAC Output and ADC Output for Lost of Synchronization

de-emphasis control

DEMP1, DEMP0: De-emphasis control pins select the de-emphasis mode of the DACs as shown below.

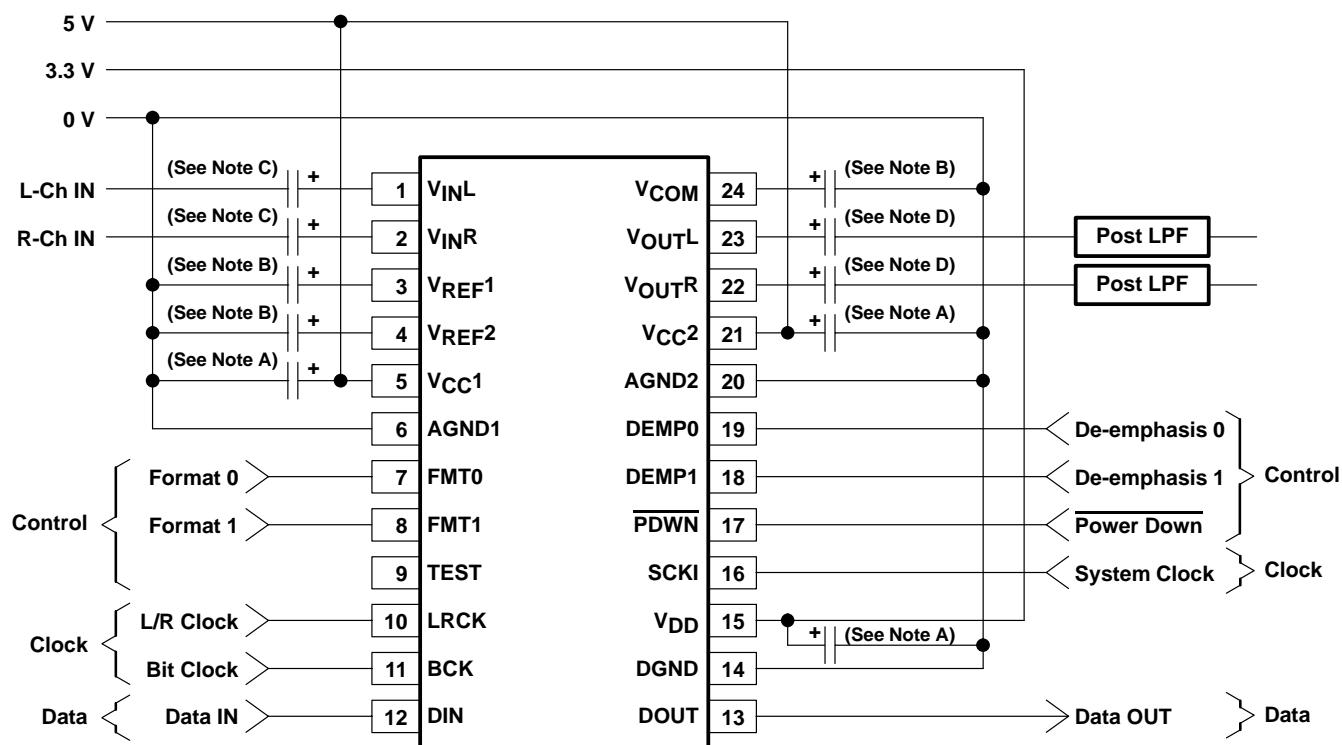
DEMP1	DEMP0	DESCRIPTION
LOW	LOW	De-emphasis 44.1 kHz ON
LOW	HIGH	De-emphasis OFF
HIGH	LOW	De-emphasis 48 kHz ON
HIGH	HIGH	De-emphasis 32 kHz ON

test control

TEST: The TEST pin is used for device testing; it must be connected to DGND for normal operation.

typical circuit connection

The following figure illustrates typical circuit connection.



- NOTES: A. 0.1 μ F ceramic and 10 μ F electrolytic capacitors typical, depending on power supply quality and pattern layout.
 B. 0.1 μ F ceramic and 10 μ F electrolytic capacitors are recommended.
 C. 1 μ F electrolytic capacitor typical, gives 8-Hz cutoff frequency of input HPF in normal operation and gives settling time with 20 ms ($1 \mu\text{F} \times 20 \text{k}\Omega$) time constant in power ON and power down OFF period.
 D. 10 μ F electrolytic capacitor typical, gives 2-Hz cutoff frequency for 10-k Ω post-LPF input resistance in normal operation and gives settling time with 100 ms ($10 \mu\text{F} \times 10 \text{k}\Omega$) time constant in power ON and power down OFF period.

design and layout considerations in application

power supply pins (V_{CC1} , V_{CC2} , V_{DD})

The digital and analog power supply lines to the PCM3010 should be bypassed to the corresponding ground pins, with 0.1- μ F ceramic and 10- μ F electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC and the DAC.

Although the PCM3010 has three power lines to maximize the potential of dynamic performance, using one common 5-V power supply for V_{CC1} and V_{CC2} and a 3.3-V power supply, which is generated from the 5-V V_{CC1} and V_{CC2} power supply, for V_{DD} . This power supply arrangement is recommended to avoid unexpected power supply trouble, like latch-up or power supply sequencing problems.

grounding ($AGND1$, $AGND2$, $DGND$)

To maximize the dynamic performance of the PCM3010, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. They should be connected directly to each other under the connected parts to reduce the potential for noise problems.

V_{IN} pins

A 1- μ F electrolytic capacitor is recommended as an ac-coupling capacitor, which gives an 8-Hz cutoff frequency. If a higher full-scale input voltage is required, it can be adjusted by adding only one series resistor to each V_{IN} pin.

V_{REF1}, V_{REF2} pins

A 0.1- μ F ceramic capacitor and a 10- μ F electrolytic capacitor are recommended between V_{REF1}, V_{REF2}, and AGND1 to ensure low source impedance of the ADC references. These capacitors should be located as close as possible to the V_{REF1} and V_{REF2} pins and the AGND1 pin to reduce dynamic errors on the ADC references.

V_{COM} pin

A 0.1- μ F ceramic capacitor and a 10- μ F electrolytic capacitor are recommended between V_{COM} and AGND2 to ensure low source impedance of the DAC common voltage. These capacitors should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the DAC common voltage.

system clock

The quality of SCKI may influence dynamic performance, as the PCM3010 (both DAC and ADC) operates based on SCKI. Therefore, it may be necessary to consider the jitter, duty cycle, rise and fall time, etc., of the system clock.

reset control

If large capacitors (more than 22 μ F) are used on V_{REF1}, V_{REF2}, and V_{COM}, external reset control by $\overline{\text{PDWN}} = \text{LOW}$ is required after the V_{REF1}, V_{REF2}, and V_{COM} transient response settles.

external mute control

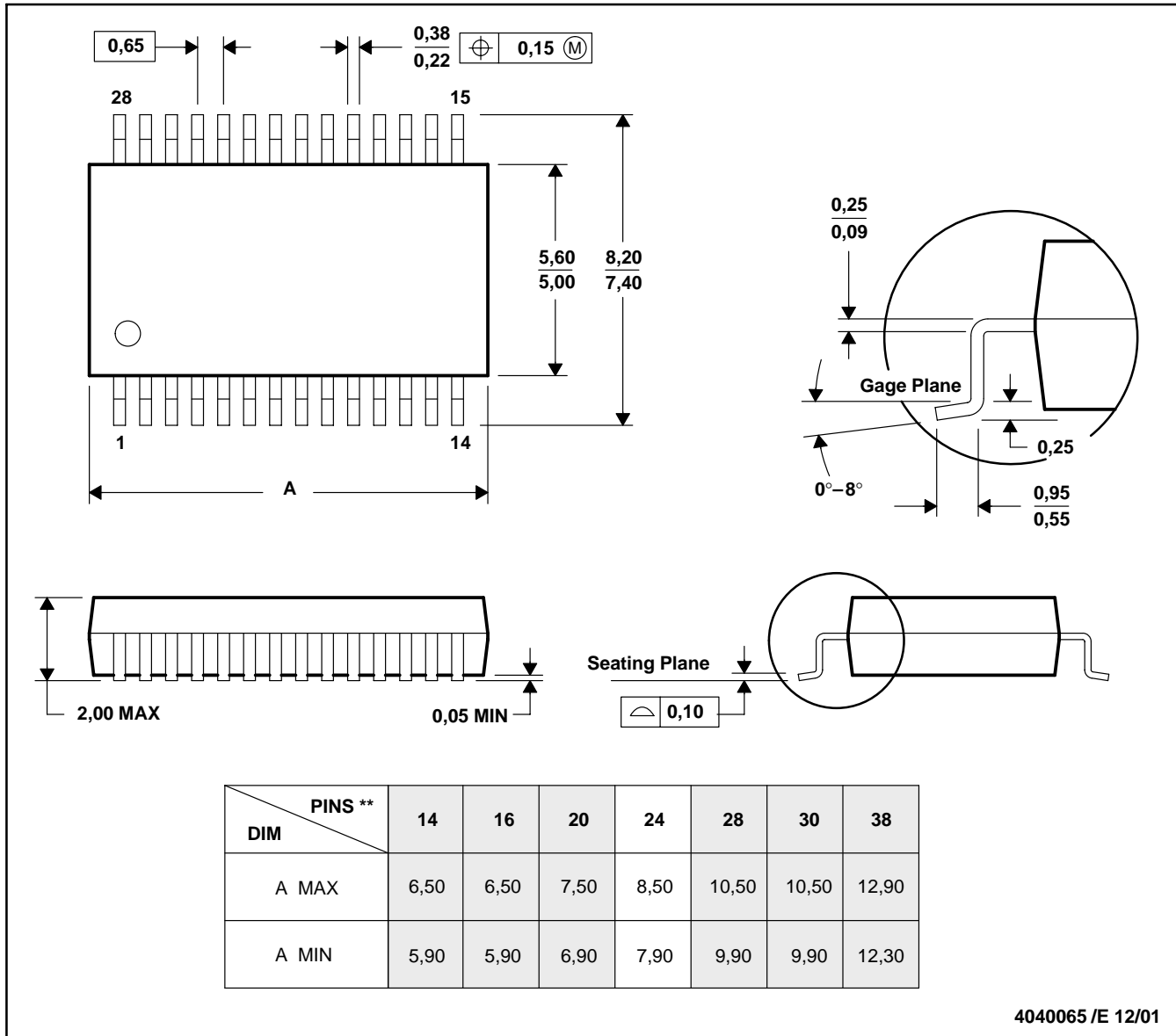
To eliminate the clicking noise which is generated by DAC output dc level change during power-down ON/OFF control, external mute control is generally required. The recommended control sequence is: external mute ON, codec power down ON, SCKI stop and restart if necessary, codec power down OFF, and external mute OFF.

MECHANICAL DATA

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



4040065 /E 12/01

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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