SN74LVC32374A
32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 4.5 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**

- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

description/ordering information

This 32-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC32374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA – GKE	Tape and reel	SN74LVC32374AGKER	NC374A
	LFBGA – ZKE (Pb-free)		SN74LVC32374AZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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SN74LVC32374A
32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

GKE OR ZKE PACKAGE
(TOP VIEW)
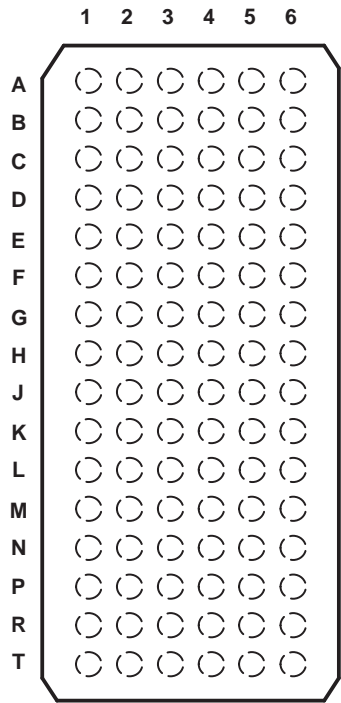
terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	1$\overline{\text{OE}}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V_{CC}	V_{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V_{CC}	V_{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	2$\overline{\text{OE}}$	2CLK	2D8	2D7
J	3Q2	3Q1	3$\overline{\text{OE}}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V_{CC}	V_{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V_{CC}	V_{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4$\overline{\text{OE}}$	4CLK	4D8	4D7

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{OE}}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels

To Seven Other Channels

To Seven Other Channels
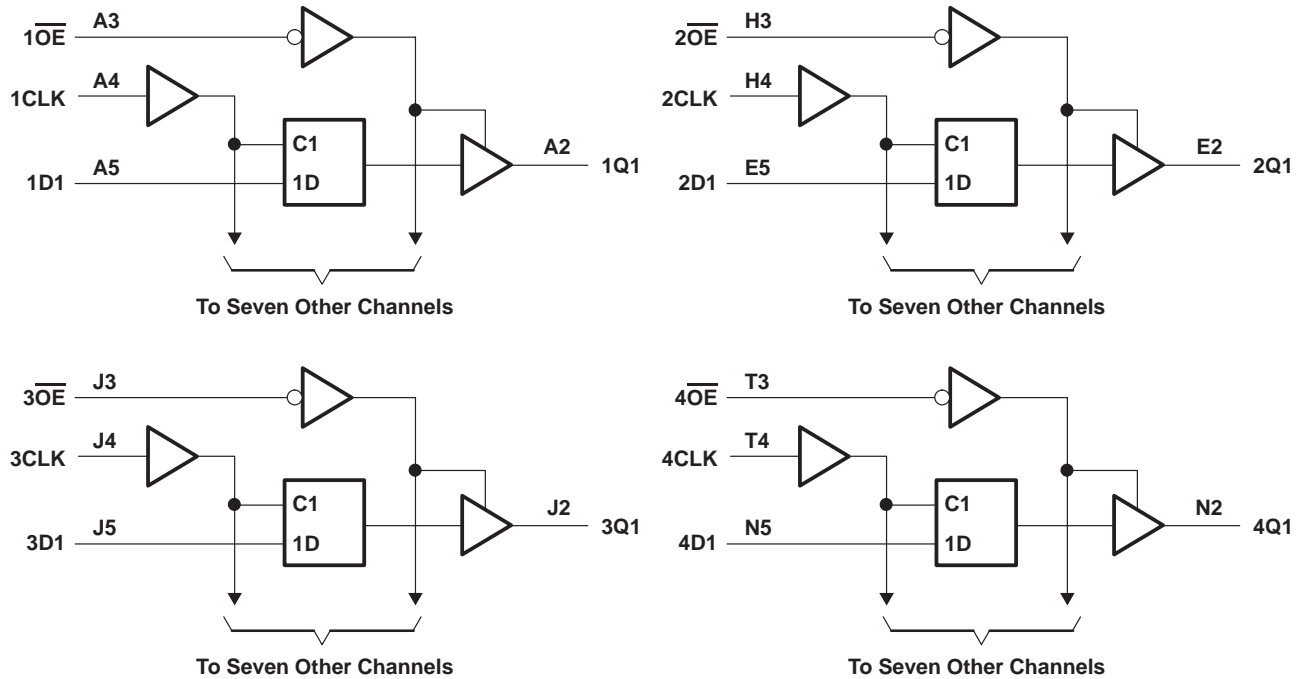
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
   (see Note 1) .... −0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
   (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Continuous output current, I_O .... ±50 mA

Continuous current through each V_{CC} or GND .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): GKE/ZKE package .... 40°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The value of V_{CC} is provided in the recommended operating conditions table.
         3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	$I_{OH} = -100$ μA		1.65 V to 3.6 V	$V_{CC}-0.2$			V
	$I_{OH} = -4$ mA		1.65 V	1.2			
	$I_{OH} = -8$ mA		2.3 V	1.7			
	$I_{OH} = -12$ mA		2.7 V	2.2			
			3 V	2.4			
	$I_{OH} = -24$ mA		3 V	2.2			
V_{OL}	$I_{OL} = 100$ μA		1.65 V to 3.6 V			0.2	V
	$I_{OL} = 4$ mA		1.65 V			0.45	
	$I_{OL} = 8$ mA		2.3 V			0.7	
	$I_{OL} = 12$ mA		2.7 V			0.4	
	$I_{OL} = 24$ mA		3 V			0.55	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5	μA
I_{off}	V_I or $V_O = 5.5$ V		0			±10	μA
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			40	μA
	$3.6\ V \le V_I \le 5.5\ V$‡					40	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		5		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		6.5		pF

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		150		150		150		150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2.4		1.6		1.9		1.9		ns
t_h	Hold time, data after CLK↑	0.8		1		1.1		1.9		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		150		MHz
t_{pd}	CLK	Q	1	6.5	1	4.3	1	4.9	1.5	4.5	ns
t_{en}	$\overline{OE}$	Q	1	6.7	1	4.7	1	5.3	1.5	4.6	ns
t_{dis}	$\overline{OE}$	Q	1	10.7	1	5	1	6.1	1.5	5.5	ns
$t_{sk(o)}$										1	ns

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	47	52	58	pF
	Outputs disabled		21	23	24	

PARAMETER MEASUREMENT INFORMATION
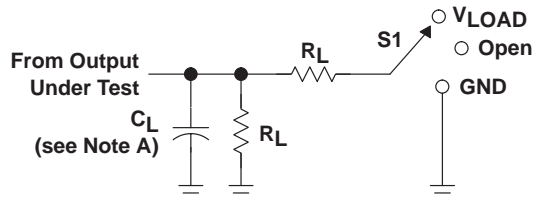
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

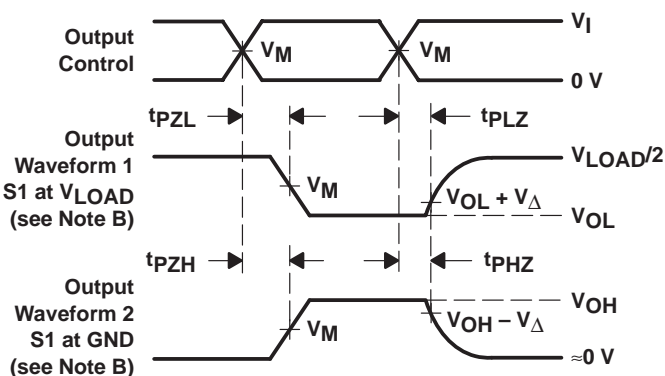| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8\ V \pm 0.15\ V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
$2.5\ V \pm 0.2\ V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\ V \pm 0.3\ V$	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
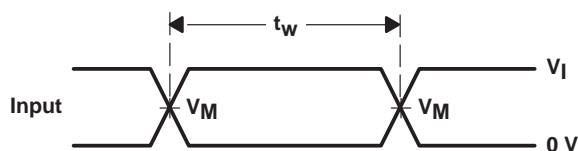
VOLTAGE WAVEFORMS
PULSE DURATION
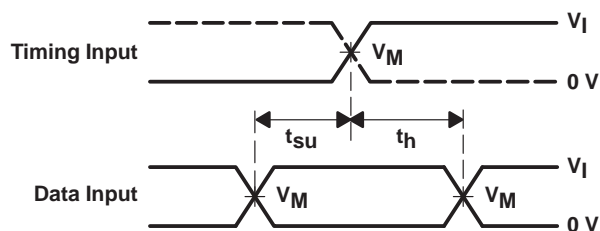
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
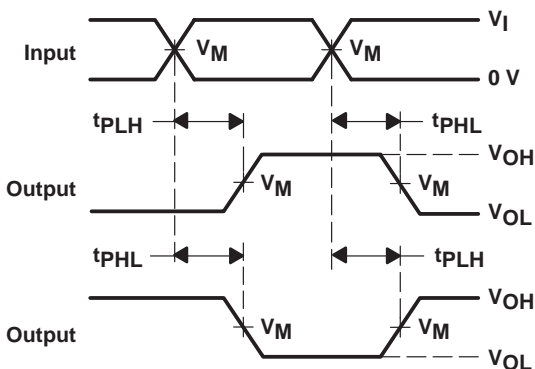
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
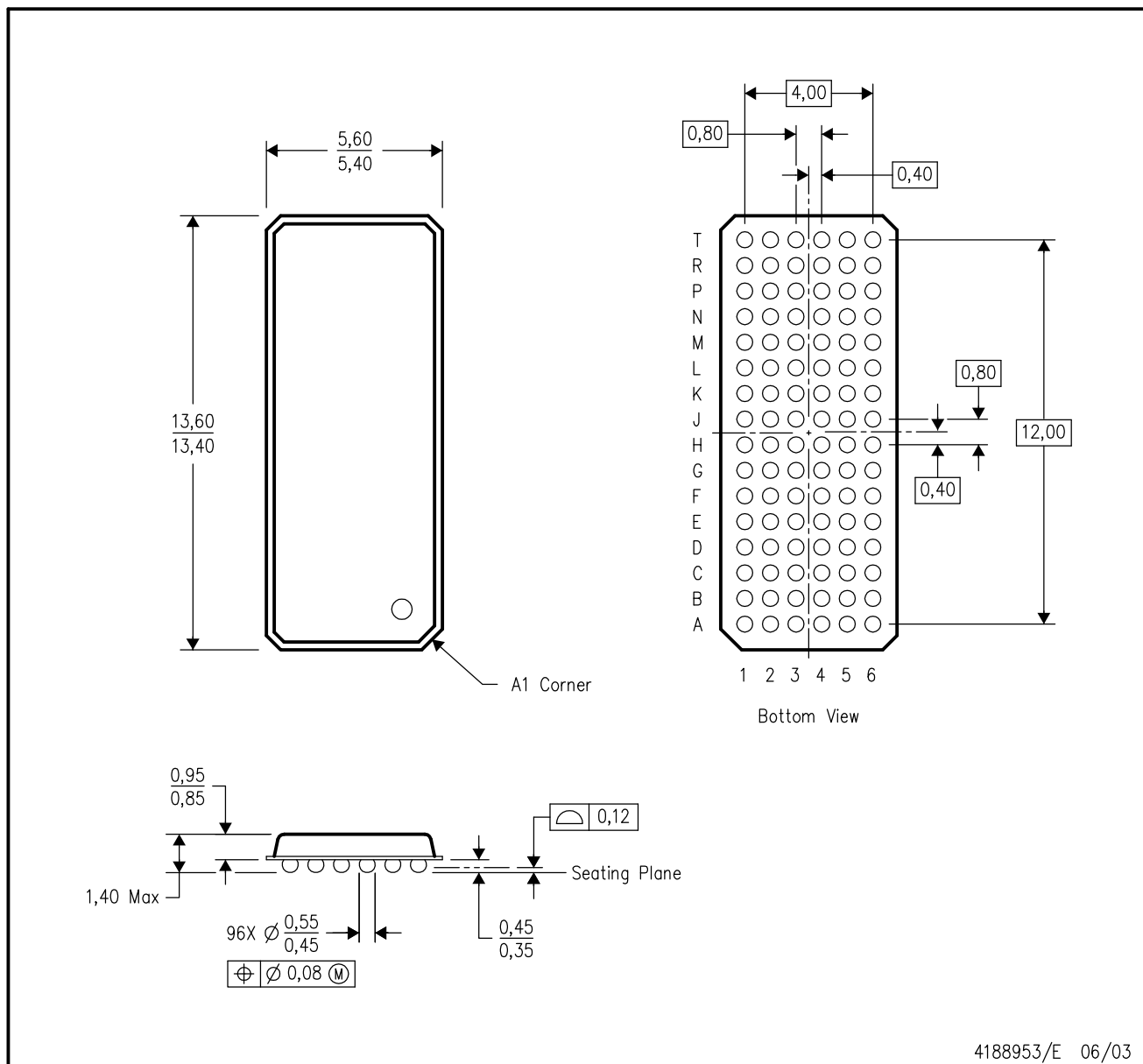**INVERTING AND NONINVERTING OUTPUTS**

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
   D. The outputs are measured one at a time with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

GKE (R−PBGA−N96) PLASTIC BALL GRID ARRAY

5,60
5,40

13,60
13,40

A1 Corner

4,00

0,80

0,40

T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

0,80

0,40

12,00

1 2 3 4 5 6

Bottom View

0,95
0,85

1,40 Max

0,12

Seating Plane
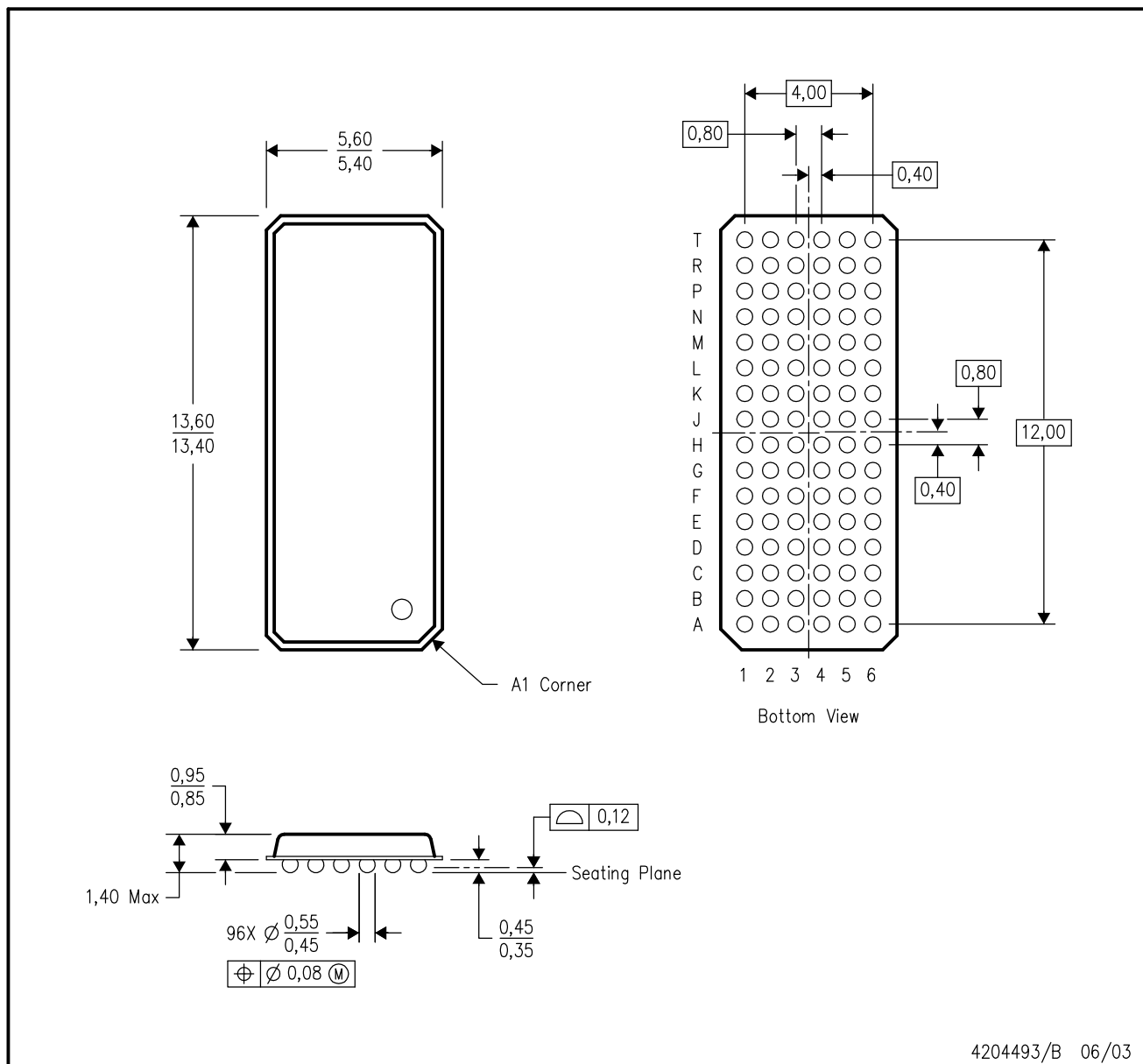
96X Ø 0,55
0,45

0,45
0,35

⊕ Ø 0,08 Ⓜ

4188953/E 06/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration
D. Falls within JEDEC MO−205 variation CC.
E. This package is tin−lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead−free.

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ZKE (R−PBGA−N96)   PLASTIC BALL GRID ARRAY

A1 Corner

Bottom View

Seating Plane

0,95
0,85

1,40 Max

96X ⌀ 0,55
        0,45

⊕ ⌀ 0,08 Ⓜ

0,45
0,35

4204493/B   06/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   MicroStar BGA™ configuration
         D.   Falls within JEDEC MO−205 variation CC.
         E.   This package is lead−free. Refer to the 96 GKE package (drawing 4188953) for tin−lead (SnPb).

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