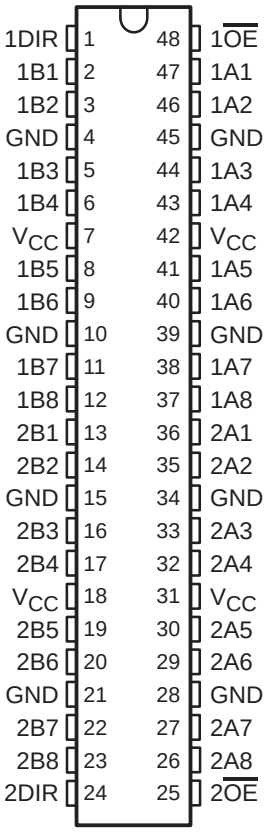
- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 2.7 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 8.5 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCR162245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses effectively are isolated.

All outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVCR162245DL	LVCR162245
		Tape and reel	SN74LVCR162245DLR	
	TSSOP – DGG	Tape and reel	SN74LVCR162245DGGR	LVCR162245
	VFBGA – GQL	Tape and reel	SN74LVCR162245KR	LEP245
	VFBGA – ZQL (Pb-free)		74LVCR162245ZQLR	

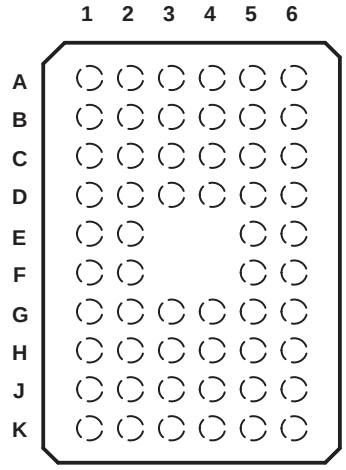
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by $\overline{OE}$ or DIR.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL OR ZQL PACKAGE
(TOP VIEW)



terminal assignments

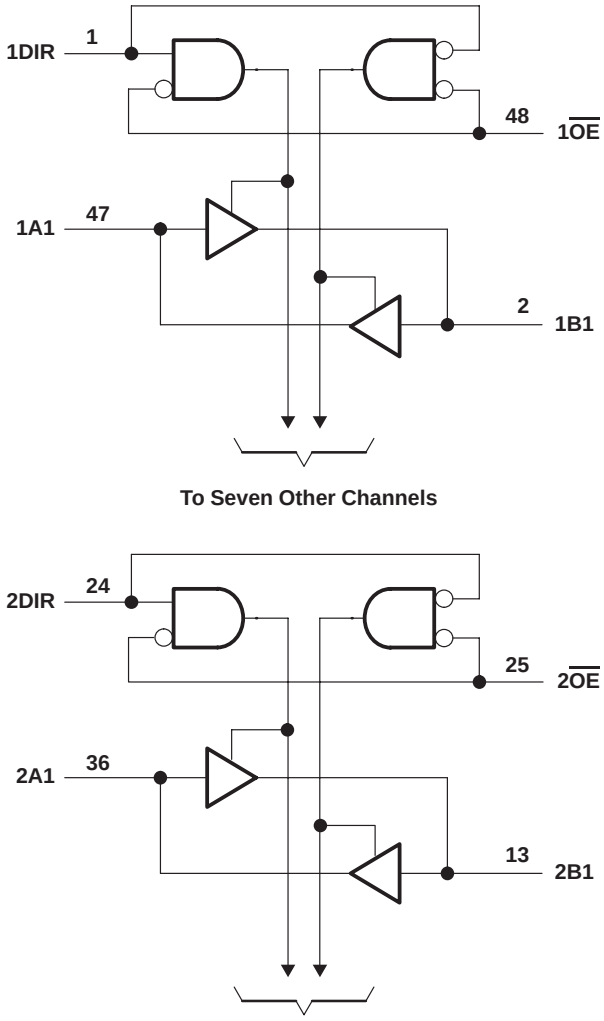
	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{OE}$

NC – No internal connection

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the DGG and DL packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to V_{CC} + 4.6 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 70°C/W
DL package . . . . . 63°C/W
GQL/ZQL package . . . . . 42°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–8	mA
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		8	mA
		V_{CC} = 3 V		12	
$\Delta t/\Delta V$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP‡	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V
		I_{OH} = –4 mA,	V_{IH} = 2 V	2.7 V	2.2			
		I_{OH} = –8 mA,	V_{IH} = 2 V		2			
		I_{OH} = –6 mA,	V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –12 mA,	V_{IH} = 2 V		2			
V_{OL}		I_{OL} = 100 μA		MIN to MAX			0.2	V
		I_{OL} = 4 mA,	V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V				0.6	
		I_{OL} = 6 mA,	V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V				0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$		V_I = 0.8 V		3 V	75			μA
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V		3.6 V			±500	μA
I_{OZ}§		V_O = 0 V or (V_{CC} to 5.5 V)		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			20	μA
		3.6 V ≤ V_I ≤ 5.5 V¶					20	
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		2.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		3.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ For the total leakage current in an I/O port, please consult the $I_{I(hold)}$ specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. The bus-hold current, at input voltage greater than V_{CC}, is negligible.
¶ This applies in the disabled state only.

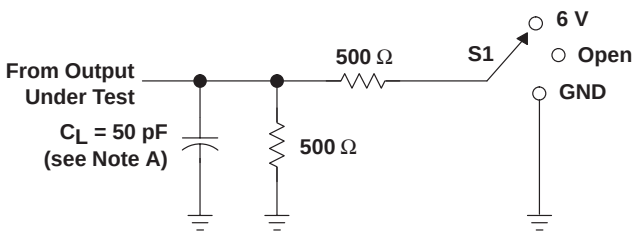
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	7.5	1.5	8.5	ns
t_{en}	$\overline{OE}$	A or B	1.5	9	1.5	10	ns
t_{dis}	$\overline{OE}$	A or B	1.5	7.5	1.5	8.5	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

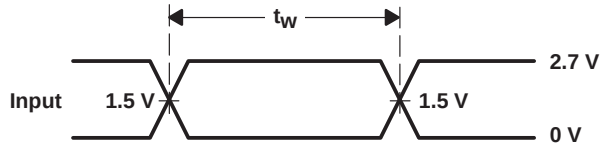
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 10 MHz	20	pF
		Outputs disabled		2	

PARAMETER MEASUREMENT INFORMATION

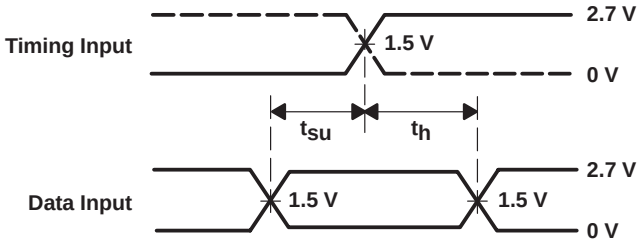


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

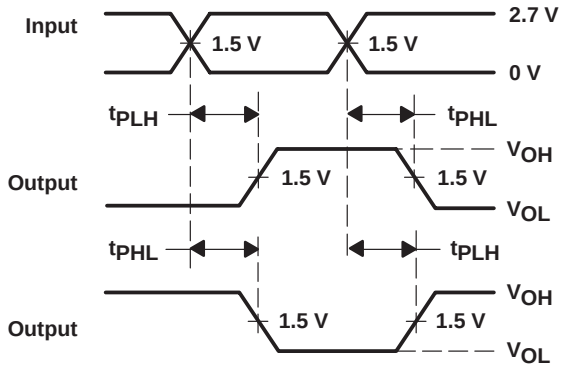
LOAD CIRCUIT FOR OUTPUTS



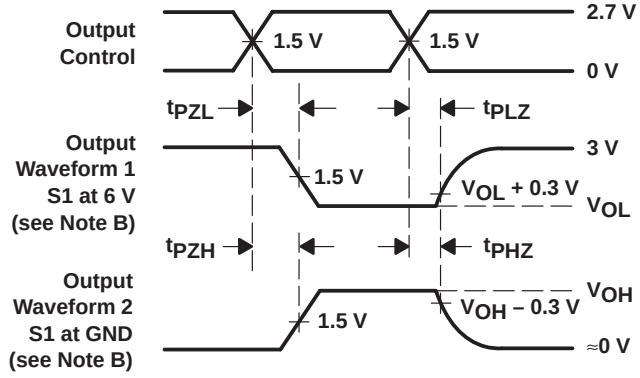
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

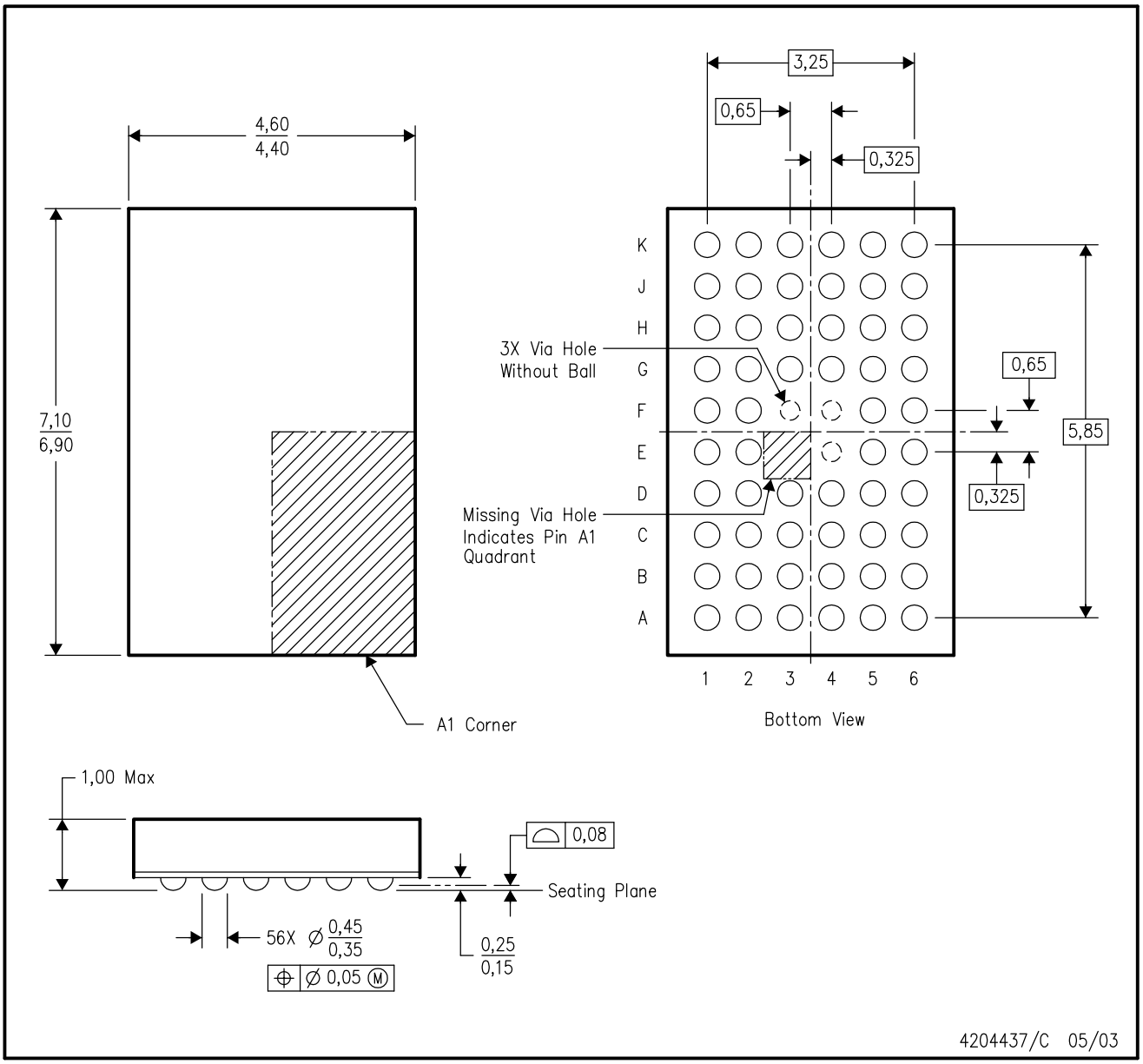


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

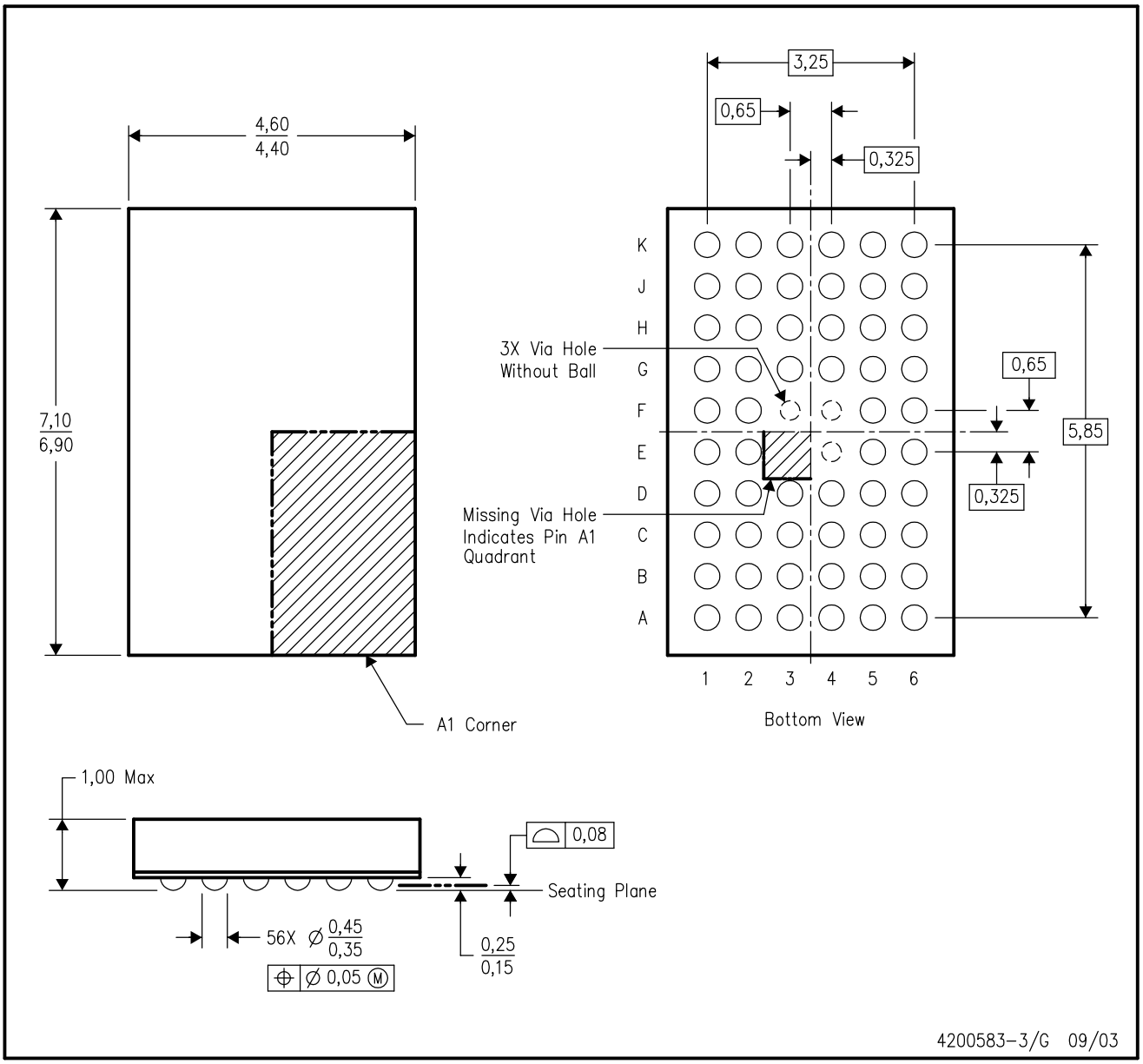
ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY

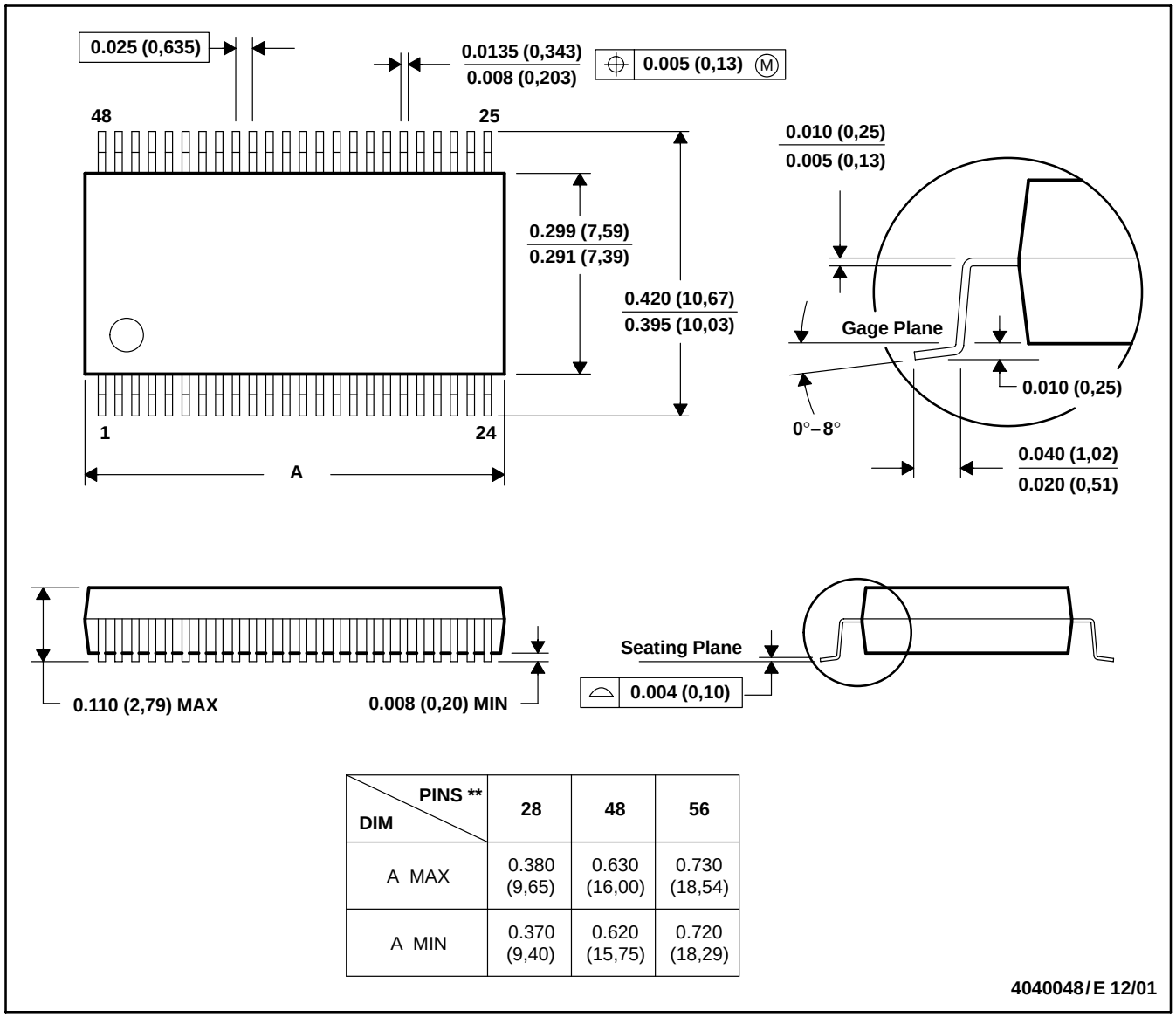


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

MicroStar Junior is a trademark of Texas Instruments.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



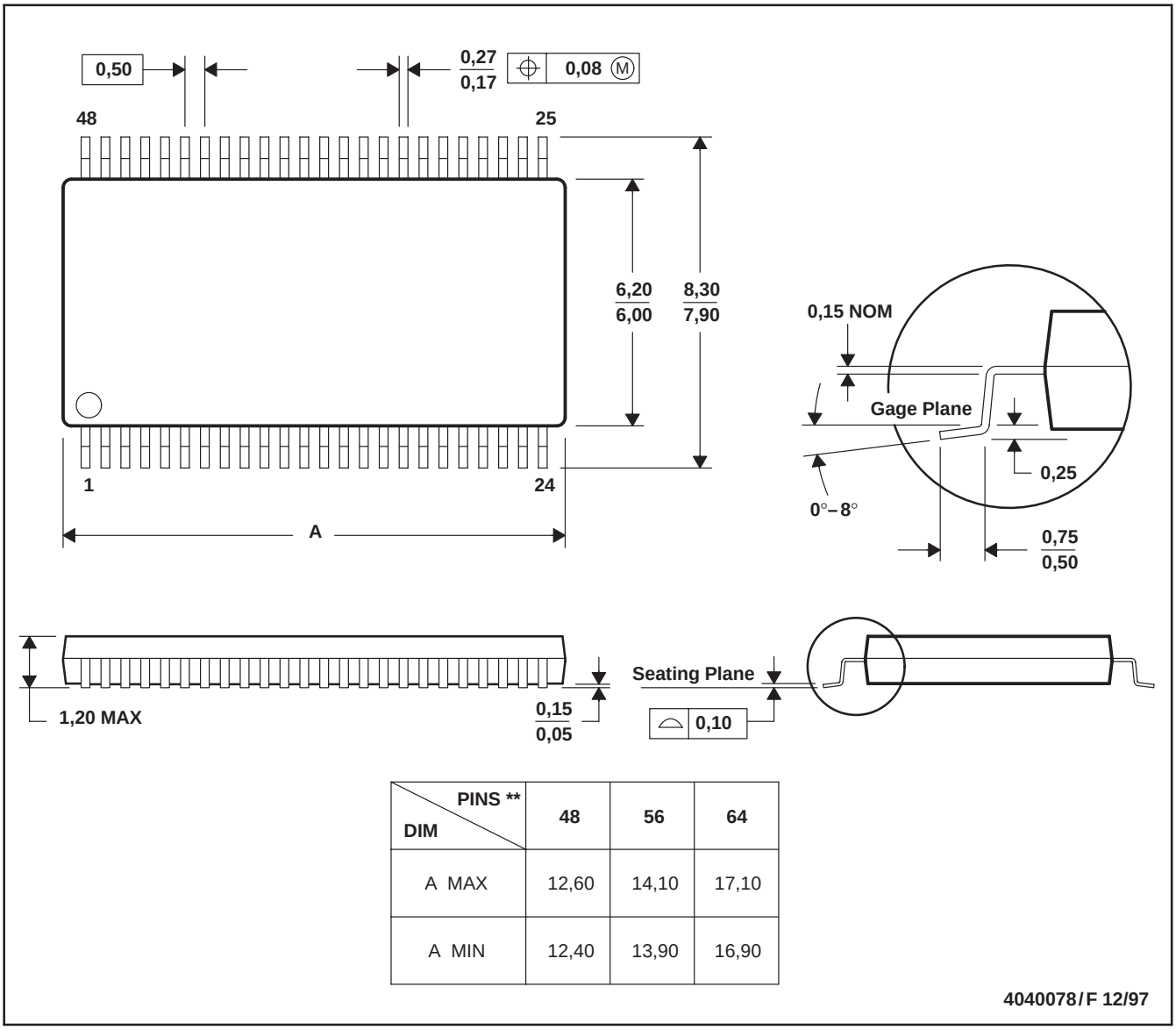
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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