- **Operates From 2.7 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 6.3 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

DIR	1	20	V_{CC}
A1	2	19	$\overline{OE}$
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8
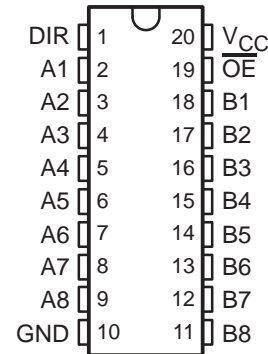
description/ordering information

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCZ245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 20	SN74LVCZ245AN	SN74LVCZ245AN
	SOIC – DW	Tube of 25	SN74LVCZ245ADW	LVCZ245A
		Reel of 2000	SN74LVCZ245ADWR	
	SOP – NS	Reel of 2000	SN74LVCZ245ANSR	LVCZ245A
	SSOP – DB	Reel of 2000	SN74LVCZ245ADBR	CV245A
	TSSOP – PW	Tube of 70	SN74LVCZ245APW	CV245A
		Reel of 2000	SN74LVCZ245APWR	CV245A
		Reel of 250	SN74LVCZ245APWT	CV245A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)

To Seven Other Channels
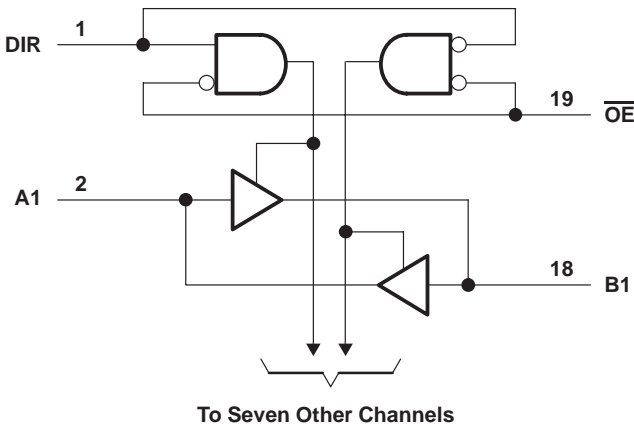
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) . . . . −0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
   (see Note 1) . . . . −0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
   (see Notes 1 and 2) . . . . −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) . . . . −50 mA

Output clamp current, I_{OK} (V_O < 0) . . . . −50 mA

Continuous output current, I_O . . . . ±50 mA

Continuous current through V_{CC} or GND . . . . ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . 70°C/W

                                                                    DW package . . . . 58°C/W

                                                                    N package . . . . 89°C/W

                                                                    NS package . . . . 60°C/W

                                                                    PW package . . . . 83°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1.   The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2.   The value of V_{CC} is provided in the recommended operating conditions table.
         3.   The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			6	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		150		µs/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = −100 µA		2.7 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −12 mA		2.7 V		2.2		
				3 V		2.4		
		I_{OH} = −24 mA		3 V		2.2		
V_{OL}		I_{OL} = 100 µA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±5	µA
I_{off}		V_I or V_O = 5.5 V		0			±5	µA
I_{OZ}‡		V_O = 0 to 5.5 V		3.6 V			±5	µA
I_{OZPU}		V_O = 0.5 V to 2.5 V,	$\overline{OE}$ = don't care	0 to 1.5 V			±5	µA
I_{OZPD}		V_O = 0.5 V to 2.5 V,	$\overline{OE}$ = don't care	1.5 V to 0			±5	µA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			100	µA
		3.6 V ≤ V_I ≤ 5.5 V§					100	
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			100	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A		7.3	1.5	6.3	ns
t_{en}	$\overline{OE}$	A or B		9.5	1.5	8.5	ns
t_{dis}	$\overline{OE}$	A or B		8.5	1.7	7.5	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 3.3 V TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	42	pF
		Outputs disabled	3	

(Test conditions: f = 10 MHz)

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PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V
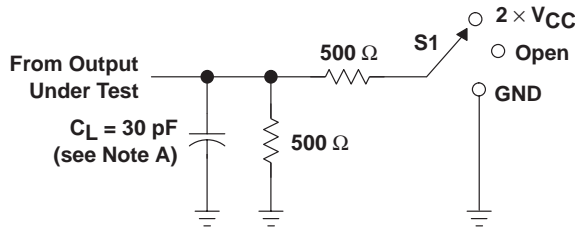
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

VOLTAGE WAVEFORMS
PULSE DURATION
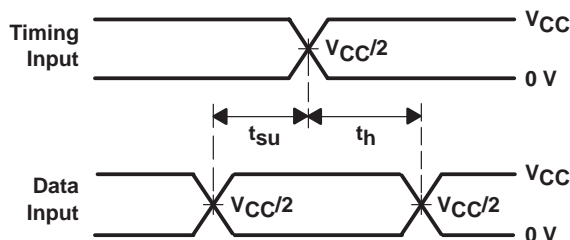
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
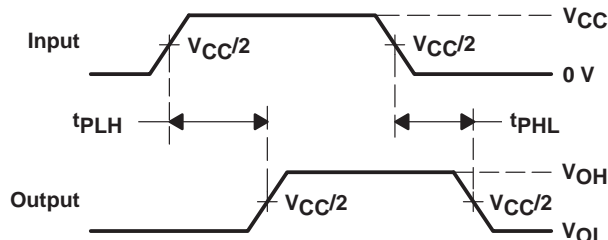
VOLTAGE WAVEFORMS
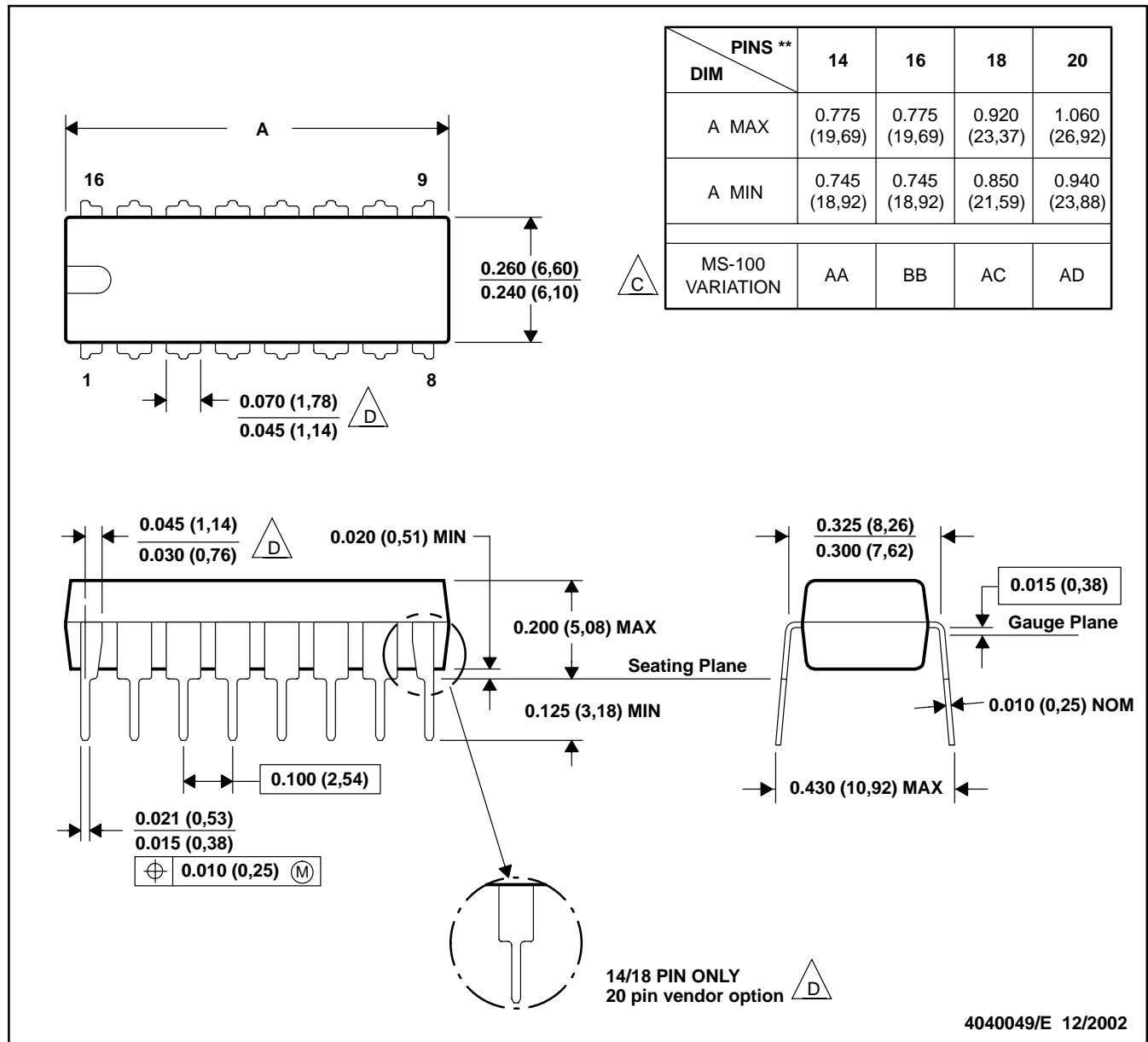**PROPAGATION DELAY TIMES**
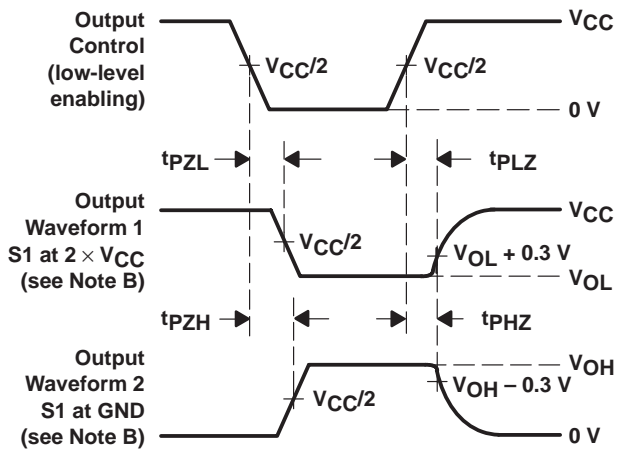
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
  D. The outputs are measured one at a time with one transition per measurement.
  E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
  F. t_{PZL} and t_{PZH} are the same as t_{en}.
  G. t_{PLH} and t_{PHL} are the same as t_{pd}.
  H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

MECHANICAL

MPDI002C – JANUARY 1995 – REVISED DECEMBER 20002

N (R-PDIP-T**)   PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
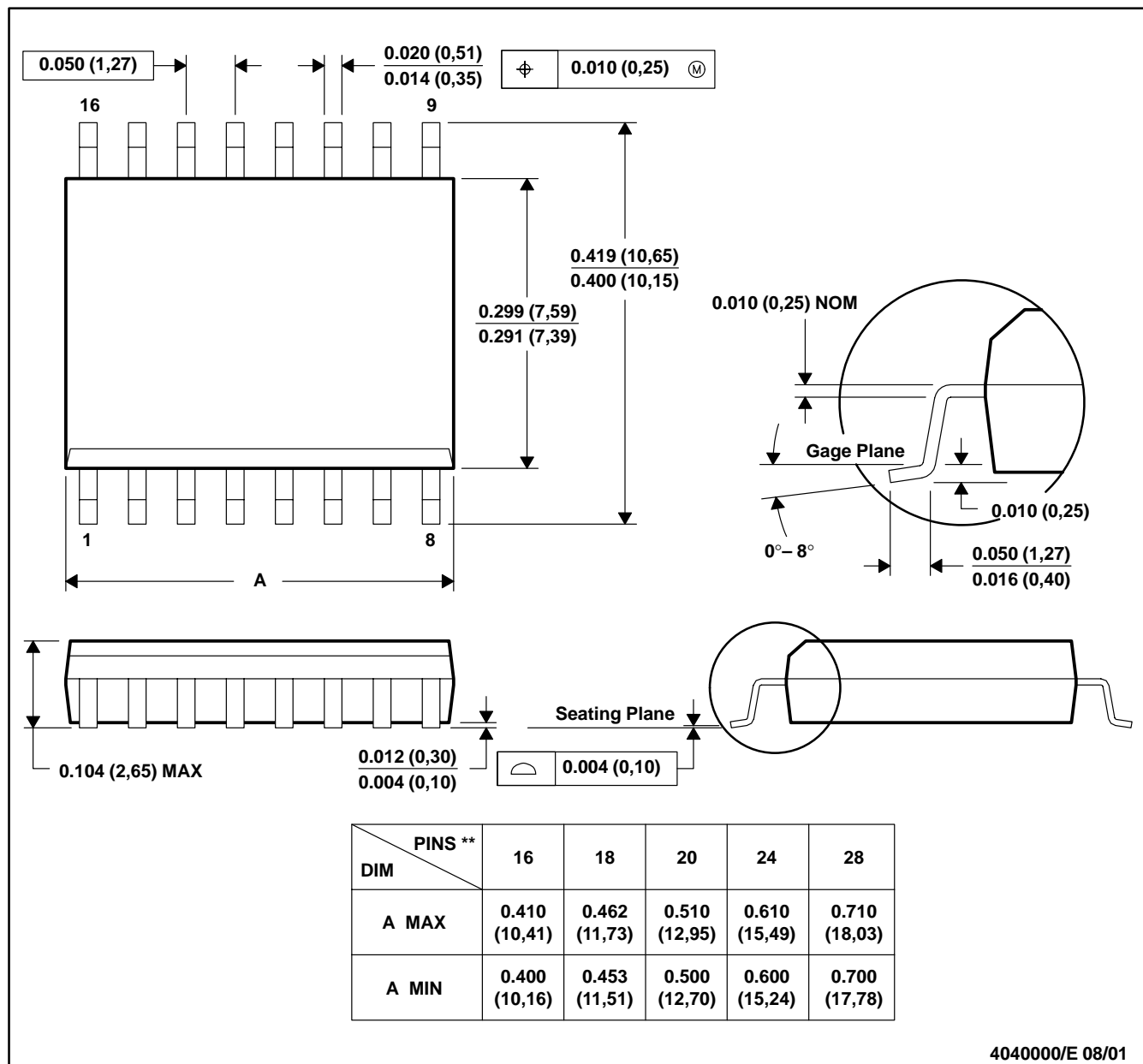   B. This drawing is subject to change without notice.
   C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
   D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN

	PINS **	16	18	20	24	28
DIM						
A MAX		0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN		0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
   D. Falls within JEDEC MS-013

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NS (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

DIM ＼ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

1,27

0,51 / 0,35   ⊕ 0,25 Ⓜ

5,60 / 5,00   8,20 / 7,40

A

0,15 / 0,05

2,00 MAX

0,15 NOM

Gage Plane

0,25

0°–10°

1,05 / 0,55

Seating Plane

◁ 0,10

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
            B.   This drawing is subject to change without notice.
            C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

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