- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Support Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVT16500 . . . WD PACKAGE
SN74LVT16500 . . . DGG OR DL PACKAGE
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

description

The 'LVT16500 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

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description (continued)

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE[†]

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0[‡]
H	L	L	X	B_0[§]

[†] A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.
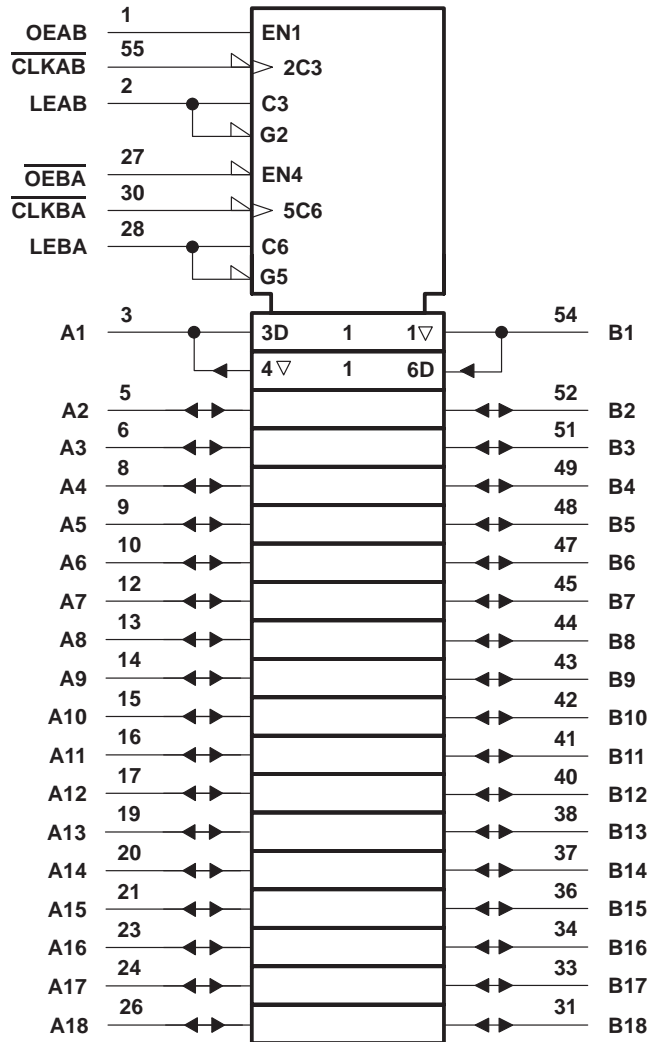
[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low

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logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
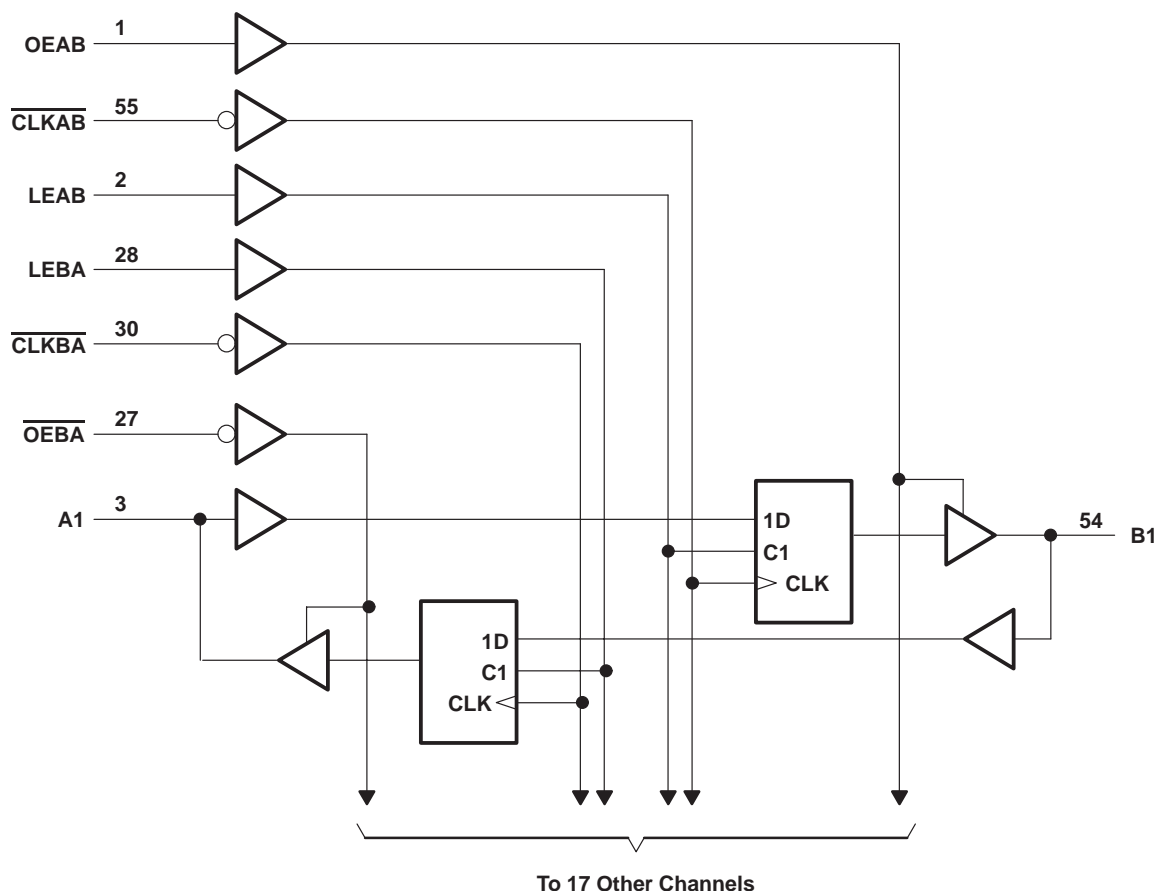
logic diagram (positive logic)

To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V

Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V

Current into any output in the low state, I_O: SN54LVT16500 .... 96 mA

SN74LVT16500 .... 128 mA

Current into any output in the high state, I_O (see Note 2): SN54LVT16500 .... 48 mA

SN74LVT16500 .... 64 mA

Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 3): DGG package .... 1 W

DL package .... 1.4 W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			SN54LVT16500		SN74LVT16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16500 MIN	SN54LVT16500 TYP†	SN54LVT16500 MAX	SN74LVT16500 MIN	SN74LVT16500 TYP†	SN74LVT16500 MAX	UNIT
V_{IK}	$V_{CC} = 2.7$ V,	$I_I = -18$ mA				−1.2			−1.2	V
V_{OH}	$V_{CC} = 2.7$ V to 3.6 V,	$I_{OH} = -100$ μA		V_{CC}−0.2			V_{CC}−0.2			V
	$V_{CC} = 2.7$ V,	$I_{OH} = -8$ mA		2.4			2.4			
	$V_{CC} = 3$ V	$I_{OH} = -24$ mA		2						
		$I_{OH} = -32$ mA					2			
V_{OL}	$V_{CC} = 2.7$ V	$I_{OL} = 100$ μA				0.2			0.2	V
		$I_{OL} = 24$ mA				0.5			0.5	
	$V_{CC} = 3$ V	$I_{OL} = 16$ mA				0.4			0.4	
		$I_{OL} = 32$ mA				0.5			0.5	
		$I_{OL} = 48$ mA				0.55				
		$I_{OL} = 64$ mA							0.55	
I_I	$V_{CC} = 3.6$ V,	$V_I = V_{CC}$ or GND	Control inputs			±1			±1	μA
	$V_{CC} = 0$ or 3.6 V,	$V_I = 5.5$ V				10			10	
	$V_{CC} = 3.6$ V	$V_I = 5.5$ V	A or B ports‡			20			20	
		$V_I = V_{CC}$				5			5	
		$V_I = 0$				−10			−10	
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V				±100			±100	μA
$I_{I(hold)}$	$V_{CC} = 3$ V	$V_I = 0.8$ V	A or B ports	75			75			μA
		$V_I = 2$ V		−75			−75			
I_{OZH}	$V_{CC} = 3.6$ V,	$V_O = 3$ V				1			1	μA
I_{OZL}	$V_{CC} = 3.6$ V,	$V_O = 0.5$ V				−1			−1	μA
I_{CC}	$V_{CC} = 3.6$ V, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}§	$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	$V_I = 3$ V or 0				3.5			3.5		pF
C_{io}	$V_O = 3$ V or 0				12			12		pF

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°$C.
‡ Unused pins at V_{CC} or GND
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT16500				SN74LVT16500				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	125	0	150	0	125	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		$\overline{CLK}$ high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before $\overline{CLKAB}$↓	1.8		1.1		1.8		1.1		ns
		B before $\overline{CLKBA}$↓	1.9		1.2		1.9		1.2		
		A or B before LE↓ , $\overline{CLK}$ high	2.2		1.3		2.2		1.3		
		A or B before LE↓ , $\overline{CLK}$ low	2.7		1.9		2.7		1.9		
t_h	Hold time	A or B after $\overline{CLK}$↓	1.2		1.2		1.2		1.2		ns
		A or B after LE↓	0.9		1.1		0.9		1.1		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16500				SN74LVT16500						UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		125		150			125		MHz
t_{PLH}	B or A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns
t_{PHL}			1.6	6		7.8	1.6	3.2	5.9		7.7	
t_{PLH}	LEBA or LEAB	A or B	2.3	7.3		8.9	2.3	4	7		8.5	ns
t_{PHL}			2.7	8.2		9.8	2.7	4.3	7.9		9.7	
t_{PLH}	$\overline{CLKBA}$ or $\overline{CLKAB}$	A or B	2	7.4		8.8	2	4.1	7		8.3	ns
t_{PHL}			2.4	8.1		10	2.4	4.4	7.9		9.9	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.2		6.1	1.2	3	5		5.9	ns
t_{PZL}			1.5	5.9		7	1.5	3	5.8		6.9	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	ns
t_{PLZ}			2.8	7.3		7.7	2.8	4.7	6.7		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION
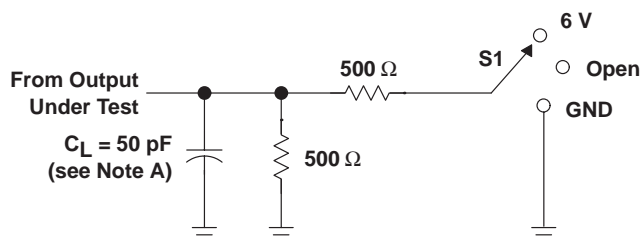
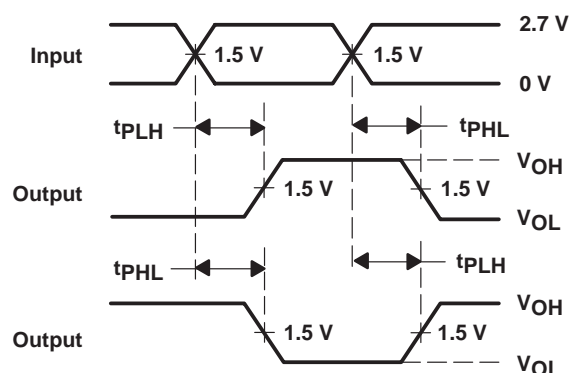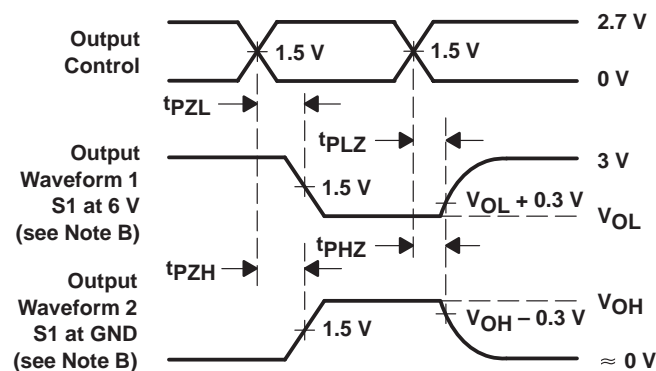| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
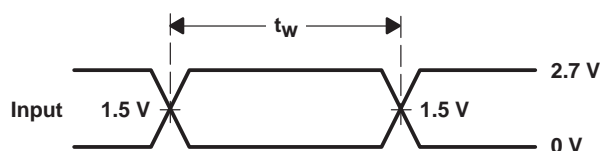
**VOLTAGE WAVEFORMS
PULSE DURATION**
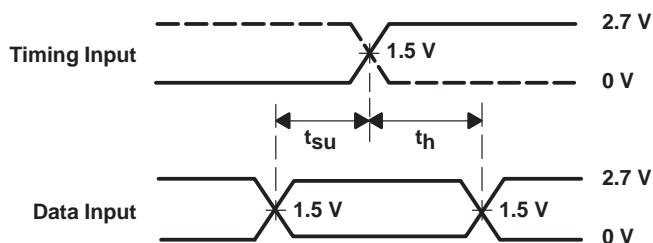
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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