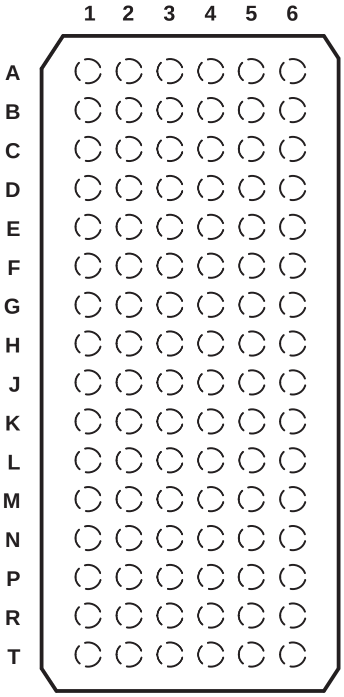
SN74LVT32240
3.3-V ABT 32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCBS747C − SEPTEMBER 2000 − REVISED SEPTEMBER 2003

- **Member of Texas Instruments Widebus+™ Family**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Supports Mixed-Mode Signal Operation (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

GKE OR ZKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Y2	1Y1	1$\overline{\text{OE}}$	2$\overline{\text{OE}}$	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	1V_{CC}	1V_{CC}	2A1	2A2
D	2Y2	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	1V_{CC}	1V_{CC}	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	4$\overline{\text{OE}}$	3$\overline{\text{OE}}$	4A4	4A3
J	5Y2	5Y1	5$\overline{\text{OE}}$	6$\overline{\text{OE}}$	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	2V_{CC}	2V_{CC}	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	2V_{CC}	2V_{CC}	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	8$\overline{\text{OE}}$	7$\overline{\text{OE}}$	8A4	8A3

description/ordering information

The SN74LVT32240 is a 32-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. The device provides inverted outputs and symmetrical active-low output-enable ($\overline{\text{OE}}$) inputs. It is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA − GKE	Tape and reel	SN74LVT32240GKER	VJ240
	LFBGA − ZKE (Pb-free)		SN74LVT32240ZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

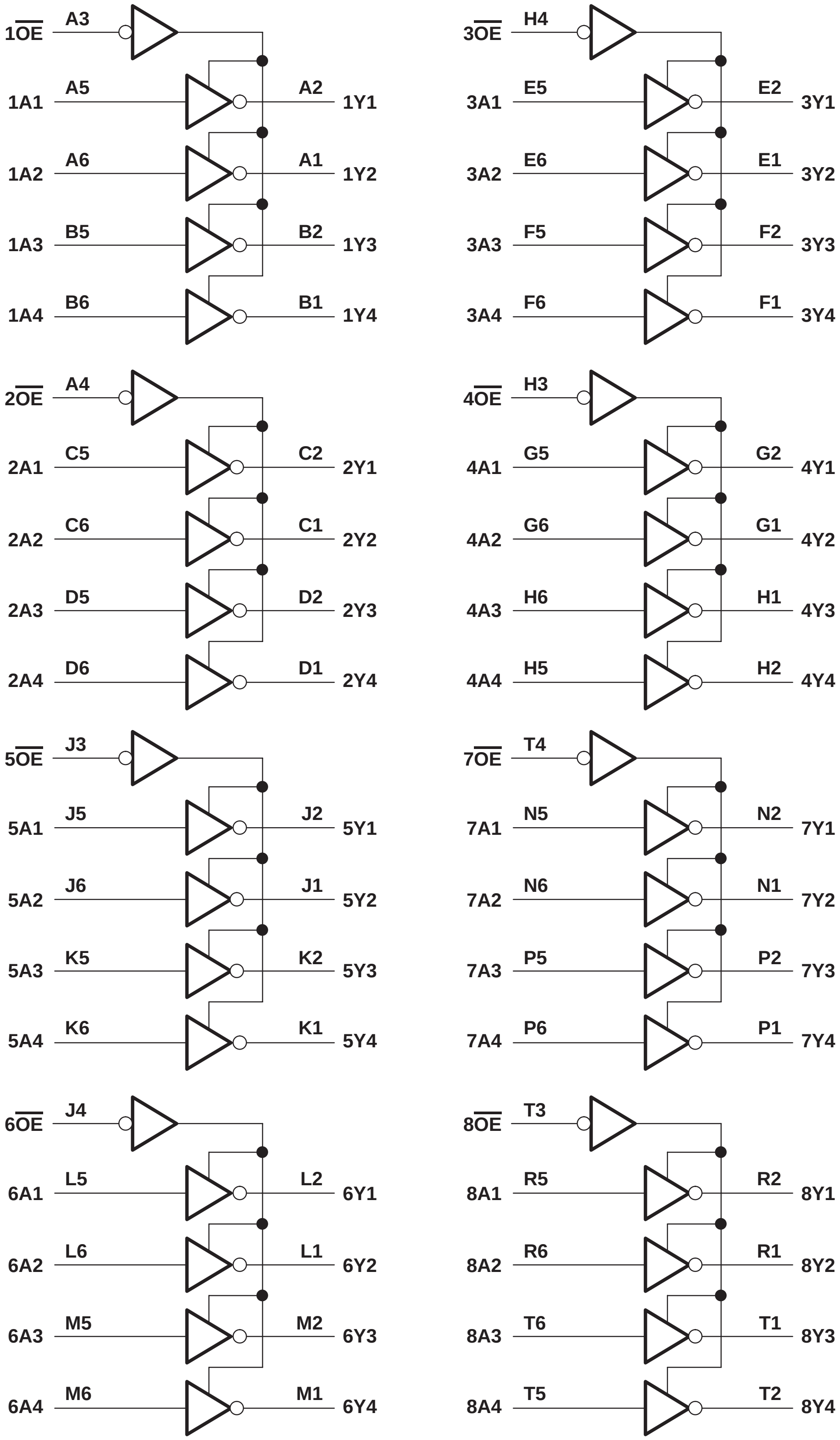
When V_{CC} is between 0 and 1.5-V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5-V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . 128 mA
Current into any output in the high state, I_O (see Note 2) . . . . 64 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . −50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 3): GKE/ZKE package . . . . 40°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			−32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		µs/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			
		V_{CC} = 3 V,	I_{OH} = −32 mA	2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1	
			V_I = 0			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100	µA
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			−5	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don’t care				±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don’t care				±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.38	mA
			Outputs low			10	
			Outputs disabled			0.38	
ΔI_{CC}‡		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2	mA
C_i		V_I = 3 V or 0			4		pF
C_o		V_O = 3 V or 0			9		pF

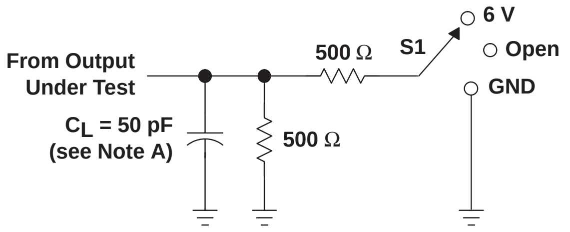
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.2	3.5		4	ns
t_{PHL}			1	2.7	3.5		4	
t_{PZH}	$\overline{OE}$	Y	1	2.6	4		4.9	ns
t_{PZL}			1.2	2.6	4.4		4.6	
t_{PHZ}	$\overline{OE}$	Y	2	3.4	4.5		5	ns
t_{PLZ}			2	3.2	4.2		4.2	
$t_{sk(o)}$					0.5		0.5	ns

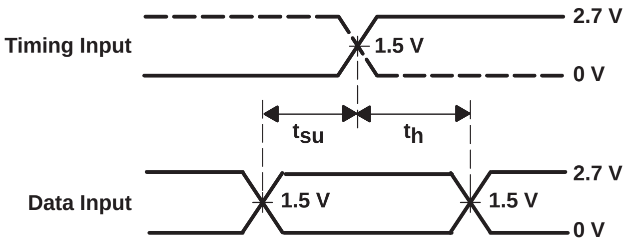
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

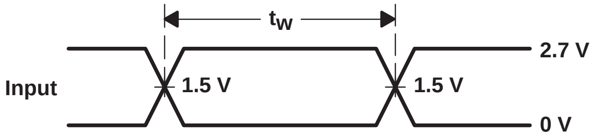
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

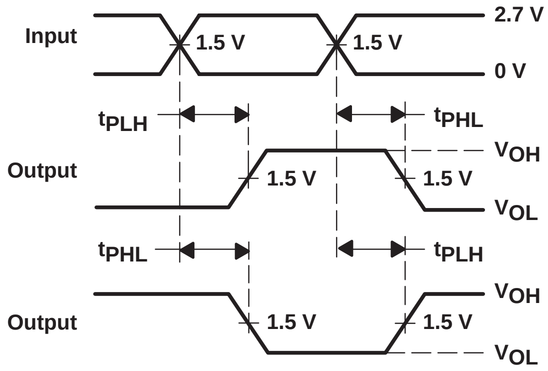
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



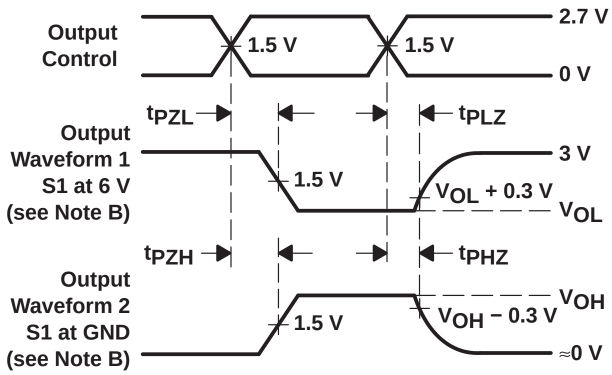


VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

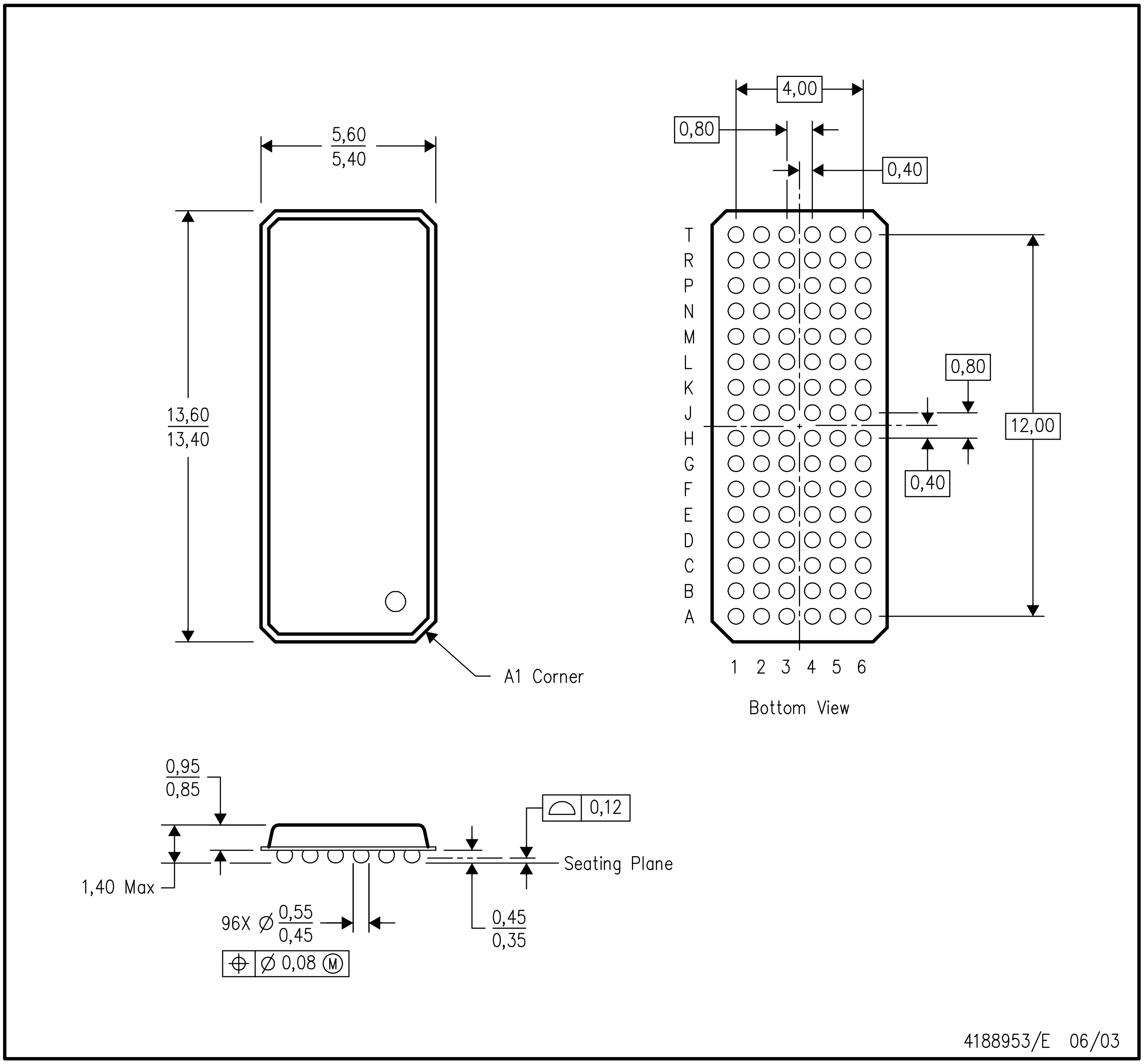


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

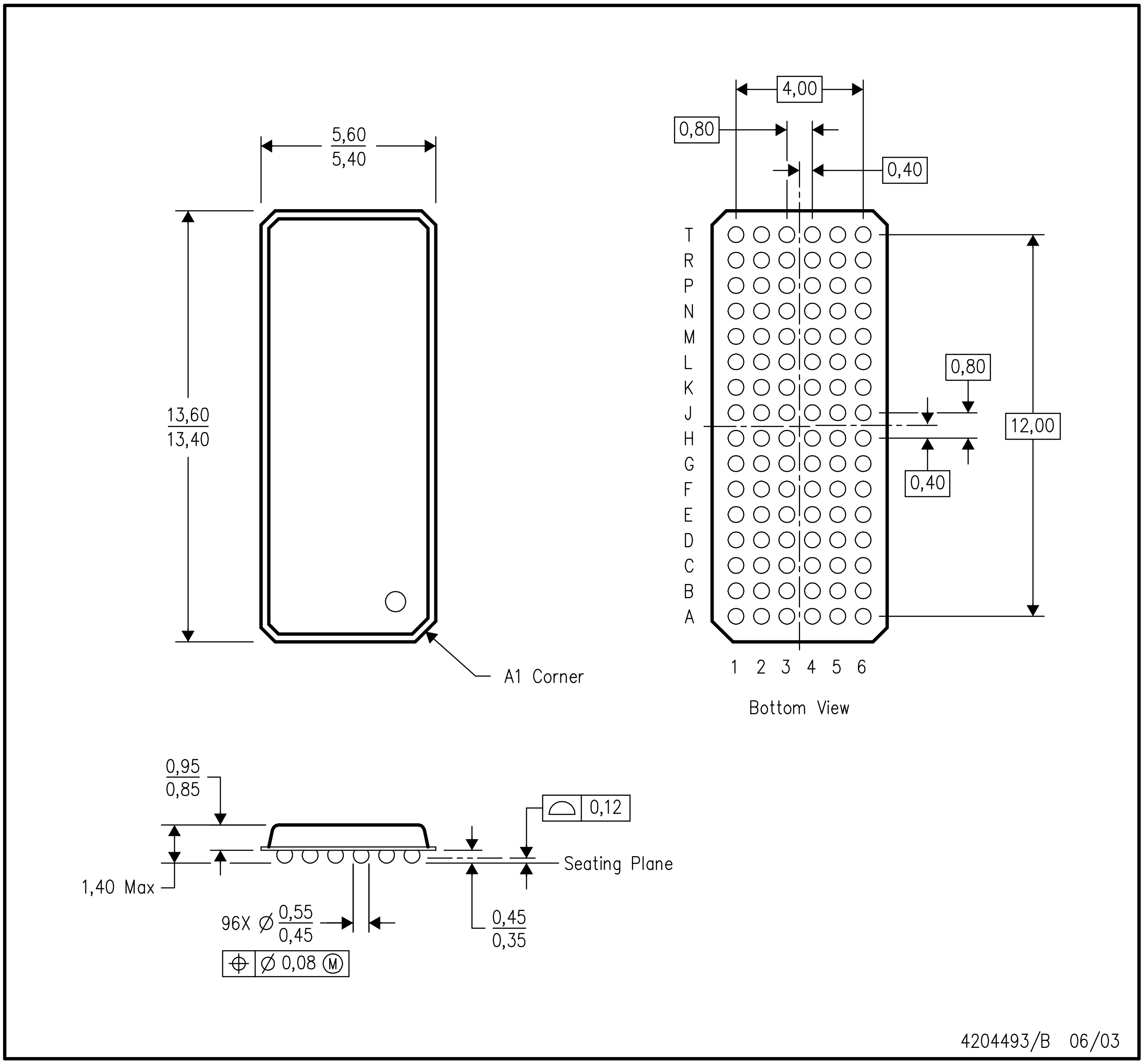
GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar BGA™ configuration
- D. Falls within JEDEC MO–205 variation CC.
- E. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

MicroStar BGA is a trademark of Texas Instruments.

ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar BGA™ configuration
- D. Falls within JEDEC MO–205 variation CC.
- E. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).

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