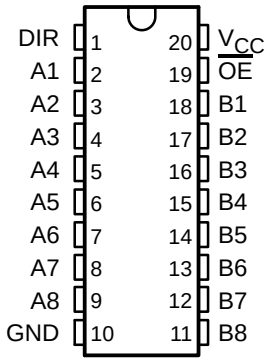
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Reduced Output Structure on A Port Minimizes V_{OHV}**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

NS PACKAGE
(TOP VIEW)



description/ordering information

This octal bus transceiver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVTR245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The A port is designed to minimize the undershoot exhibited on high-to-low transitions during simultaneous switching conditions.

ORDERING INFORMATION

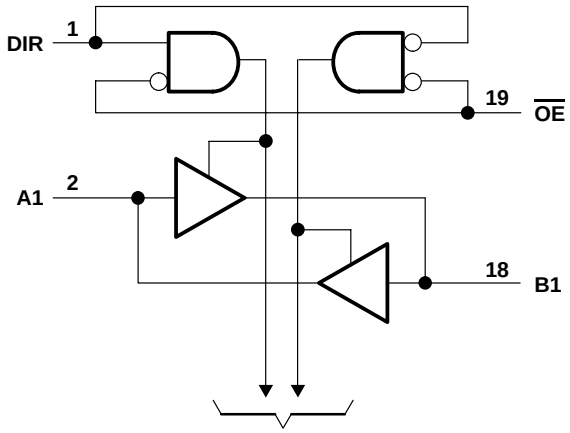
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOP – NS	Tape and reel	SN74LVTR245NSR	LVTR245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Current into any output in the low state, I_O . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2) . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current	B port		–32	mA
		A port		–12	
I_{OL}	Low-level output current			32	mA
I_{OL}†	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		–40	85	°C

† Current duty cycle ≤50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unlessotherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA	B port	V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = –8 mA	B port	2.4			
	V_{CC} = 3 V,	I_{OH} = –32 mA	B port	2			
	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA	A port	V_{CC}–0.2			
	V_{CC} = 2.7 V,	I_{OH} = –1 mA	A port	2.4			
	V_{CC} = 3 V	I_{OH} = –3 mA	A port	2.4			
		I_{OH} = –12 mA	A port	2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 24 mA				0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4	
		I_{OL} = 32 mA				0.5	
		I_{OL} = 64 mA				0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V	Control pins			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20	
		V_I = V_{CC}	A or B ports§			5	
		V_I = 0	A or B ports§			–5	
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			µA
		V_I = 2 V	A or B ports	–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1	µA
I_{CC}	V_{CC} = 3.6 V V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19	mA
			Outputs low		8.8	12	
			Outputs disabled		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V,	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	V_I = 3 V or 0				4		pF
C_{io}	V_O = 3 V or 0				10		pF

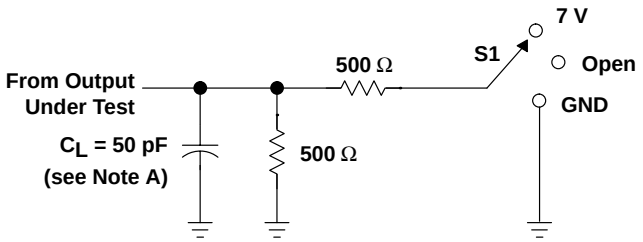
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	B	1.1	2.5	4.2		4.7	ns
	B	A	1.4	2.7	4.4		5.3	
t_{PHL}	A	B	1.1	2.6	4.6		5.8	ns
	B	A	1	2.3	4.1		5.1	
t_{PZH}	$\overline{OE}$	B	1.3	3.1	5.5		6.7	ns
		A	1.6	3.6	6		8.3	
t_{PZL}	$\overline{OE}$	B	2	3.9	6.6		8	ns
		A	1.8	3.8	6.4		7.6	
t_{PHZ}	$\overline{OE}$	B	2.7	4.2	6.1		6.7	ns
		A	2.5	4	5.8		6.4	
t_{PLZ}	$\overline{OE}$	B	2.4	3.7	5.2		5.4	ns
		A	2.4	3.7	5.2		5.3	

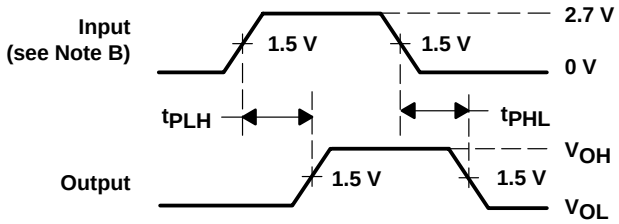
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

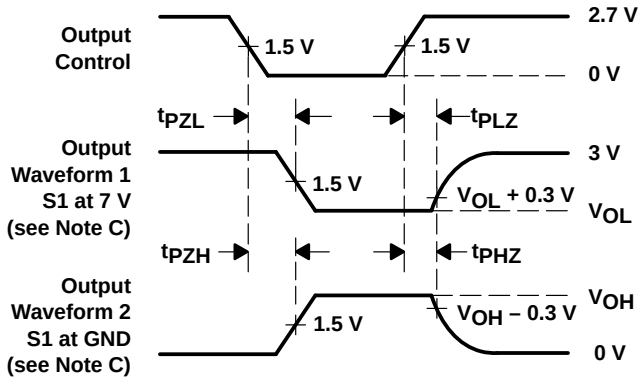


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



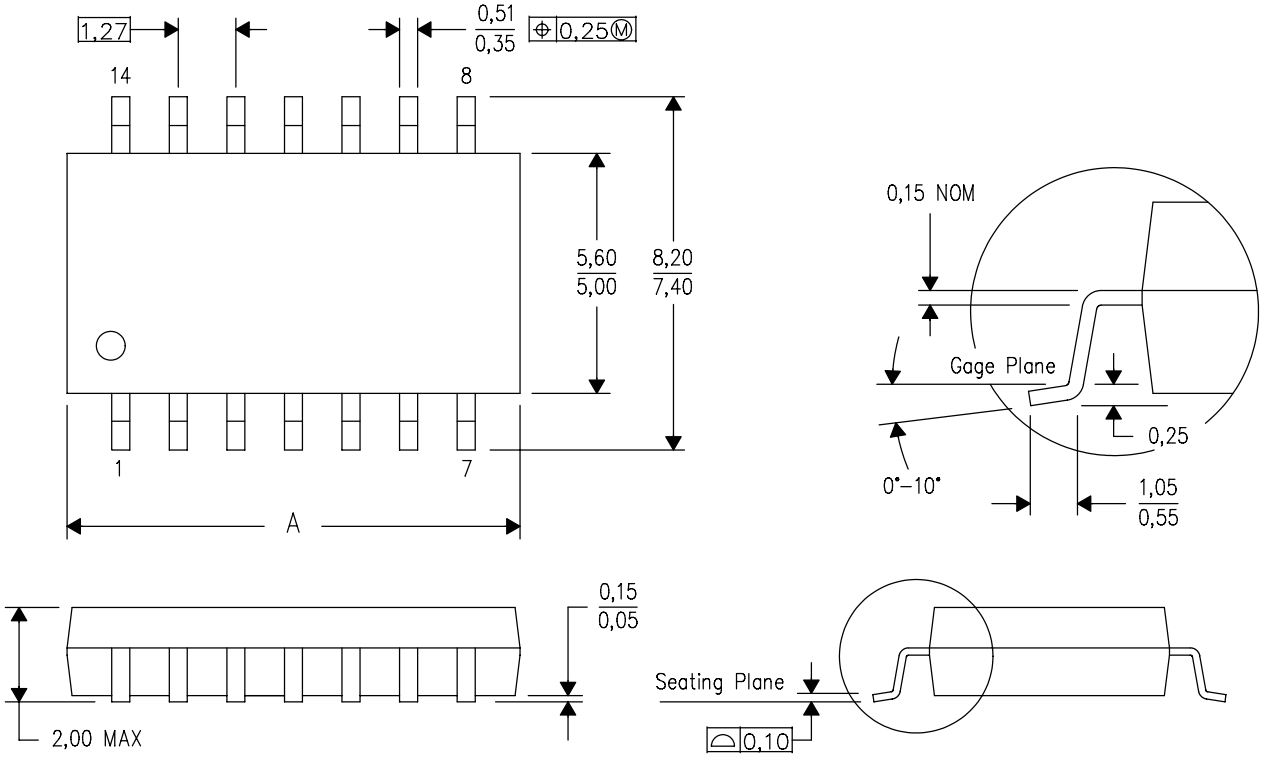
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

NS (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

14–PIN SHOWN



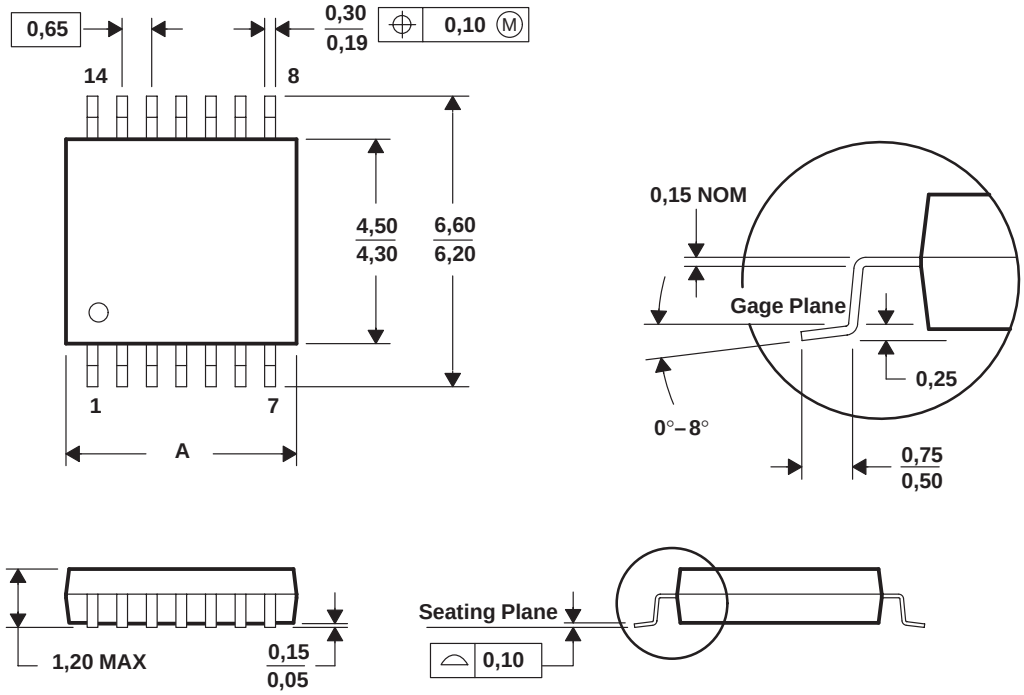
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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