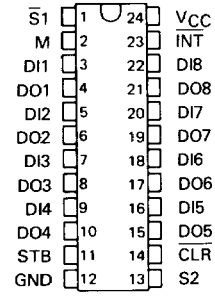
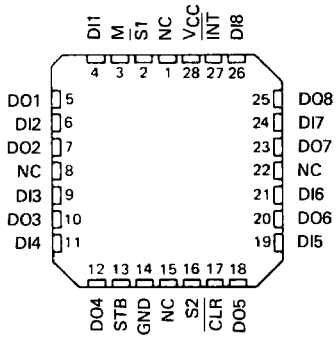
OCTOBER 1975–REVISED DECEMBER 1983

- PNP Inputs and 3-State Outputs Maximize I/O and Data Bus Capabilities
- Data Latch Transparency Permits Asynchronous or Latched Receiver Modes
- Mode and Select Inputs Permit Storing With Outputs Enabled or Disabled
- Strobe-Controlled Flag Flip-Flop Indicates Status or Interrupt
- Asynchronous Clear Sets All Eight Data Latches Low and Initializes Status Flag
- High-Level Output Voltage, Typically 4 V, Drives Most MOS Functions Directly
- Direct Replacement for Intel 3212 or 8212 in Most Applications

SN54S412 . . . J PACKAGE
SN74S412 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54S412 . . . FK PACKAGE
SN74S412 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The three-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides package busy or request interrupt commands. The outputs, with a 4-volt typical high-level voltage, are compatible for driving low-threshold MOS directly.

DATA LATCHES

The eight data latches are fully transparent when the internal gate enable, G, input is high and the outputs are enabled (OE = H). Latch transparency is selected by the mode control (M), select ($\overline{S1}$ and S2), and the strobe (STB) inputs and during transparency each data output (DO_i) follows its respective data input (DI_i). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See data latches function table.

MODE SELECTION

An input mode or an output mode is selectable from this single input line. In the input mode, MD = L, the eight data latch inputs are enabled when the strobe is high regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S1}$ and S2) inputs. See data latches function table.

STATUS FLIP-FLOP

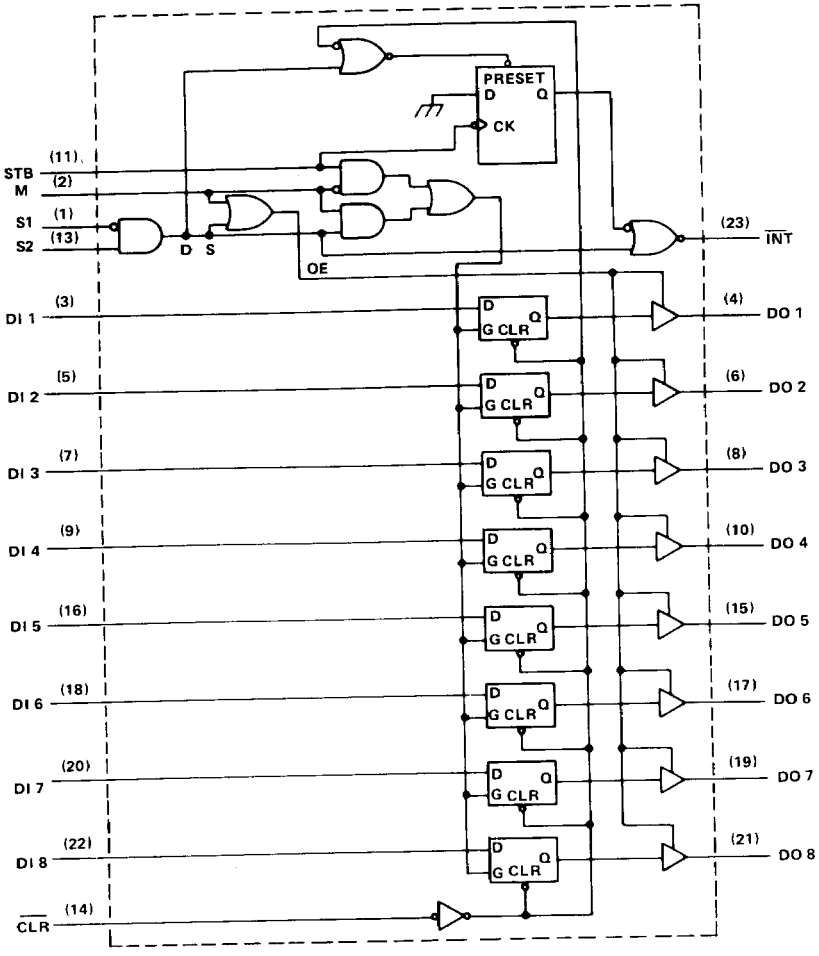
The status flip-flop provides a low-level output signal when:

a. the package is selected

b. a strobe input is received.

This status signal can be used to indicate that the register is busy or to initiate an interrupt type command.

logic diagram



Pin numbers shown on logic notation are for DW, J or N packages.

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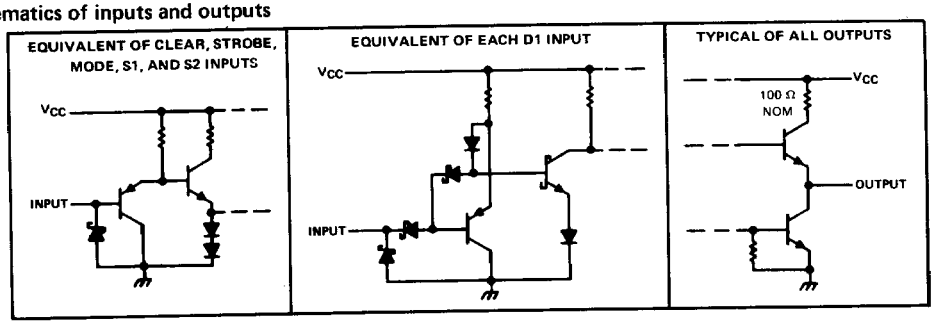
schematics of inputs and outputs



DATA LATCHES FUNCTION TABLE

FUNCTION	CLEAR	M	$\overline{S1}$	S2	STB	DATA IN	DATA OUT
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q_O
	H	L	L	H	L	X	Q_O
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

STATUS FLIP-FLOP FUNCTION TABLE

CLEAR	$\overline{S1}$	S2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H ≡ high level (steady state)
L ≡ low level (steady state)
X ≡ irrelevant (any input, including transitions)
Z ≡ high impedance (off)
↓ ≡ transition from low to high level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S412 . . . . . −55°C to 125°C
SN74S412 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S412			SN74S412			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Pulse width, t_w (see Figures 1, 2, and 4)	STB or $\overline{S1}$ • S2	25			25			ns
	Clear low	25			25			
Setup time, t_{su} (see Figure 3)		15↓			15↓			ns
Hold time, t_h (see Figures 1 and 3)		20↓			20↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S412			SN74S412			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.85			0.85	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = −1 mA	3.4	4		3.65	4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.85 V	I_{OL} = 15 mA			0.45			0.45	V
				I_{OL} = 20 mA			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 5.25 V			20			10	μA
I_{IL}	Low-level input current	$\overline{S1}$	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
		M					−0.75			−0.75	
		All others					−0.25			−0.25	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−65	−20		−65	mA
I_{CC}	Supply current		V_{CC} = MAX,	see Note 2		82			82	130	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear input at 4.5 V, and all other inputs grounded.

3

TTL DEVICES

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	STB, $\overline{S1}$, or S2	Any DO	1	C_L = 30 pF, See Note 3		18	27	ns
t_{PHL}						15	25	
t_{PHL}	$\overline{CLR}$	Any DO	2			18	27	ns
t_{PLH}	DI_i	DO_i	3			12	20	ns
t_{PHL}						10	20	
t_{PLH}	$\overline{S1}$ or S2	$\overline{INT}$	4	C_L = 30 pF, See Note 3		12	20	ns
t_{PHL}	STB	$\overline{INT}$	4			16	25	
t_{PZH}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 30 pF, See Note 3		21	35	ns
t_{PZL}						25	40	
t_{PHZ}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 5 pF, See Note 3		9	20	ns
t_{PLZ}						12	20	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3: See General Information Section for load circuits and voltage waveforms.

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PARAMETER MEASUREMENT INFORMATION

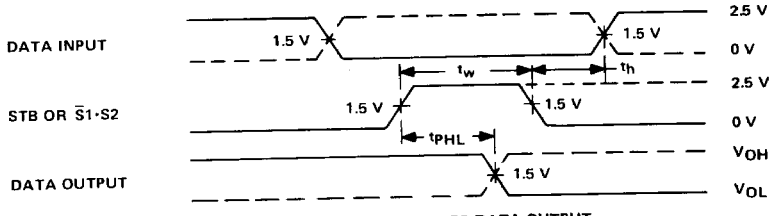

FIGURE 1 – STROBE OR SELECT TO DATA OUTPUT

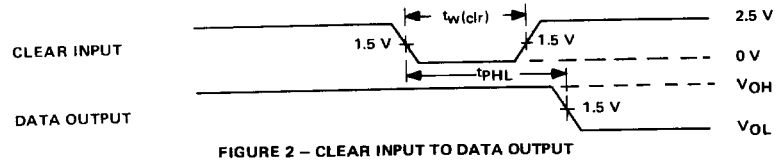

FIGURE 2 – CLEAR INPUT TO DATA OUTPUT

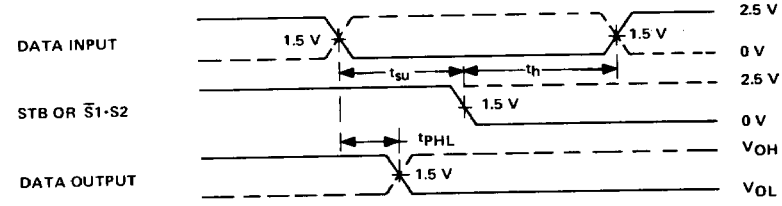

FIGURE 3 – DATA INPUT TO DATA OUTPUT

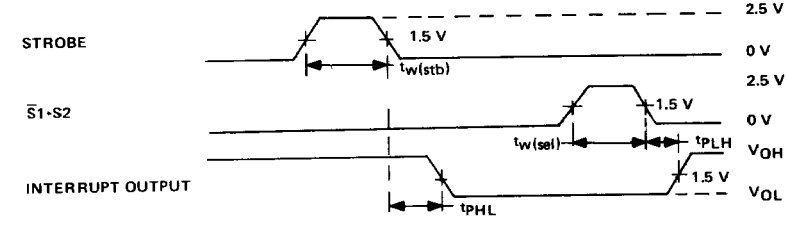

FIGURE 4 – STROBE OR SELECT TO INTERRUPT OUTPUT

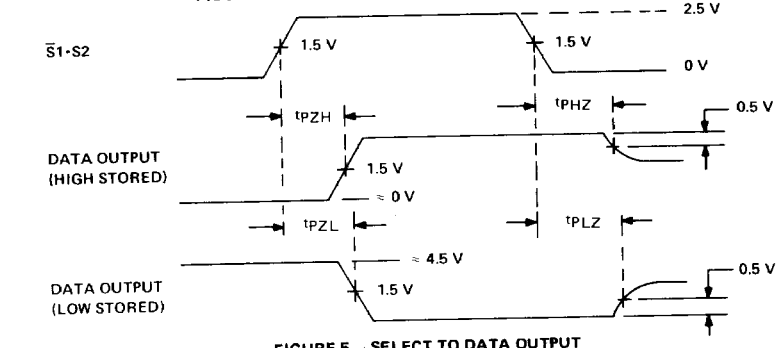

FIGURE 5 – SELECT TO DATA OUTPUT