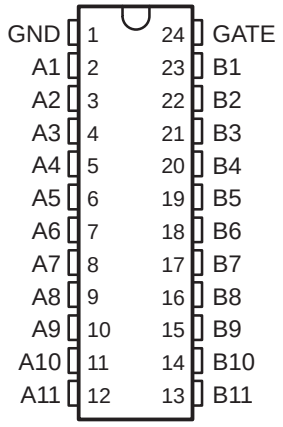
SCDS088A – APRIL 1999 – REVISED JUNE 1999

- **Designed to be Used in Voltage-Limiting Applications**
- **6.5-Ω On-State Connection Between Ports A and B**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Direct Interface With GTL+ Levels**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

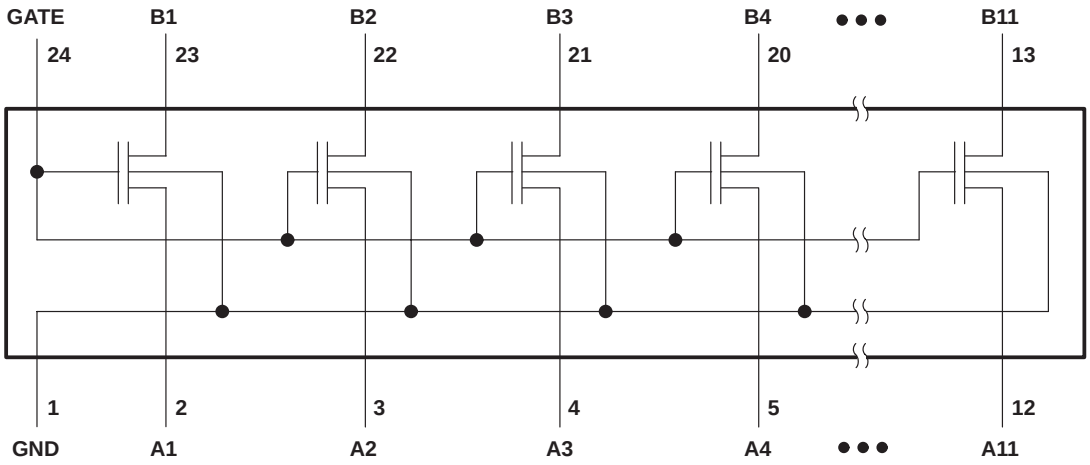
The SN74TVC3010 provides 11 parallel NMOS pass transistors with a common gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a 10-bit switch with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots. (See Application Information in this data sheet.)

All of the transistors in the TVC array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Since, within the device, the characteristics from transistor-to-transistor are equal, the maximum output high-state voltage (V_{OH}) will be approximately the reference voltage (V_{REF}), with minimum deviation from one output to another. This is a large benefit of the TVC solution over discrete devices. Because the fabrication of the transistors is symmetrical, either port connection of each bit can be used as the low-voltage side, and the I/O signals are bidirectional through each FET.

The SN74TVC3010 is characterized for operation from –40°C to 85°C.

simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBQ package . . . . . 103°C/W
DGV package . . . . . 139°C/W
DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	TYP	MAX	UNIT
$V_{I/O}$	Input/output voltage	0		5	V
V_{GATE}	GATE voltage	0		5	V
I_{PASS}	Pass-transistor current		20	64	mA
T_A	Operating free-air temperature	–40		85	°C

application operating conditions (see Figure 2)

		MIN	TYP	MAX	UNIT
V_{BIAS}	BIAS voltage	3	3.3	3.6	V
V_{REF}	Reference voltage	1.365	1.5	1.635	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	0		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

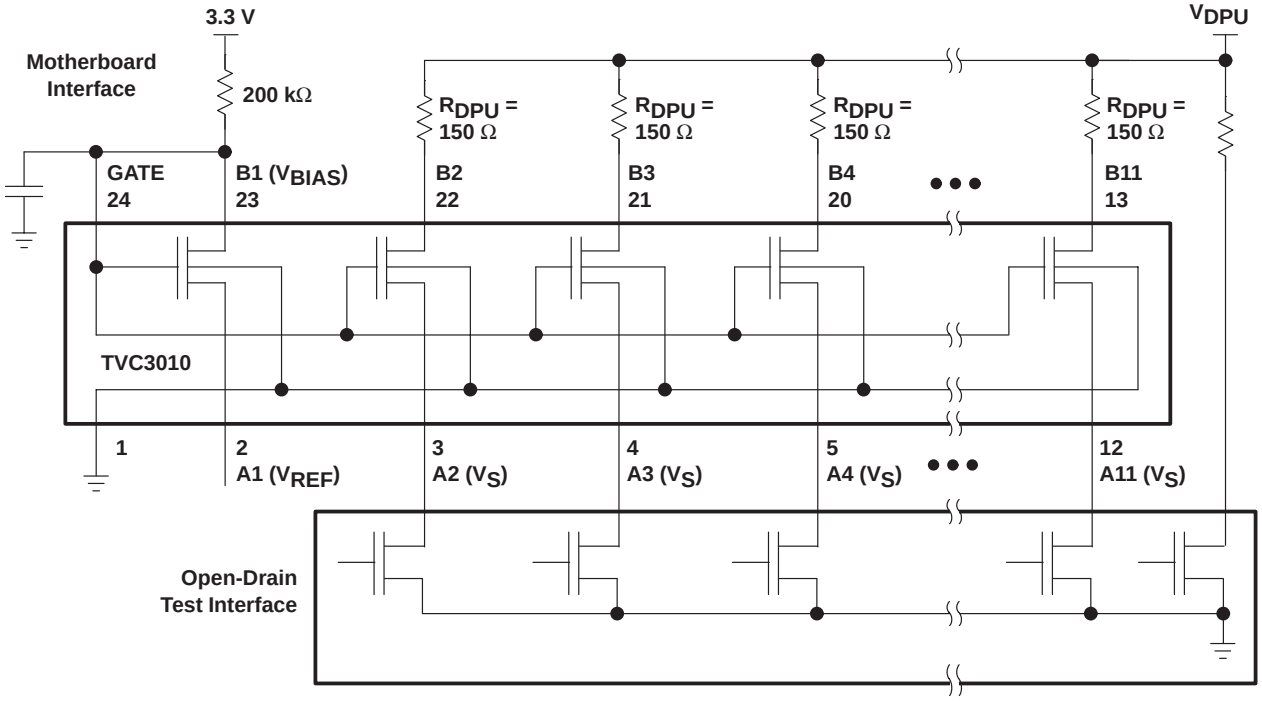
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{BIAS} = 0,	I_I = –18 mA				–1.2	V
V_{OL}	I_{REF} = 5 μA, V_{DPU} = 2.625 V,	V_{REF} = 1.365 V, R_{DPU} = 150 Ω,	V_S = 0.175 V, (see Figure 1)			350	mV
$C_{i(GATE)}$	V_I = 3 V or 0				24		pF
$C_{io(OFF)}$	V_O = 3 V or 0				4	12	pF
$C_{io(ON)}$	V_O = 3 V or 0				12	30	pF
r_{on}‡	I_{REF} = 5 μA, V_{DPU} = 2.625 V,	V_{REF} = 1.365 V, R_{DPU} = 150 Ω,	V_S = 0.175 V, (see Figure 1)			12.5	Ω

† All typical values are at T_A = 25°C.
‡ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

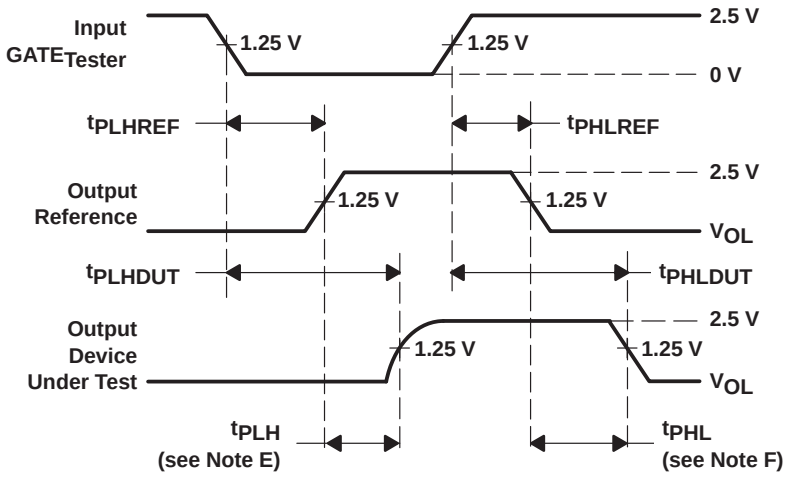
switching characteristics over recommended operating free-air temperature range, V_{DPU} = 2.36 V to 2.64 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A or B	B or A	0	4	ns
t_{PHL}			0	4	

PARAMETER MEASUREMENT INFORMATION



TESTER CALIBRATION SETUP (see Note D)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. Test procedure: t_{PLHREF} and t_{PHLREF} are obtained by measuring the propagation delay of a reference measuring point. t_{PLHDUT} and t_{PHLDUT} are obtained by measuring the propagation delay of the device under test.
E. $t_{PLH} = t_{PLHDUT} - t_{PLHREF}$
F. $t_{PHL} = t_{PHLDUT} - t_{PHLREF}$

Figure 1. Tester Calibration Setup and Voltage Waveforms

APPLICATION INFORMATION

TVC background information

In personal computer (PC) architecture there are industry-accepted bus standards. These standards define, among other things, the I/O voltage levels at which the bus communicates. Examples include the GTL+ host bus, the AGP graphics port, and the PCI local bus. In new designs, the system components must communicate with existing bus infrastructure. Providing an evolutionary upgrade path is important in the design of PC architecture, but the existing bus standards must be preserved.

To achieve the ever-present needs for smaller, faster, lighter devices that draw less power, yet have faster performance, most new high-performance digital integrated circuits are being designed and produced with advanced submicron semiconductor process technologies. These devices have thin gate-oxide or short channel lengths and very low absolute-maximum voltages that can be tolerated at the inputs/outputs (I/Os) without causing damage. In many cases, the I/Os of these devices are not tolerant of the high-state voltage-levels on the pre-existing buses with which they must communicate. Therefore, the need arose for protection of the I/Os of devices by limiting the I/O voltages.

The Texas Instruments (TI™) Translation Voltage Clamp (TVC) family was designed for the specific application of protecting sensitive I/Os (see Figure 2). The information in this data sheet describes the I/O protection application of the TVC family and should enable the design engineer to successfully implement an I/O protection circuit utilizing the TI TVC solution.

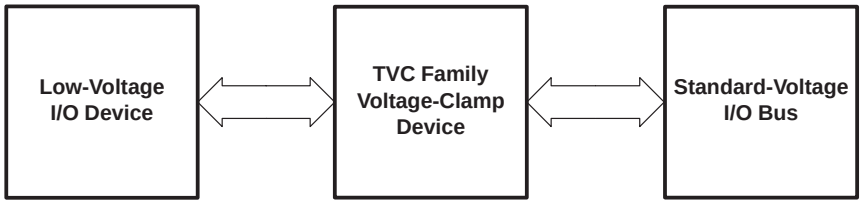
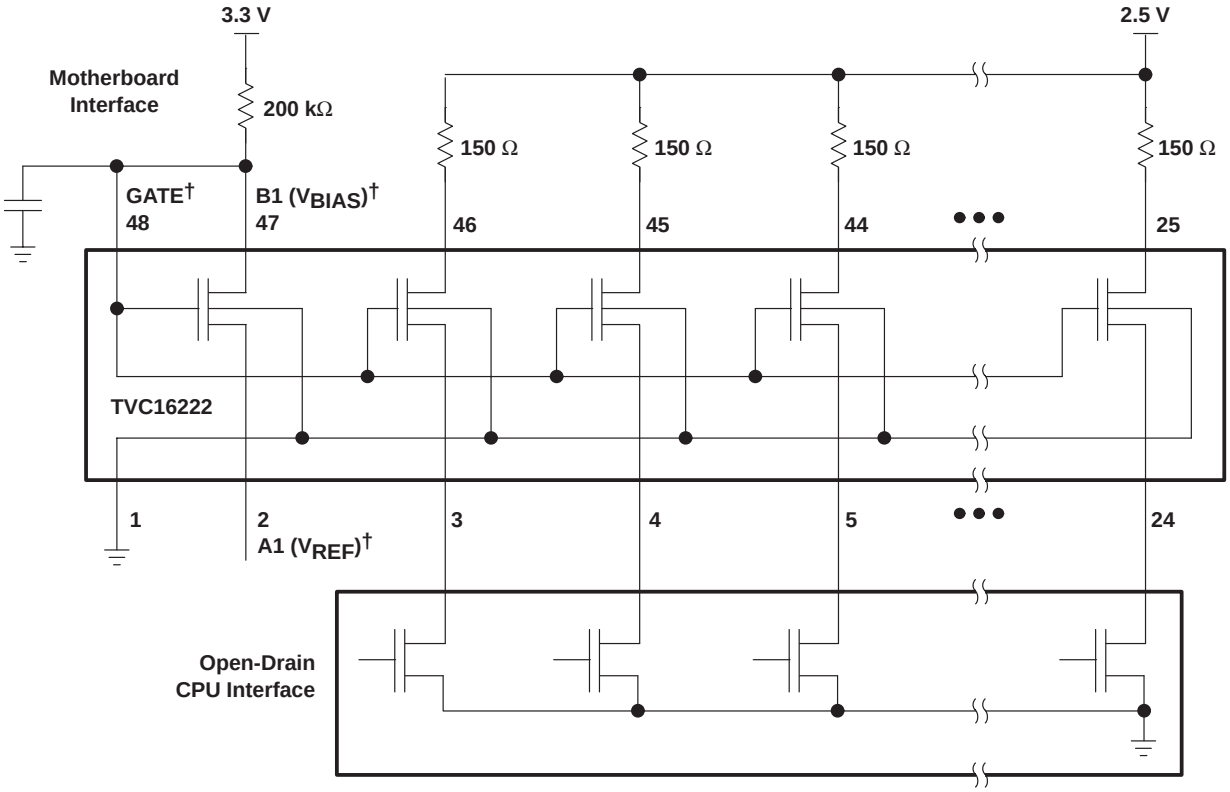


Figure 2. Thin Gate-Oxide Protection Application

APPLICATION INFORMATION

TVC voltage-limiting application

For the voltage-limiting configuration, the common GATE input must be connected to one side (A or B) of any one of the transistors (see Figure 3). This connection determines the V_{BIAS} input of the reference transistor. The V_{BIAS} input is connected through a pullup resistor (typically, 200 kΩ) to the V_{DD} supply. A filter capacitor on V_{BIAS} is recommended. The opposite side of the reference transistor is used as the reference voltage (V_{REF}) connection. The V_{REF} input must be less than V_{DD} – 1 V to bias the reference transistor into conduction. The reference transistor regulates the gate voltage (V_G) of all the pass transistors. V_G is determined by the characteristic gate-to-source voltage difference (V_{GS}) because $V_G = V_{REF} + V_{GS}$. The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of $V_G – V_{GS}$, or V_{REF}.



† V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS}.

Figure 3. Typical Application Circuit

APPLICATION INFORMATION

electrical characteristics

The electrical characteristics of the NMOS transistors used in the TVC devices are illustrated by TI SPICE simulations. Figure 4 shows the test configuration for the TI SPICE simulations. The results, shown in Figures 5 and 6, show the current through a pass transistor, versus the voltage at the source for different reference voltages. The plots of the dc characteristics clearly reveal that the device clamps at the desired reference voltage for the varying device environments.

Figure 5 shows the V-I characteristics, with low reference voltages and a reference-transistor drain-supply voltage of 3.3 V. To further investigate the spread of the V-I characteristic curves, V_{REF} was held at 2.5 V and I_{REF} was increased by raising V_{DDREF} (see Figure 6). The result was a tighter grouping of the V-I curves.

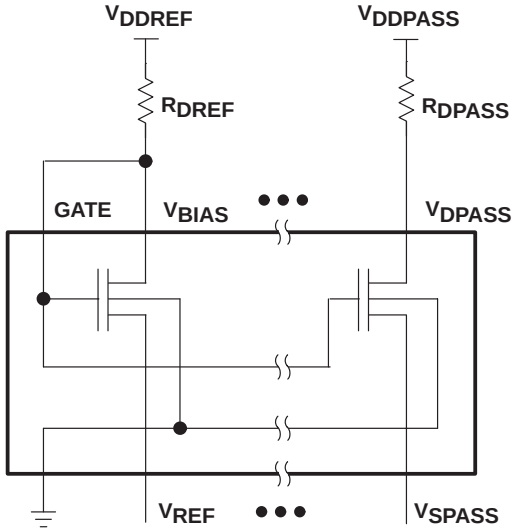


Figure 4. TI SPICE Simulation Schematic and Voltage-Node Names

APPLICATION INFORMATION

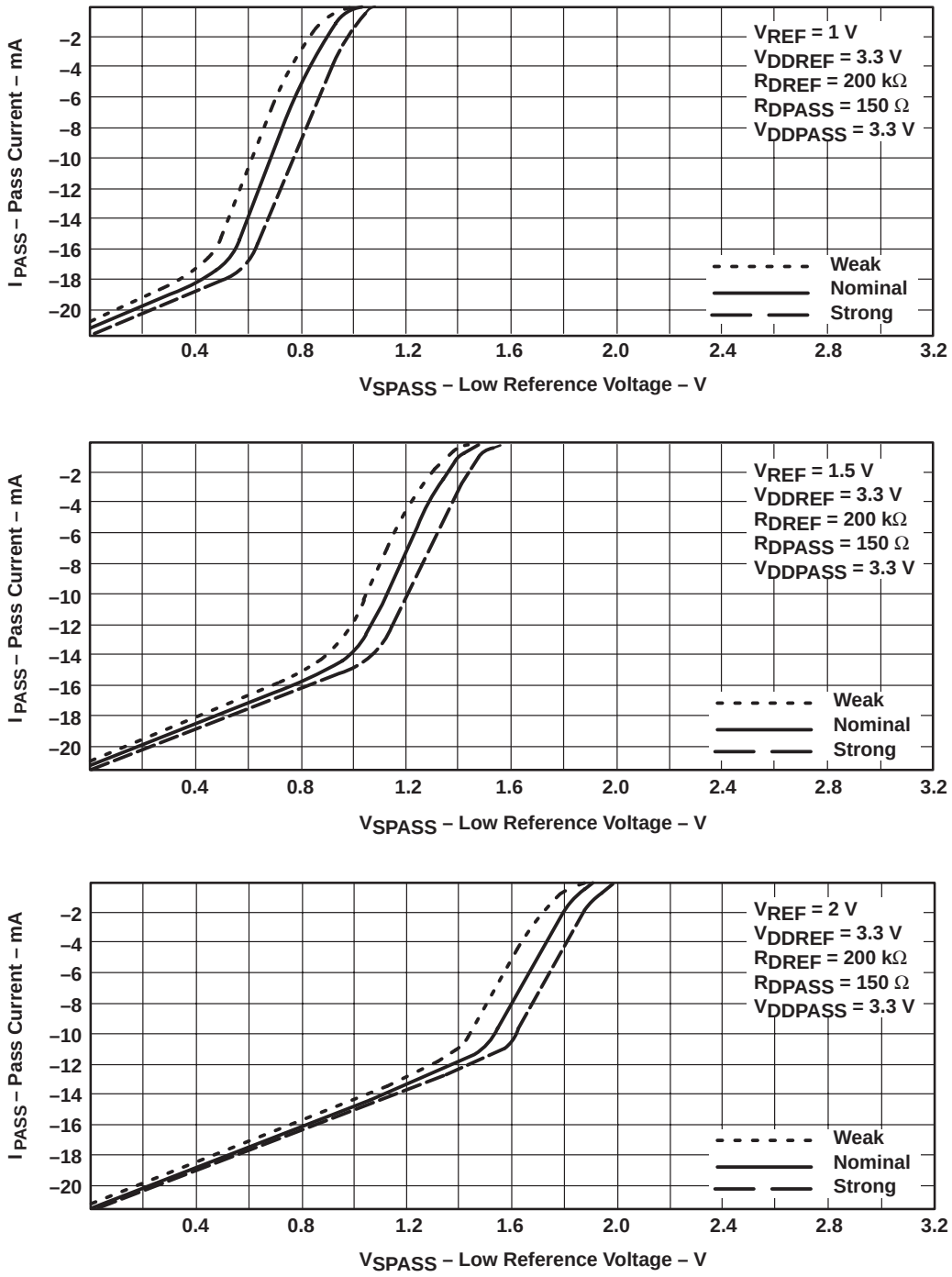


Figure 5. Electrical Characteristics at Low V_{REF} Voltages

APPLICATION INFORMATION

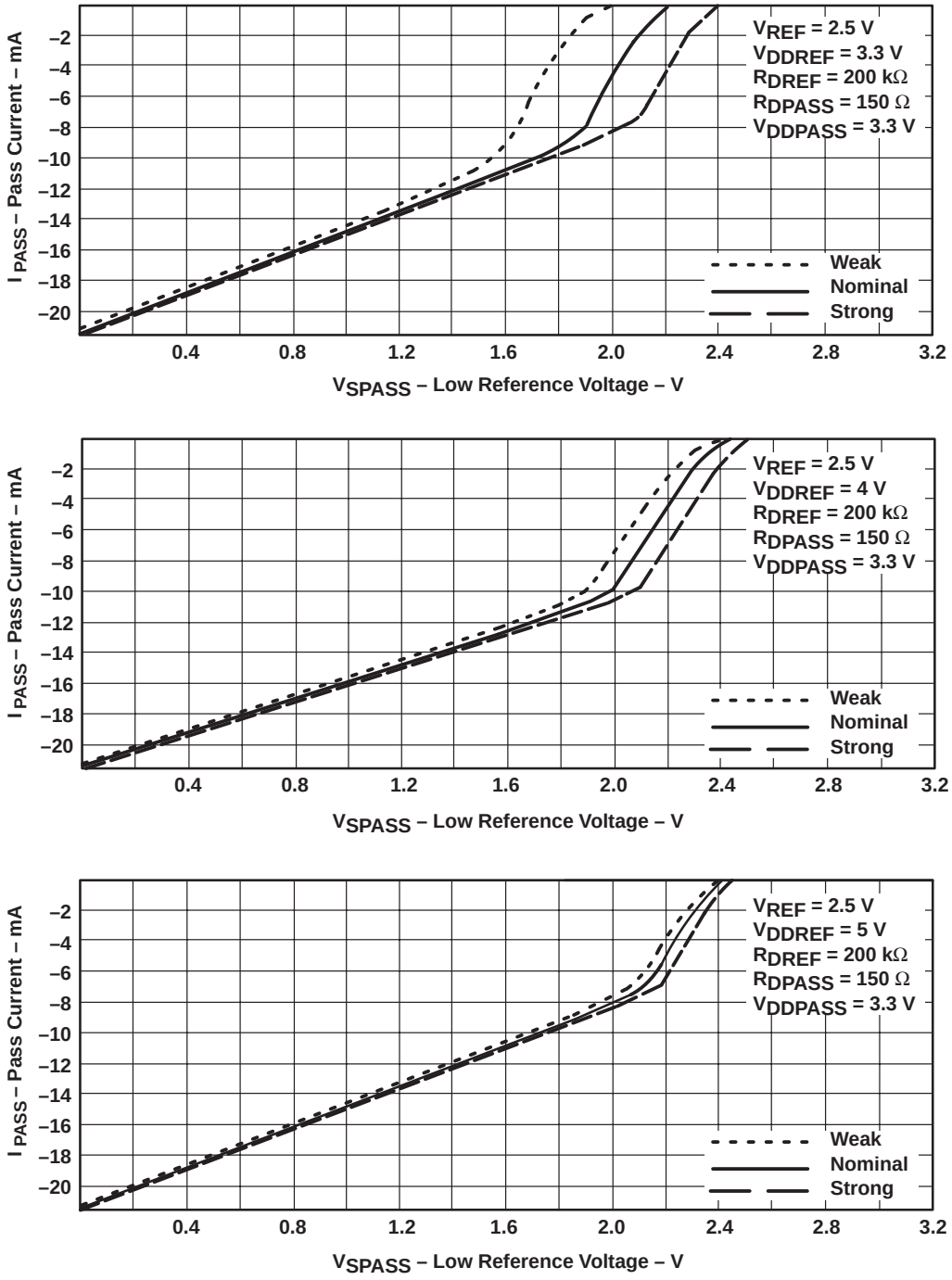


Figure 6. Electrical Characteristics at V_{REF} = 2.5 V

APPLICATION INFORMATION

features and benefits

The TVC family has several features that benefit a system designer when implementing a sensitive I/O protection solution. Table 1 lists these features and their associated benefits.

Table 1. Features and Benefits

FEATURES	BENEFITS
Any FET can be used as the reference transistor	Ease of layout
All FETs on one die, tight process control	Very low spread of V_O relative to V_{REF}
No active control logic (passive device)	No logic power supply (V_{CC}) required
Flow-through pinout	Ease of trace routing
Devices offered in different bit-widths and packages	Optimizes design and cost effectiveness
Designer flexibility with V_{REF} input	Allows migration to lower-voltage I/Os without board redesign

conclusion

The TI TVC family provides the designer with a solution for protection of circuits with I/Os that are sensitive to high-state voltage-level overshoots. The flexibility of TVC enables a low-voltage migration path for advanced designs to align with industry standards.

frequently asked questions (FAQ)

1. Q: Can any of the transistors in the array be used as the reference transistor?

   A: Yes, any transistor can be used as long as its V_{BIAS} pin is connected to the GATE pin.

2. Q: In the recommended operating conditions table of the data sheet, the typical V_{BIAS} is 3.3 V. Should V_{BIAS} be equal to or greater than V_{REF} on the reference transistor?

   A: V_{BIAS} is a variable that is determined by V_{REF}. V_{BIAS} is connected to V_{DD} through a resistor to allow the bias voltage to be controlled by V_{REF}. V_{DD} can be as high as 5.5 V. V_{REF} needs to be at least 1 V less than V_{BIAS} on the reference transistor.

3. Q: Do both A and B ports have 5-V I/O tolerance or is 5-V I/O tolerance provided only on the low-voltage side?

   A: Both ports are 5-V tolerant.

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