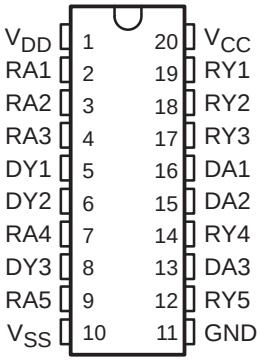
- **Single Chip With Easy Interface Between UART and Serial Port Connector of IBM PC/AT™ and Compatibles**
- **Three Drivers and Five Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Designed to Support Data Rates Up To 120 kbps**
- **ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 5 kV on All Other Pins (Human-Body Model)**
- **Pinout Compatible With the SN75C185**

DW OR N PACKAGE
(TOP VIEW)



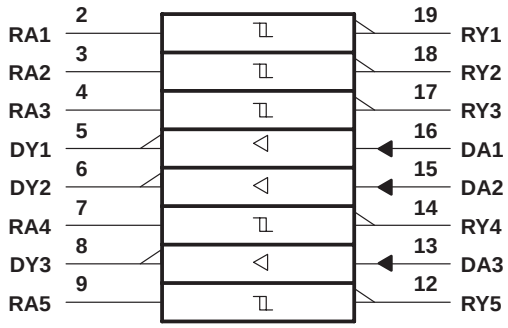
description

The SN75185 combines three drivers and five receivers from TI trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provides a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The SN75185 complies with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU v.10) and TIA/EIA-422-B (ITU v.11) standards are recommended.

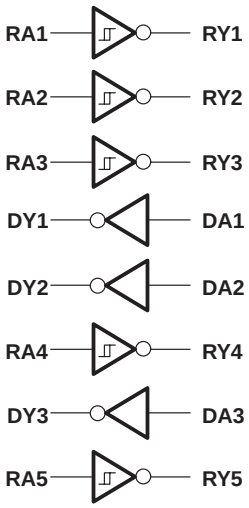
The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

logic symbol†

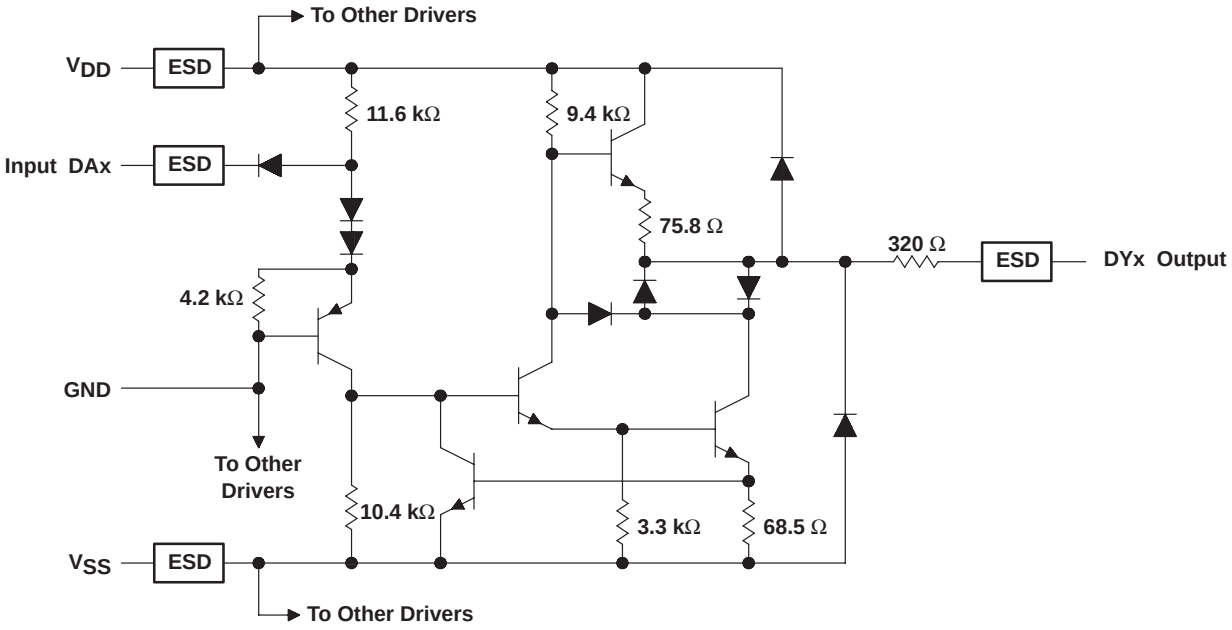


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

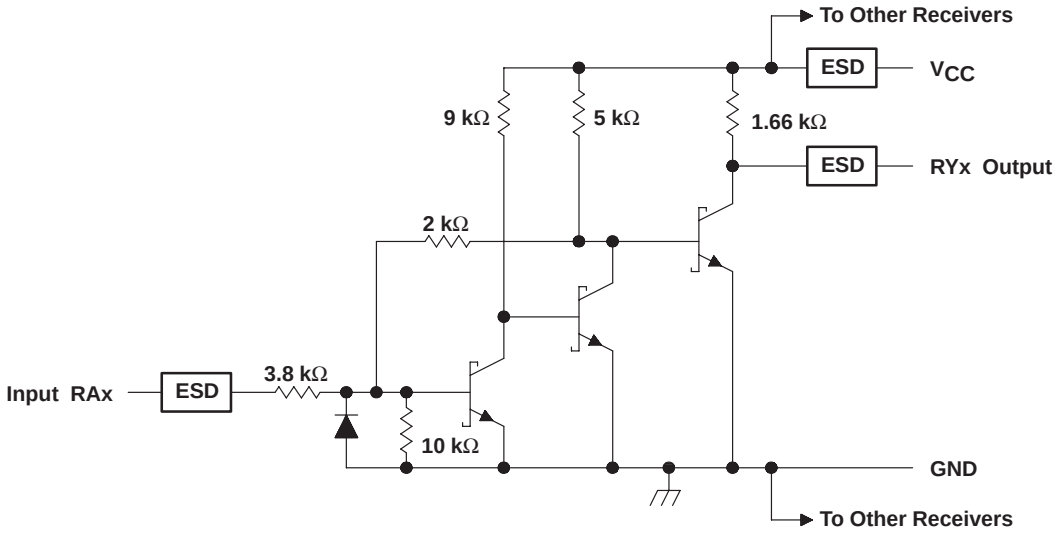


schematic of drivers



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 10 V
Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{SS} (see Note 1) . . . . . –15 V
Input voltage range: Driver . . . . . –15 V to 7 V
Receiver . . . . . –30 V to 30 V
Driver output voltage range . . . . . –15 V to 15 V
Receiver low-level output current . . . . . 20 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 97°C/W
N package . . . . . 67°C/W
Electrostatic discharge: Human-body model: RS-232 pins, class 3, A (see Note 3) . . . . . 10 kV
Human-body model: All pins, class 3, A (see Note 4) . . . . . 5 kV
Machine model: RS-232 pins, class 3, B (see Note 5) . . . . . 600 V
Machine model: All pins, class 3, B (see Note 4) . . . . . 300 V
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.
3. RS-232 pins are tested with respect to ground and each other.
4. Per MIL-PRF–38535
5. RS-232 pins are tested with respect to ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	15	V
Supply voltage, V_{SS}		–7.5	–9	–15	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH} (driver only)		1.9			V
Low-level input voltage, V_{IL} (driver only)				0.8	V
High-level output current, I_{OH}	Driver			–6	mA
	Receiver			–0.5	
Low-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V, V_{SS} = –9 V		15	mA
				V_{DD} = 12 V, V_{SS} = –12 V		19	
				V_{DD} = 15 V, V_{SS} = –15 V		25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V, V_{SS} = –9 V		4.5	mA
				V_{DD} = 12 V, V_{SS} = –12 V		5.5	
				V_{DD} = 15 V, V_{SS} = –15 V		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V, V_{SS} = –9 V		–15	mA
				V_{DD} = 12 V, V_{SS} = –12 V		–19	
				V_{DD} = 15 V, V_{SS} = –15 V		–25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V, V_{SS} = –9 V		–3.2	mA
				V_{DD} = 12 V, V_{SS} = –12 V		–3.2	
				V_{DD} = 15 V, V_{SS} = –15 V		–3.2	
I_{CC}	Supply current from V_{CC}	V_{CC} = 5 V,	All inputs at 5 V,	No load		30	mA

DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 9 V, V_{SS} = –9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 6)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		–7.5	–6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	µA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				–1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 7)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	–4.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	12	19.5	mA
r_o	Output resistance (see Note 8)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = –2 V to 2 V	300			Ω

NOTES: 6. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if –10 V is maximum, the typical value is a more negative voltage).
7. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
8. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output			75	175	ns
t_{TLH}	Transition time, low-to-high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		60	100	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3 and Note 9		1.7	2.5	µs
t_{THL}	Transition time, high-to-low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		40	75	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3 and Note 10		1.5	2.5	µs

NOTES: 9. Measured between –3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied.
10. Measured between 3-V and –3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70 °C	1.55		2.3	
V_{T-}	Negative-going threshold voltage			0.75	0.97	1.25	
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5			
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level input voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level output current	V_I = –25 V,	See Figure 5	–3.6		–8.3	mA
		V_I = –3 V,	See Figure 5	–0.43			
I_{OS}	Short-circuit output current	See Figure 4			–3.4	–12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = –9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Figure 6	R_L = 5 kΩ		107	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output				42	150	ns
t_{TLH}	Transition time, low-to-high-level output				175	525	ns
t_{THL}	Transition time, high-to-low-level output				16	60	ns

PARAMETER MEASUREMENT INFORMATION

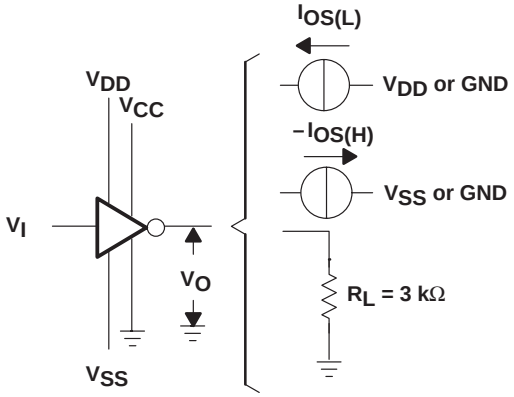


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

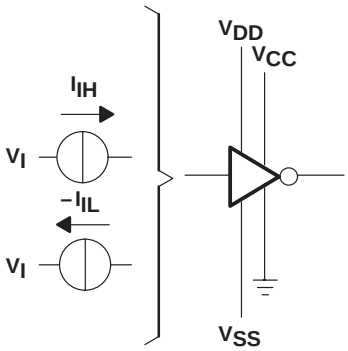
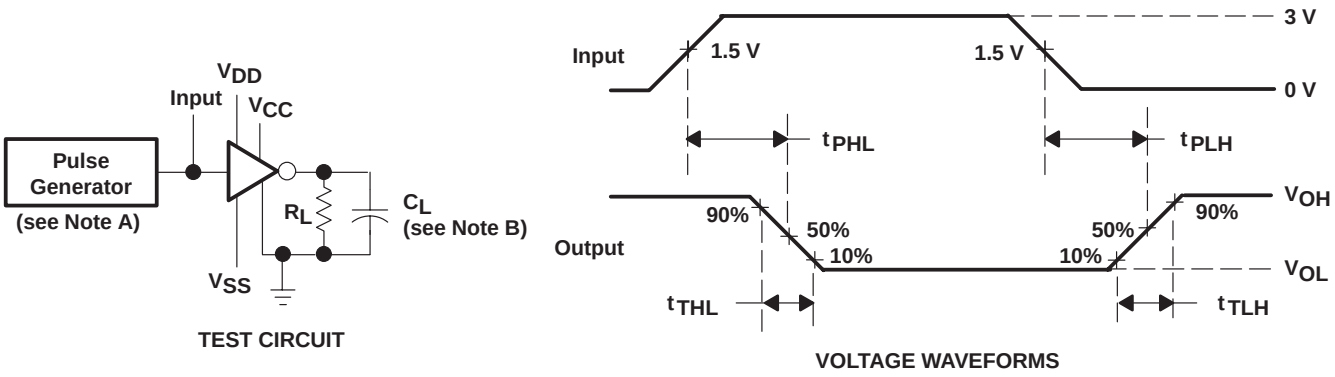


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

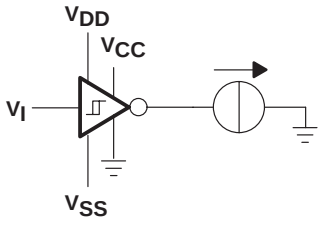


Figure 4. Receiver Test Circuit for I_{OS}

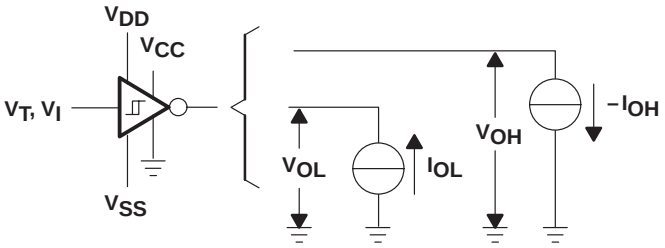
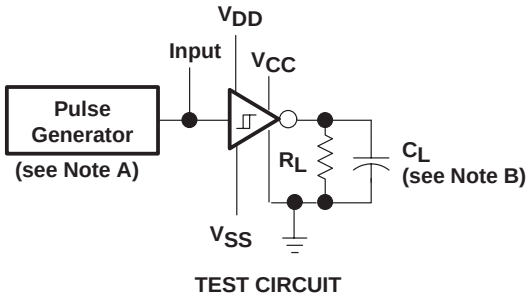
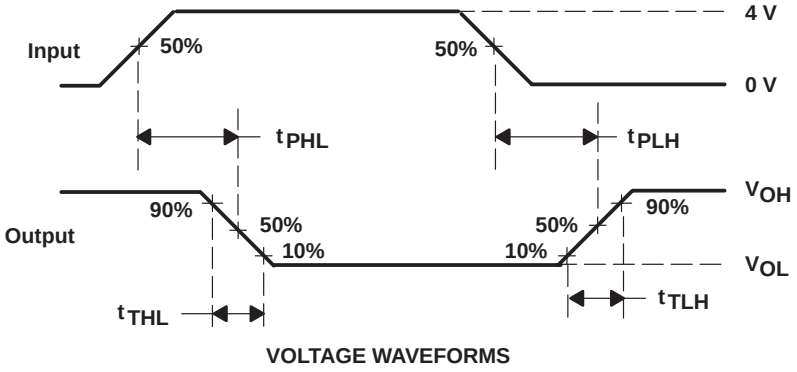


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}





NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

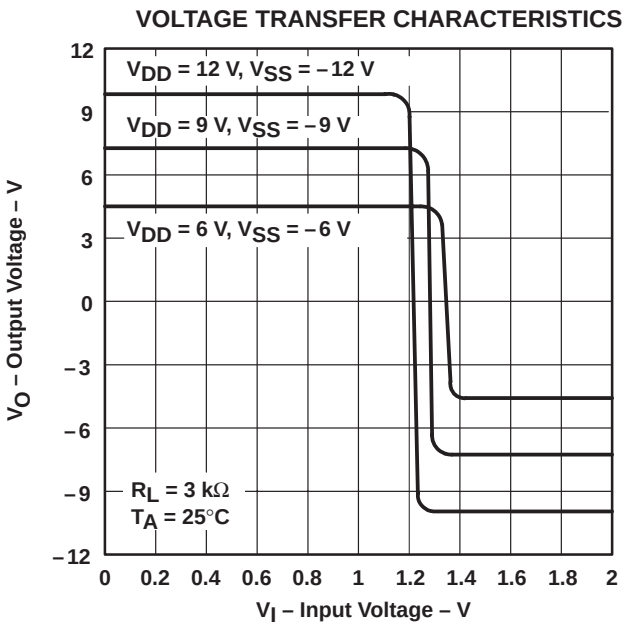


Figure 7

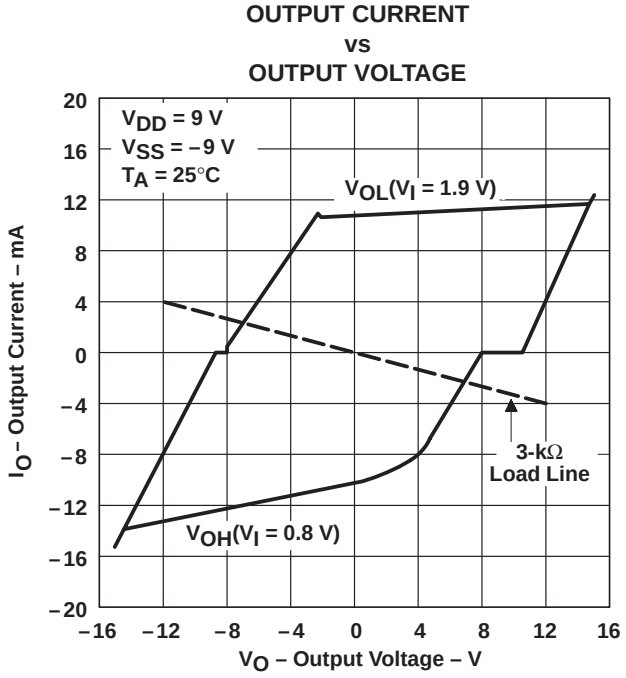


Figure 8

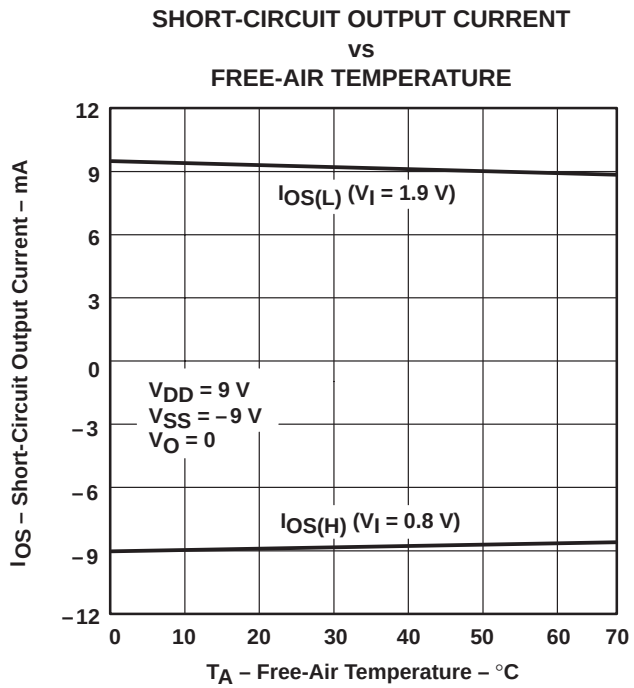


Figure 9

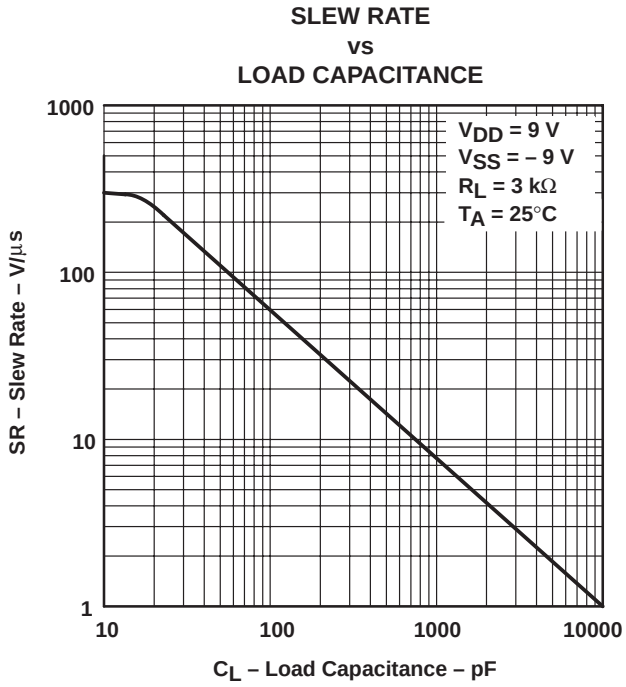


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER SECTION

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

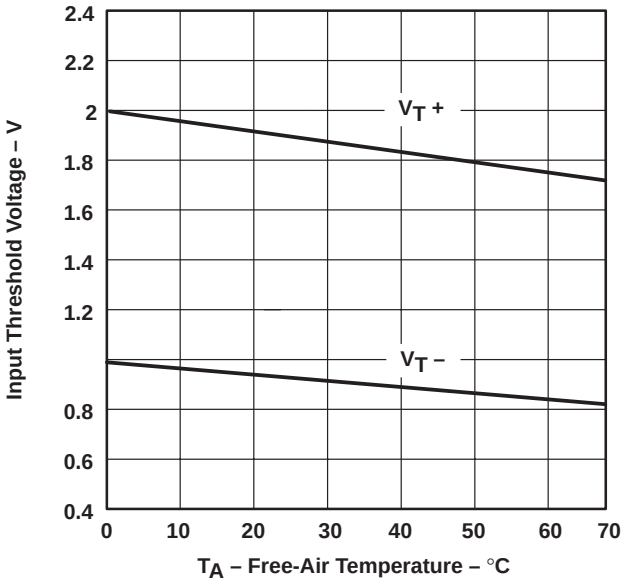


Figure 11

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

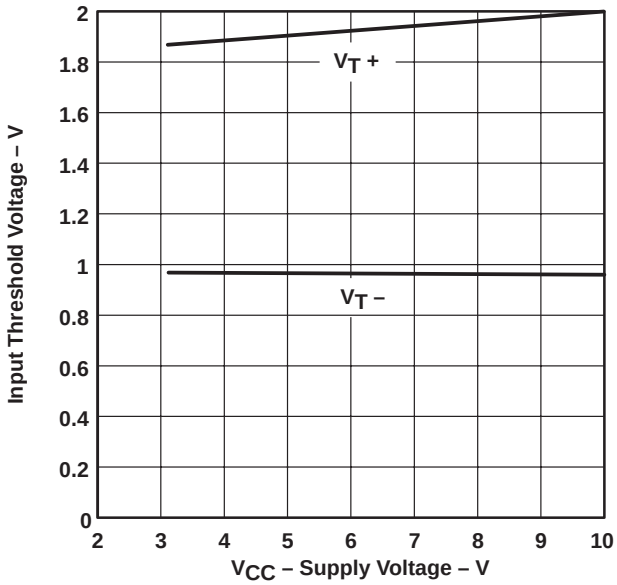
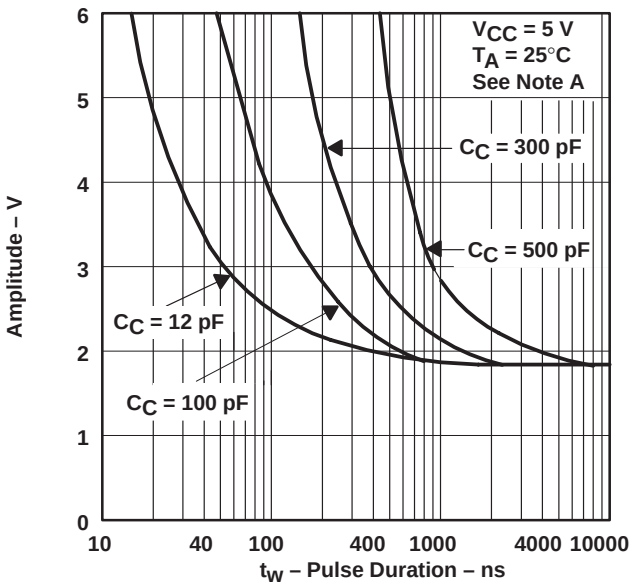


Figure 12

NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13

MAXIMUM SUPPLY VOLTAGE vs FREE-AIR TEMPERATURE

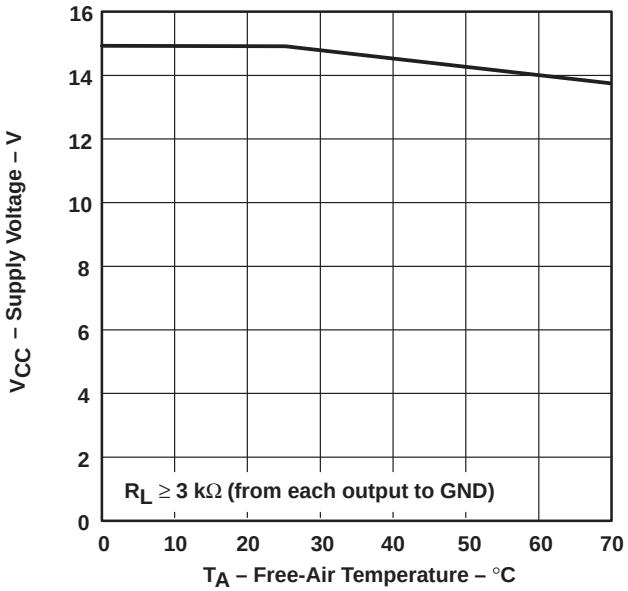


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75185 in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

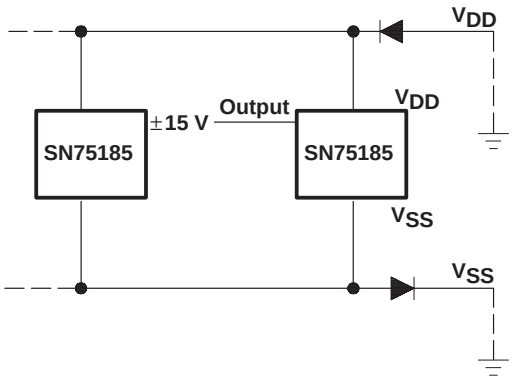
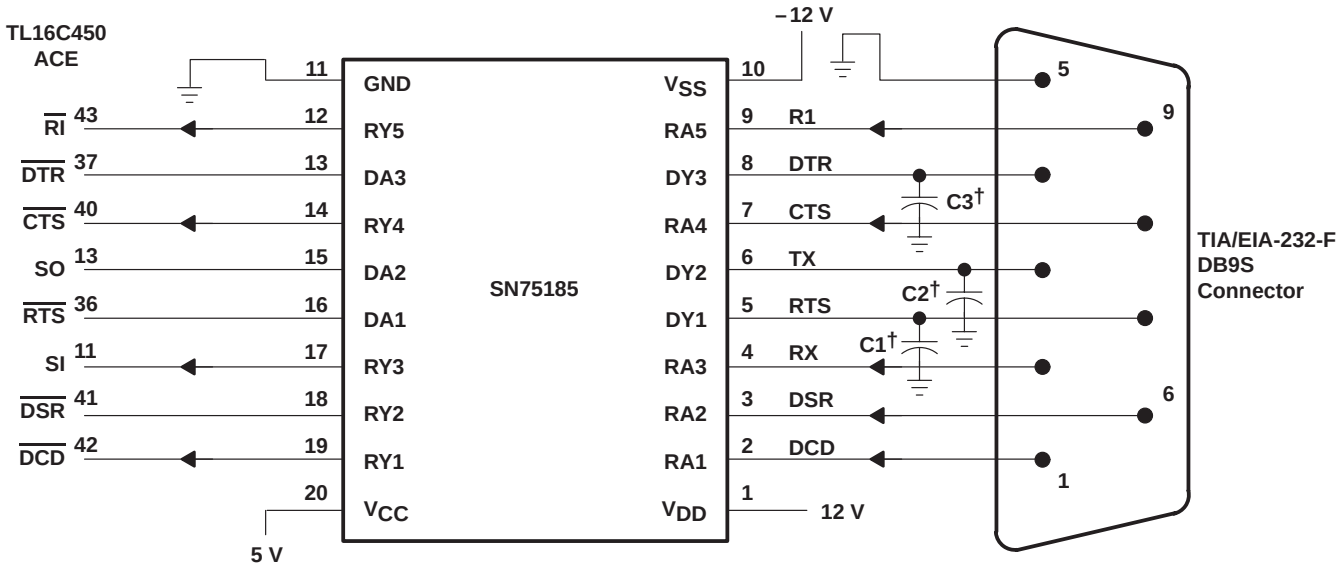


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which are required to meet the RS-232 maximum slew-rate requirement of 30 V/µs. The value of the loading capacitors required depends upon the line length and desired slew rate, but typically is 330 pF.

Figure 16. Typical Connection

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.