

T6K01

COLUMN DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The T6K01 is a column (segment) driver for a dot matrix graphic LCD. The T6K01 offers low power consumption, due to the CMOS Si-Gate process. It is designed to interface directly with a microprocessor unit (MPU). A program running on the MPU can drive the T6K01 asynchronously. The T6K01 stores data transferred from the MPU in its built-in RAM.

The data stored in the built-in display RAM corresponds to the image on the LCD screen; the data is converted into the LCD drive signal. A configuration of two T6K01s and one T6C03 can be used to drive a 480 × 160-dot LCD.

Features

- Dot matrix graphic LCD column driver with display RAM
- Display RAM capacity: 160 lines × 240 outputs = 38400 bits
- LCD drive output: 240
- Interface: 8-bit MPU
- Relation between RAM data and display
RAM bit data = 1 → display ON
RAM bit data = 0 → display OFF
- Display OFF function
- Low power consumption
- Logic power supply: 2.7 to 3.3 V
- LCD power supply: 8.0 to 26.0 V
- CMOS Process
- Package: TCP (Tape Carrier Package)

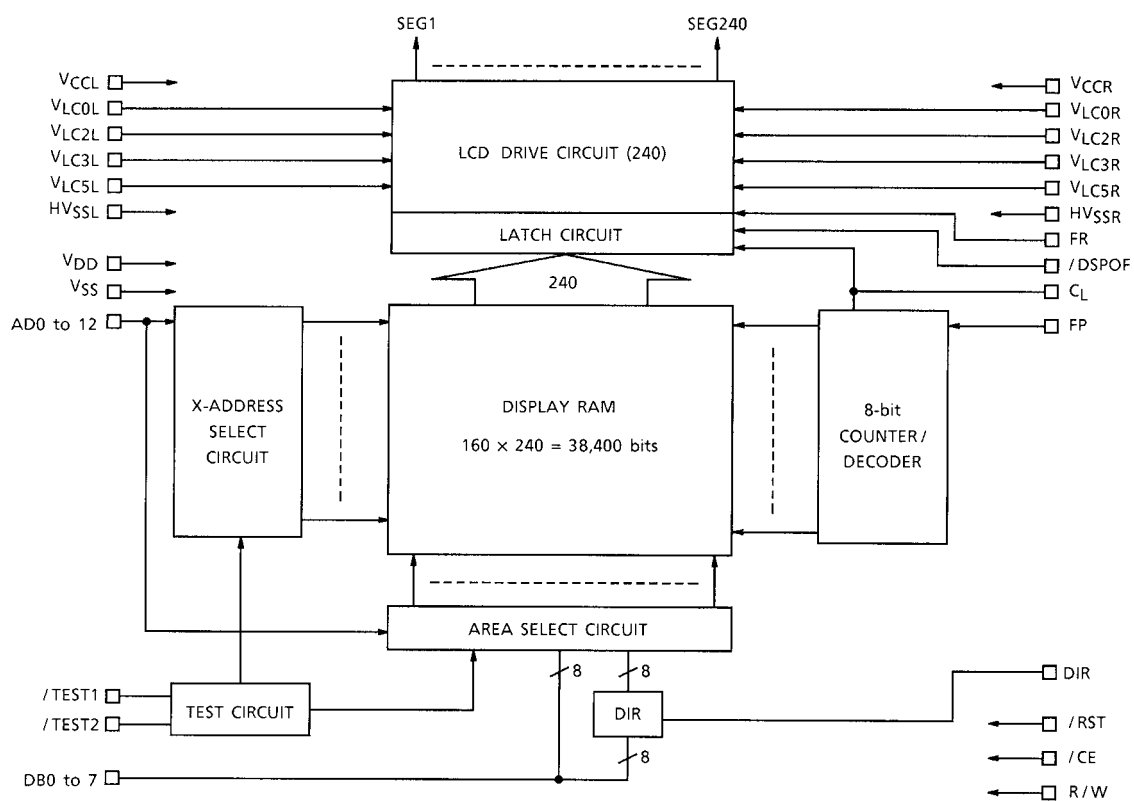
Unit: mm

| T6K01 | LEAD PITCH | |
|------------|------------|------|
| | IN | OUT |
| (UAM, 4N5) | 0.8 | 0.14 |

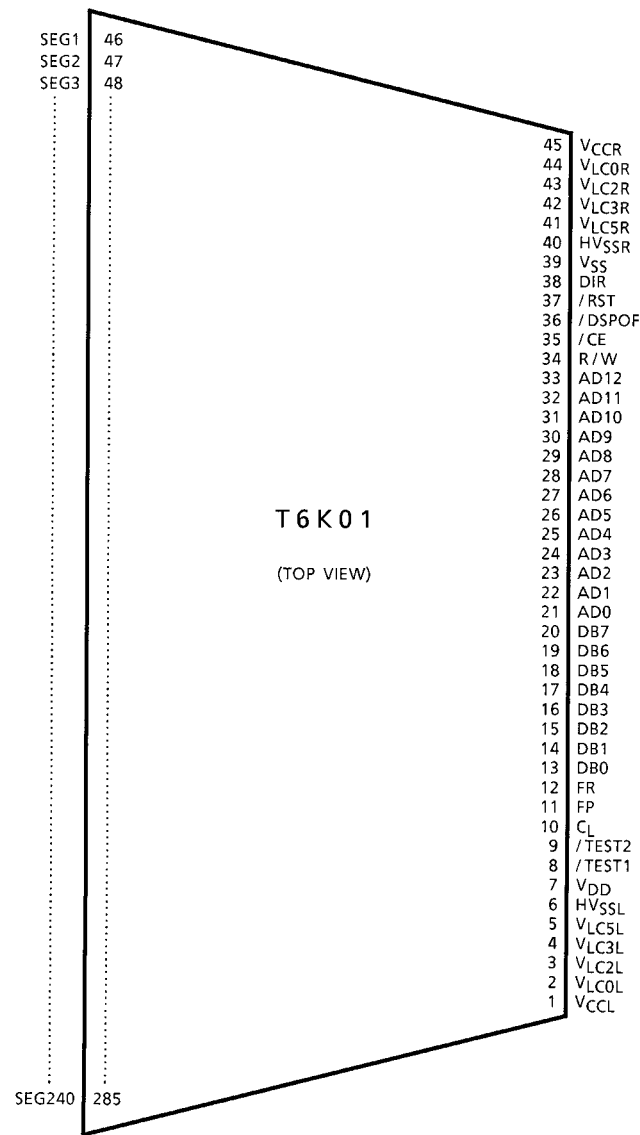
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

Block Diagram



Pin Assignment



Note: The above diagram shows the pin configuration of the LSI chip; it does not show the configuration of the tape carrier package.

Pin Functions

| Pin Name | Pin No. | I / O | Functions |
|--|--|--------|---|
| SEG1 to SEG240 | 46 to 285 | Output | Column driver outputs |
| C _L | 10 | Input | Shift clock pulse |
| FP | 11 | Input | Display synchronous signal |
| FR | 12 | Input | Frame signal |
| DB0 to DB7 | 13 to 20 | I / O | Data bus |
| AD0 to AD12 | 21 to 33 | Input | Address bus |
| R / W | 34 | Input | Read / write select R / W = H → Read selected R / W = L → Write selected |
| / CE | 35 | Input | Chip enable Data write: Data write enabled on rising edge of / CE Data read: Data read out while / CE is at L level |
| / DSPOF | 36 | Input | Display off. Usually connected to V _{DD} . / DSPOF = H: Display-on mode. (SEG1 to SEG240) are operational. / DSPOF = L: Display-off mode. (SEG1 to SEG240) are at the V _{SS} level. |
| / RST | 37 | Input | Reset signal: / RST = L → Reset state |
| DIR | 38 | Input | Data direction select |
| / TEST1, 2 | 8, 9 | Input | Test pin. Usually connected to V _{DD} |
| V _{DD} , V _{SS} | 7, 39 | — | Power supply |
| V _{CCL} , V _{CCR} V _{LC0L} , V _{LC0R} V _{LC2L} , V _{LC2R} V _{LC3L} , V _{LC3R} V _{LC5L} , V _{LC5R} HV _{SSL} , HV _{SSR} | 1, 45 2, 44 3, 43 4, 42 5, 41 6, 40 | — | Power supply for LCD drive |

Function of Each Block

- **RAM cell**

The RAM capacity is 160 lines \times 240 outputs for a total of 38400 bits.

- **DIR**

This circuit changes the data flow direction and page selection sequence.

- **Address decoder**

This decoder selects one RAM address for read / write operation.

- **8-bit counter + decoder**

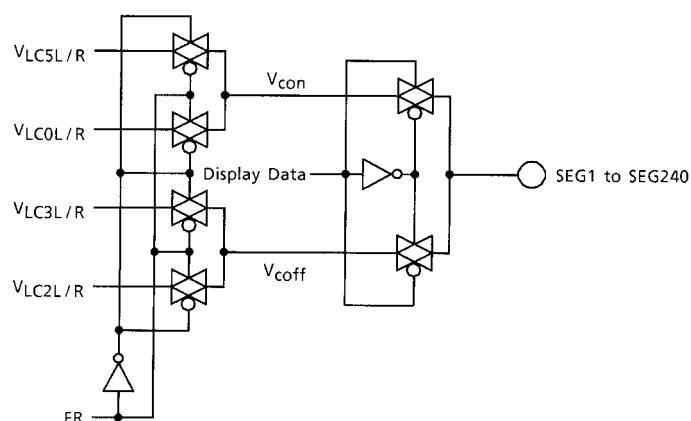
The decoder selects one RAM cell from the 160 address lines for display operation.

- **Latch**

The data is latched from the display RAM on the falling edge of CL .

- **Column driver circuit and LCD voltage generation circuit**

The T6K01 has 240 column drivers and four different LCD drive output voltage levels. The display data from the latch circuit and the M signal determine which of the four LCD drive voltages is selected. This circuit is shown in the following diagram.



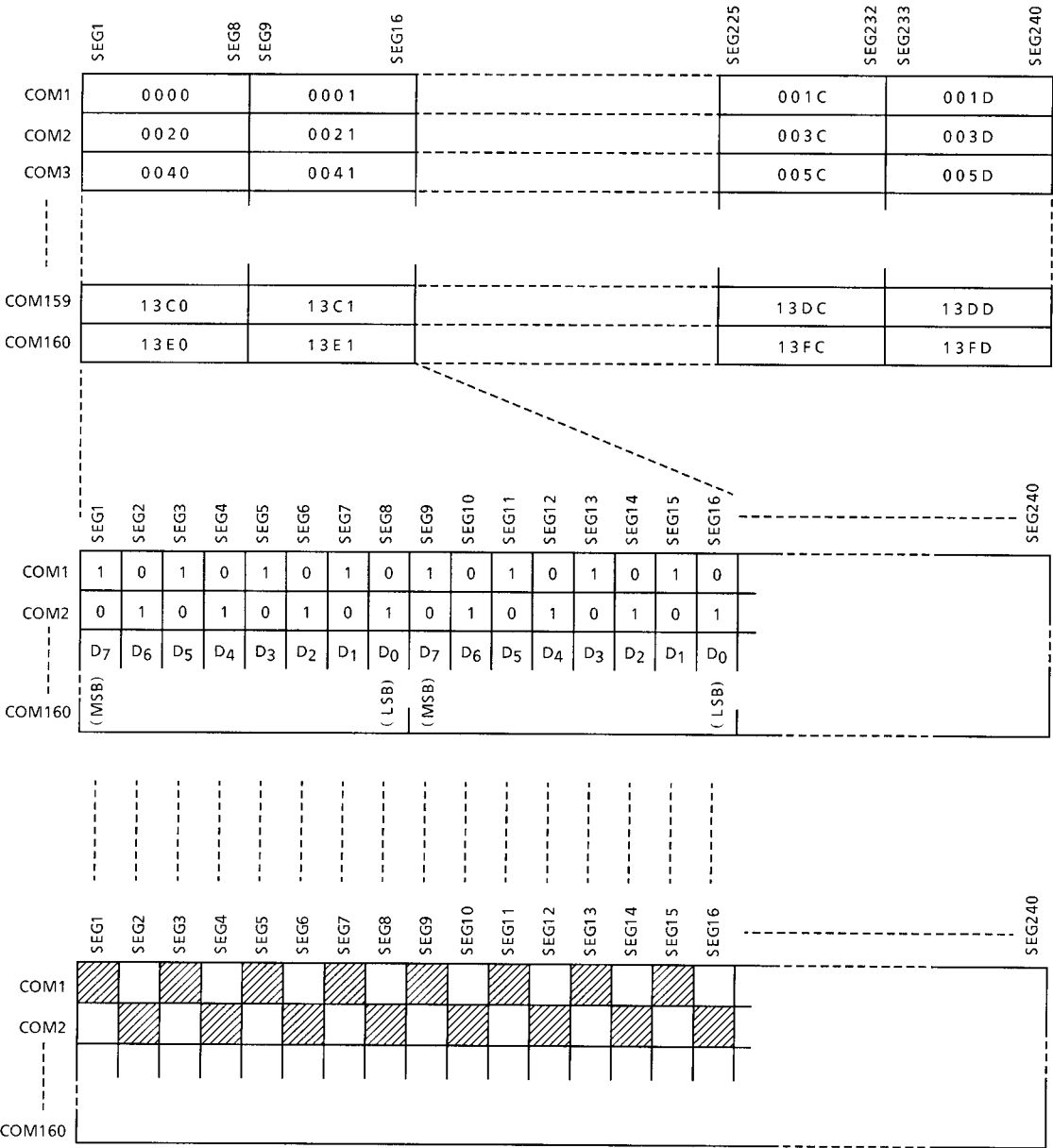
Relation Between FR, Data Input and Output Level

| / DSPOF | FR | Input Data (RAM Data) | Output Level |
|---------|----|-----------------------|--------------------|
| L | * | * | V_{SS} / V_{LC5} |
| H | L | L | V_{LC3} |
| H | L | H | V_{SS} / V_{LC5} |
| H | H | L | V_{LC2} |
| H | H | H | V_{LC0} |

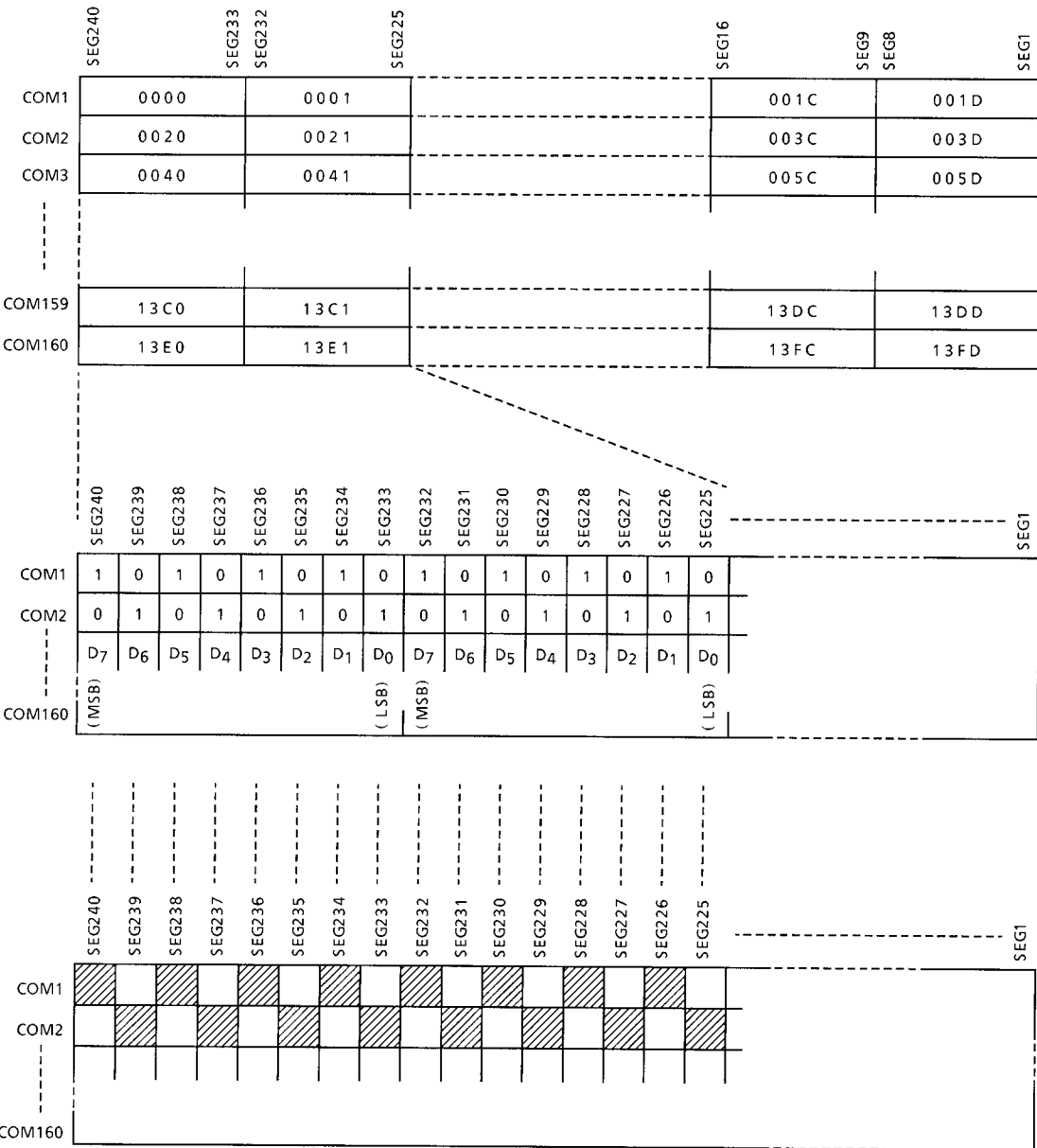
*: INVALID

• The relation between DIR and the memory map

(1) DIR = H



(2) DIR = L



Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Rating | Unit |
|-----------------------|--------------------------------|-------------------------------|------|
| Supply Voltage (1) | V _{DD} (Note 2) | -0.3 to 6.5 | V |
| Supply Voltage (2) | (Note 1, 2) | -0.3 to 28.0 | V |
| Input Voltage | V _{IN} (Note 2, 3) | -0.3 to V _{DD} + 0.3 | V |
| Operating Temperature | T _{opr} | -20 to 75 | °C |
| Storage Temperature | T _{stg} | -55 to 125 | °C |

Note 1: V_{CCL}, V_{CCR}, V_{LC0L}, V_{LC0R}, V_{LC2L}, V_{LC2R}, V_{LC3L}, V_{LC3R}, V_{LC5L} and V_{LC5R}

Note 2: Referenced to V_{SS}, HV_{SSL} and HV_{SSR}

Note 3: Applies to all data bus and I / O pins.

Note 4: Ensure that the following condition is always maintained.

$$V_{CCL} / R \geq V_{LC0L} / R \geq V_{LC2L} / R \geq V_{LC3L} / R \geq V_{LC5L} / R \geq HV_{SSL} / R$$

Electrical Characteristics

DC Characteristics

Test Conditions

(Unless Otherwise Noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL}/R = 23.0\text{ V} \pm 10\%$,
 $T_a = -20\text{ to }75^\circ\text{C}$)

| Item | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | Pin Name |
|---------------------------------|-----------|--------------|---|------------------------------------|----------------|--------------|---------------|---|
| Operating Supply (1) | V_{DD} | — | — | 2.7 | — | 3.3 | V | V_{DD} |
| Operating Supply (2) | V_{CC} | — | — | 8.0 | — | 26.0 | V | V_{CCL} , V_{CCR} |
| Input Voltage | H Level | V_{IH} | — | 0.7 V_{DD} | — | V_{DD} | V | DB0 to DB7 AD0 to AD7, / RST, / DSPOF, / CE, R / W, D / I, C_L , FP, FR, DIR, / TEST |
| | L Level | V_{IL} | — | 0 | — | 0.3 V_{DD} | V | |
| Output Voltage | H Level | V_{OH} | — | $I_{OH} = -400\text{ }\mu\text{A}$ | $V_{DD} - 0.4$ | V_{DD} | V | DB0 to DB7 |
| | L Level | V_{OL} | — | $I_{OL} = 400\text{ }\mu\text{A}$ | V_{SS} | 0.4 | V | |
| Column Driver Output Resistance | R_{col} | — | Load current = $\pm 100\text{ }\mu\text{A}$ (Note 4) | — | — | 3.0 | k Ω | SEG1 to SEG160 |
| Input Leakage | I_{IL} | — | $V_{IN} = V_{DD}$ to V_{SS} | -1 | — | 1 | μA | DB0 to DB7 AD0 to AD7, / RST, / DSPOF, / CE, R / W, D / I, C_L , FP, FR, DIR, / TEST |
| Operating Freq. | f_{CL} | — | — | 10 | — | 50 | kHz | C_L |
| Current Consumption (1) | I_{SS1} | — | (Note 1) | — | 410 | 520 | μA | V_{SS} , HV_{SSL} , HV_{SSR} , V_{LC5L} , V_{LC5R} |
| Current Consumption (2) | I_{SS2} | — | (Note 2) | — | 45 | 65 | μA | V_{SS} , HV_{SSL} , HV_{SSR} , V_{LC5L} , V_{LC5R} |
| Current Consumption (3) | I_{SS3} | — | (Note 3) | -1 | — | 1 | μA | V_{SS} , HV_{SSL} , HV_{SSR} , V_{LC5L} , V_{LC5R} |

Note 1: Current consumption while internal data receiver is operating

$V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL}/R = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias, 1 / 160 duty, no load, $f_{FP} = 70\text{ Hz}$,
 $f / CE = 5\text{ MHz}$

Note 2: Current consumption while internal data receiver is sleeping

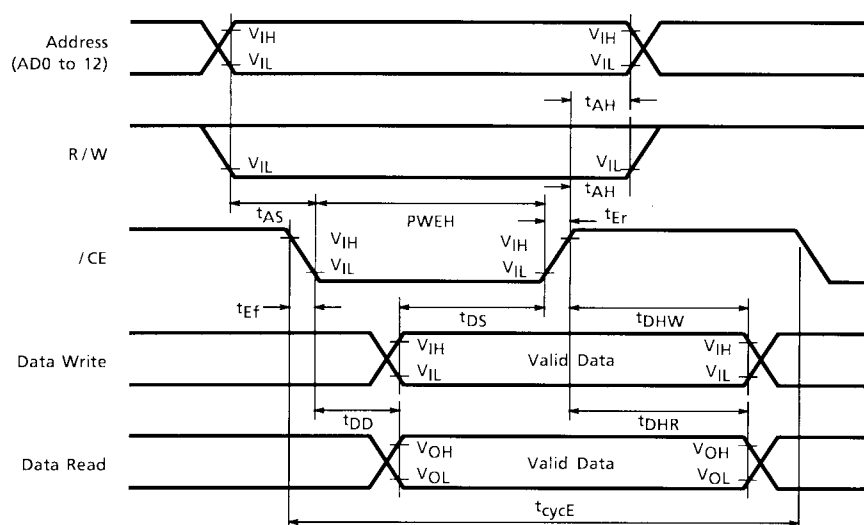
$V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL}/R = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias, 1 / 160 duty, no load, $f_{FP} = 70\text{ Hz}$,
 $f / CE = 0\text{ Hz}$

Note 3: Standby current consumption

$V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL}/R = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, no load, $f_{FP} = 0\text{ Hz}$, $f / CE = 0\text{ Hz}$

Note 4: $V_{CCL}/R = V_{LC0L}/R = 23.0\text{ V}$, $V_{LC2L}/R = V_{CC} \times 11 / 13$, $V_{LC3L}/R = V_{CC} \times 2 / 13$,
 $HV_{SSL}/R = V_{LC5L}/R = 0\text{ V}$

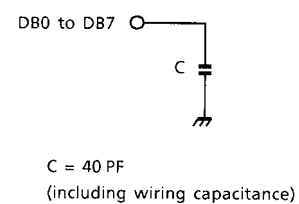
AC Characteristics (1)



Test Conditions (Unless Otherwise Noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 3.0\text{ V} \pm 10\%$, $T_a = -20\text{ to }75^\circ\text{C}$)

| Item | Symbol | Min | Max | Unit |
|-------------------------|------------------|-----|-----|------|
| Enable Cycle Time | t_{cycE} | 250 | — | ns |
| Enable Pulse Width | $PWEH$ | 160 | — | ns |
| Enable Rise / Fall Time | t_{Er}, t_{Ef} | — | 20 | ns |
| Address Set-up Time | t_{AS} | 0 | — | ns |
| Address Hold Time | t_{AH} | 10 | — | ns |
| Data Set-up Time | t_{DS} | 100 | — | ns |
| Data Hold Time | t_{DHW} | 20 | — | ns |
| Data Delay Time | t_{DD} (Note) | — | 180 | ns |
| Data Hold Time | t_{DHR} (Note) | 20 | — | ns |

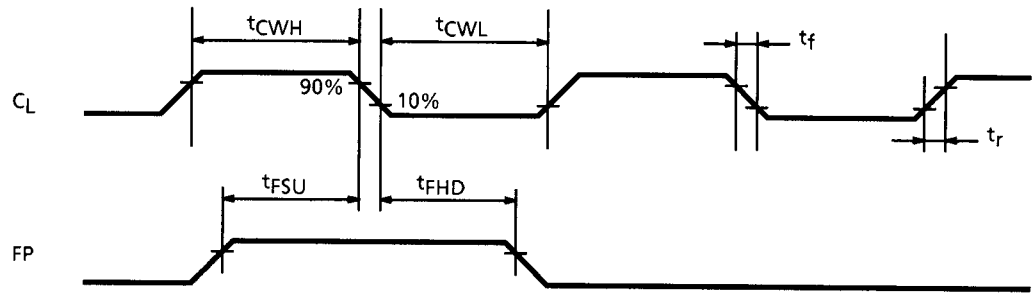
Load Circuit



Note: With load circuit connected

AC Characteristics (2)

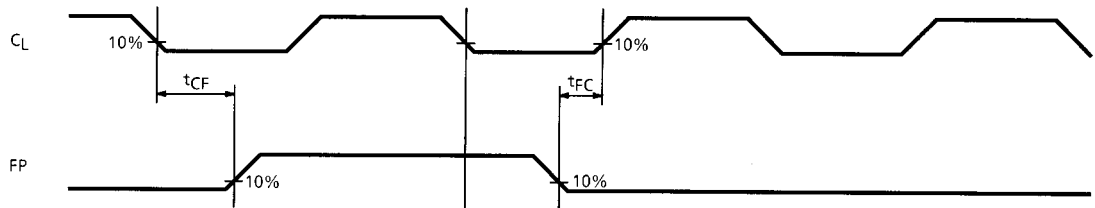
display data



Test Conditions (Unless Otherwise Noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 3.0\text{ V} \pm 10\%$, $T_a = -20\text{ to }75^\circ\text{C}$)

| Item | Symbol | Pin Name | Min | Max | Unit |
|------------------------|------------|----------|-----|-----|------|
| C_L Pulse Width H | t_{CWH} | C_L | 500 | — | ns |
| C_L Pulse Width L | t_{CWL} | C_L | 500 | — | ns |
| C_L Rise / Fall Time | t_r, t_f | C_L | — | 50 | ns |
| FP Set-up Time | t_{FSU} | FP | 100 | — | ns |
| FP Hold Time | t_{FHD} | FP | 100 | — | ns |

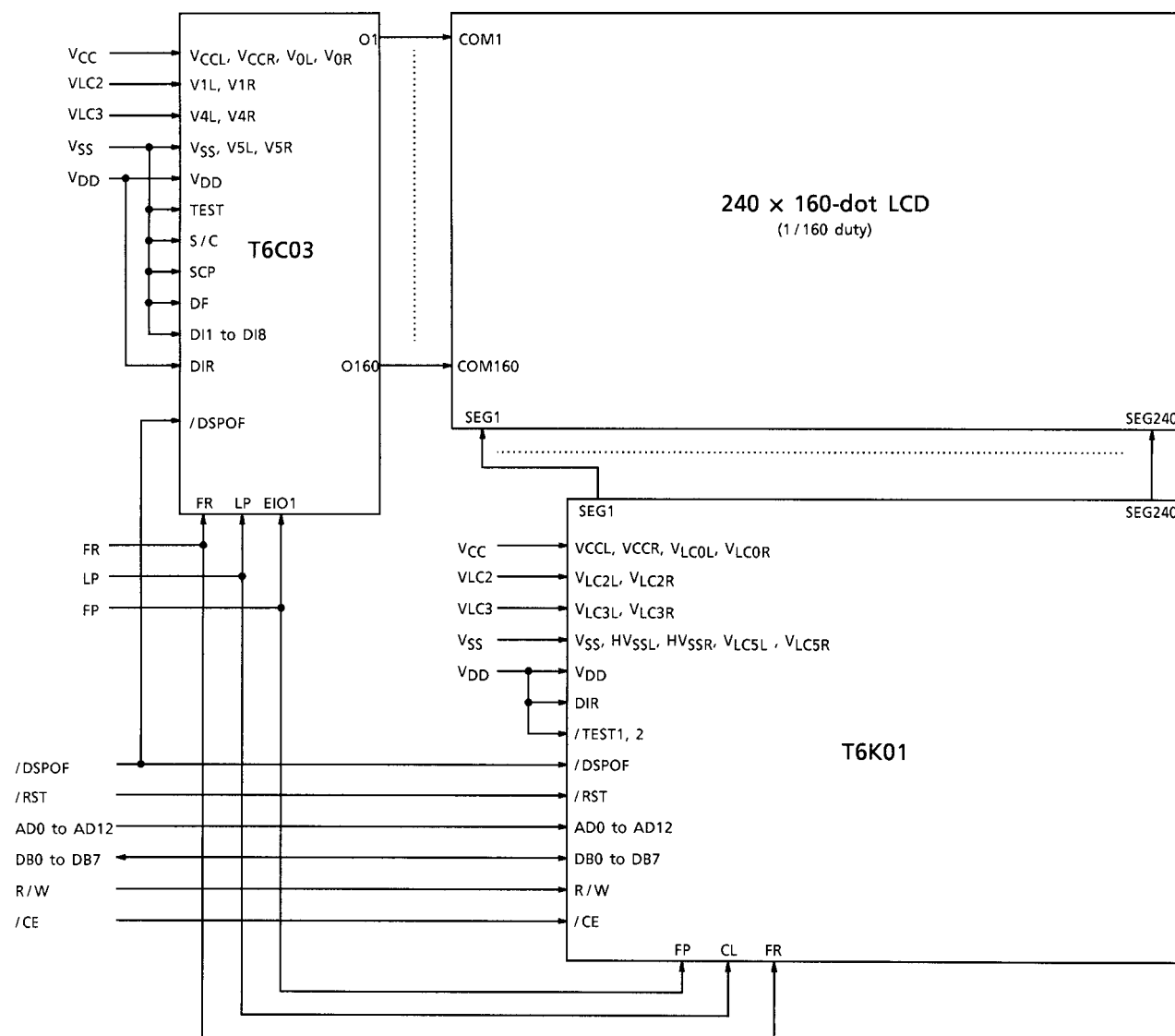
AC Characteristics (3)



| Item | Symbol | Condition | Min | Max | Unit |
|------------------------------|----------|-----------|-----|-----|------|
| C_L -to- FP -margin time | t_{CF} | | 20 | — | ns |
| FP -to- C_L -margin time | t_{FC} | | 0 | — | ns |

Application Circuit

T6K01 + T6C03



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