TOSHIBA

TC240DC/DE Embedded DRAM SLI ASIC 0.25µm dRAMASIC™

Description

The TC240D is Toshiba's 0.25µm Embedded DRAM System-Level Integration (SLI) ASIC family. The TC240D is targeted at applications requiring high bandwidth. Toshiba's trench capacitor technology permits high-density embedded memory without degrading logic speeds.

Product Features

- Available as either standard cell or embedded array
- 80ps loaded 2-input NAND gate delay, with fanout = 5, for high-performance systems
- V_{DD}= 2.5V±0.2V (core); V_{DD}= 3.3V±0.3V (I/O)
- Typical 0.17µW/MHz core power consumption
- Maximum 128Mbits of memory; actual gate count will depend on memory core size, e.g., up to 500K gates with 64Mbits of DRAM
- Utilizes Toshiba's Unified Cell Architecture
- Core cell library for System ASIC implementation
- Wide range of high-performance I/O options
- Highly accurate delay model with non-linear dependency on slew rate, load, and logic state
- Commercial EDA tool sign-off for design flexibility
- Wide range of package options including TQFP, TBGA, TPGA to meet all application needs

DRAM Core Features

- 1 transistor cell structure utilizing trench capacitor technology
- Maximum 10.6GB/s bandwidth
- Power supply: 2.5V±0.2V
- Memory organization
  - 2Mbit–16Mbit/Macro (×64 or ×128; 1, 2 or 4 banks)
  - 4Mbit–32Mbit/Macro (×128 or ×256; 1, 2 or 4 banks)
- Excellent DRAM core granularity and bus width flexibility up to 512 bits wide
  - 2Mbit–16Mbit/Macro (in 1Mbit increment/ bank)
  - 4Mbit–32Mbit/Macro (in 2Mbit increment/ bank)
- Synchronous interface. All signals referenced to positive edge of the clock
- 1024 refresh cycles/16ms, automatic refresh
- Byte Write data control
- Frequency of Operation: 166MHz max

Embedded DRAM Benefits

- Flexibility in configuring the DRAM macrocell based on application requirements
- Significant increase in bandwidth due to the flexibility of wide and fast memory buses (max. 10.6GB/s bandwidth)
- Memory access time lower then discrete DRAM approach
- Elimination of a large number of devices as well as reduction of total ASIC pin count
- Lower power consumption—systems with fast and wide memory buses will dissipate significantly less power due to lower-capacitance on-chip connections
- Lower switching noise on data bus between memory and logic

Benefits of Toshiba's trench capacitor technology as compared to stacked capacitor technology are significant:

- Achieve a higher density DRAM core and gate count for a given die size
- The trench capacitor, which is formed beneath the surface of the silicon, requires no additional manufacturing steps between the gate and metal. This allows for a planar silicon surface topology which improves reliability
- Trench DRAM cell capacitance significantly lowers the soft error rate—large capacitors require more charge to switch states.

Target Applications

- Graphics controllers
- Hubs
- Switches
- Set-Top-Boxes
- Printers
- Digital Video Disks
- HDD
- Any application with high-performance data transfer requirements, especially those requring wider bus widths

Optimized Macrocell Performance

The TC240D family has three ranges of logic macrocells for speed/power optimization:

	Cell Type*		
	Low-Power	**Normal**	**High-Speed**
Delay	186ps	119ps	80ps
Power	0.1µW	0.17µW	0.31µW

* 2-input NAND, fanout = 5 plus typical interconnect load, nominal operating conditions

System-Level IC Cores and Cells

Toshiba's SLI ASIC TC240D family is supported by cores and cells such as 10/100 Ethernet, ATM, RISC, PCI, USB, 1394, LVDS, etc. In addition, Toshiba has established partnerships with IP providers so the broadest offering of IP can be accessed for a design.

Commercial EDA Tool Sign-off

The TC240D is supported by Toshiba's open EDA strategy based on sign-off on multiple commercial EDA tools. Support includes Static Timing Sign-off (STSO) and Toshiba's Timing-Driven Flow (TDF™) that can reduce SLI design iterations an order of magnitude and achieve timing convergence.

Toshiba has a range of Design for Test (DFT) support, including SCAN, Partial SCAN, BIST, and Boundary SCAN.

DRAM Test Strategy

The test strategy is based on using the standard DRAM test algorithms to guarantee that functionality specifications for the embedded DRAM core are met. The scheme for implementation of the redundancy in the DRAM core is consistent with that of the standard DRAM device. Toshiba guarantees full testing of the embedded DRAM core.

Technology Resource Centers

Toshiba SLI ASIC Technology Resource Centers are located throughout the U.S. to provide technical support before, during, and after the design of a Toshiba ASIC. This includes support with EDA environments and design kits, Toshiba design methodologies, ASIC technologies, and design implementation.

In addition, Toshiba's North America Semiconductor Engineering Development Center based in San Jose, CA is staffed with system, technology, and EDA design experts who work with customers on advanced System IC applications.

High-Quality, High-Volume Manufacturing

Toshiba's ASIC manufacturing plants are among the largest and most advanced in the world. They are all certified to ISO9000. Rigorous quality control coupled with a sophisticated batch tracking system allows Toshiba to meet the needs of fast-ramping, high-volume markets.

TOSHIBA

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