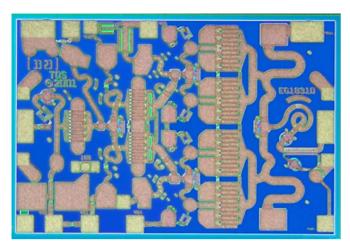
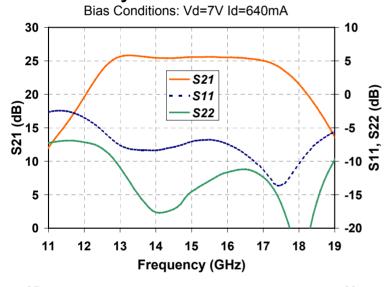
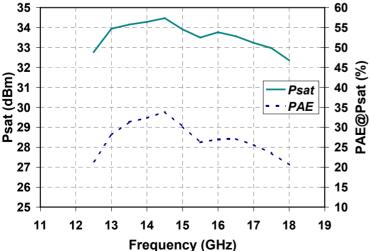


13 - 17 GHz 2.5 Watt, 25dB Power Amplifier TGA2505-EPU



Preliminary Measured Performance





Key Features and Performance

- 34 dBm Midband Pout
- 25 dB Nominal Gain
- 7 dB Typical Input Return Loss
- 12 dB Typical Output Return Loss
- Built-in Directional Power Detector with Reference
- 0.25µm pHEMT, 3MI Technology
- Bias Conditions: 7V, 640mA
- Chip dimensions: 2.0 x 1.4 x 0.1 mm (80 x 55 x 4 mils)

Primary Applications

- VSAT
- Point-to-Point



TGA2505-EPU

TABLE I MAXIMUM RATINGS

Symbol	Parameter <u>1</u> /	Value	Notes
V ⁺	Positive Supply Voltage	8 V	<u>2</u> /
V	Negative Supply Voltage Range	-5V to 0V	
I ⁺	Positive Supply Current (Quiescent)	TBD	<u>2</u> /
I _G	Gate Supply Current	18 mA	
P _{IN}	Input Continuous Wave Power	24 dBm	<u>2</u> /
P_D	Power Dissipation	6.43 W	<u>2</u> / <u>3</u> /
T _{CH}	Operating Channel Temperature	150 °C	<u>4</u> / <u>5</u> /
T _M	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
- 3/ When operated at this bias condition with a base plate temperature of 70°C, the median life is reduced from 8.9E+6 to 1E+6.
- 4/ These ratings apply to each individual FET.
- $\underline{5}$ / Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II DC PROBE TEST

(TA = 25 °C, Nominal)

NOTES	SYMBOL	LIMI	UNITS	
		MIN	MAX	
<u>1</u> /	I _{DSS}	80	381	mA
<u>1</u> /	G _M	176	424	mS
<u>2</u> /	V _P	0.5	1.5	V
<u>2</u> /	V _{BVGS}	8	30	V
<u>2</u> /	V _{BVGD}	13	30	V

- 1/ Measurements are performed on a 800µm FET.
- $2/V_P$, V_{BVGD} , and V_{BVGS} are negative.



TGA2505-EPU

TABLE III RF CHARACTERIZATION TABLE

 $(T_A = 25^{\circ}C, Nominal)$ (Vd = 7V, ld = 680mA ±5%)

SYMBOL	PARAMETER	TEST	LIMITS		UNITS	
		CONDITION	MIN	TYP	MAX	
Gain	Small Signal Gain	F = 13-17		25		dB
IRL	Input Return Loss	F = 13-17		7		dB
ORL	Output Return Loss	F = 13-17		12		dB
PWR	Output Power @ Pin = +5 dBm	F = 13-17		34		dBm

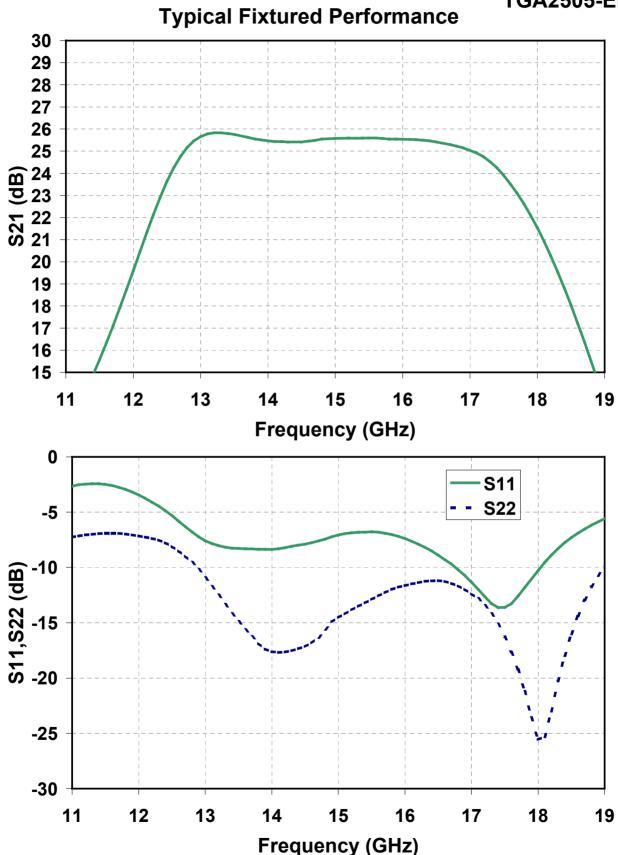
Note: Table III Lists the RF Characteristics of typical devices as determined by fixtured measurements.

TABLE IV THERMAL INFORMATION

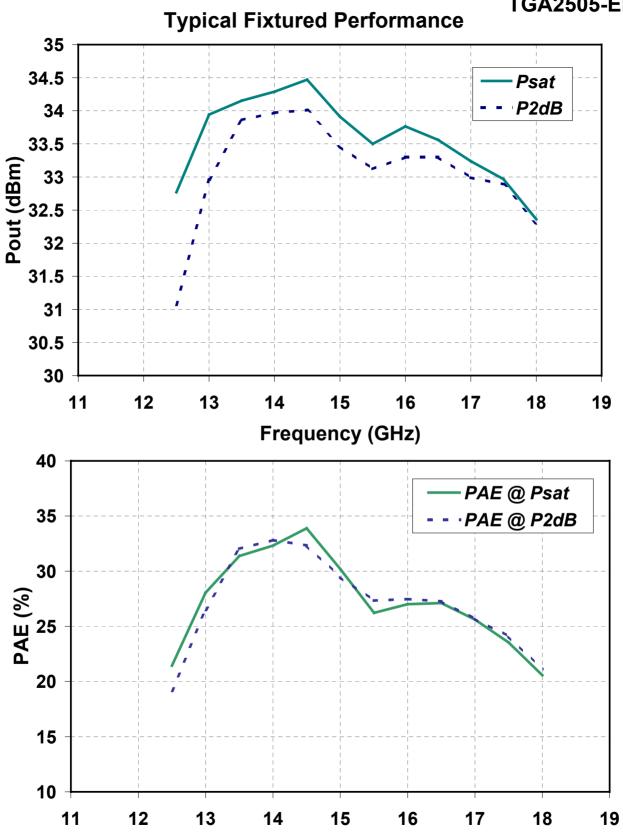
PARAMETER	TEST CONDITION	T _{CH} (°C)	R _{θjc} (°C/W)	MTTF (HRS)
R _{0ic} Thermal Resistance	$V_D = 7V$	405.74	40.44	0.05.0
(Channel to Backside)	$I_D = 640 \text{mA}$	125.74	12.44	8.9E+6
,	$P_D = 4.48W$			

Note: Assumes eutectic attach using 1.5mil 80/20 AuSn mounted to a 20mil CuMo carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.





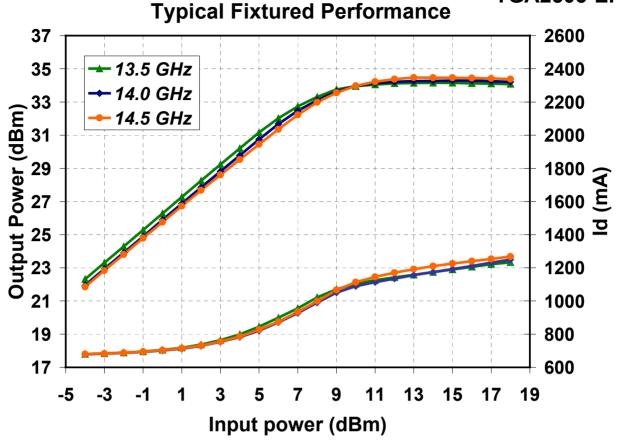




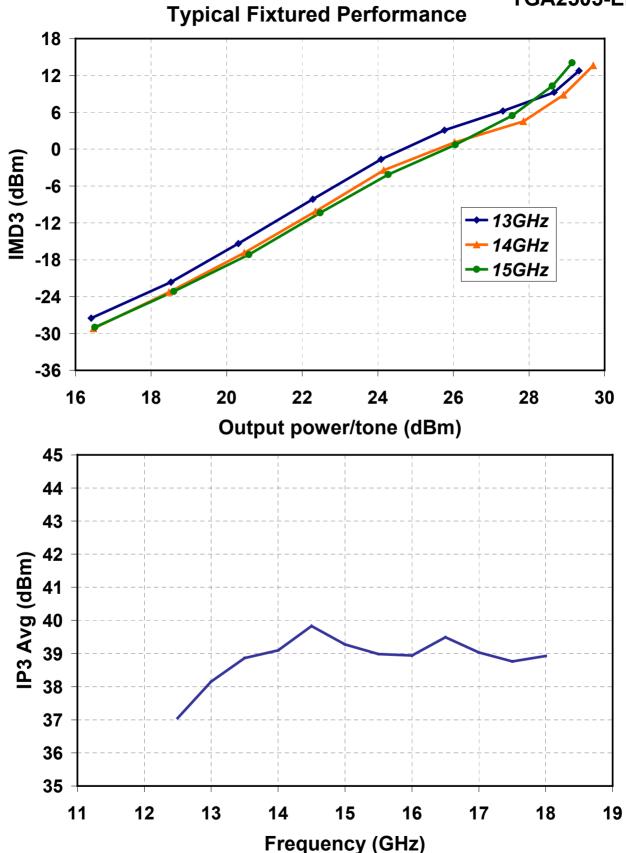
Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

Frequency (GHz)





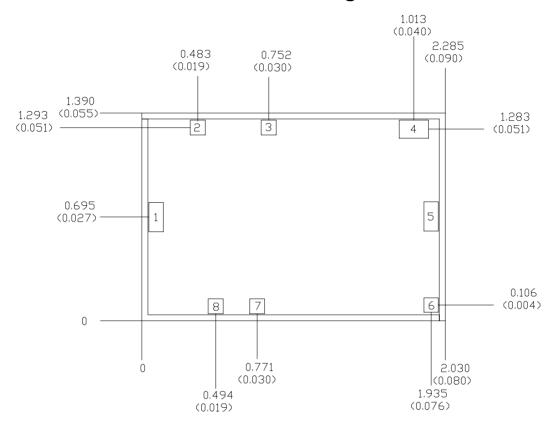






TGA2505-EPU

Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.1016 (0.004) (reference only)

Chip edge to bond pad dimensions are shown to center of Bond pads

Chip size tolerance: +/- 0.0508 (0.002)

RF Ground through Backside

Bond	Pad	#1	(RF Input)	0.100	\times	0.200	(0.004	\times	0.008)
Bond	Pad	#2	(Vref)	0.100	X	0.100	(0.004	\times	0.004)
Bond	Pad	#3	(/d3)	0.100	X	0.100	(0.004	\times	0.004)
Bond	Pad	#4	(Vd4)	0,200	\times	0.125	(0.008	×	0.005)
Bond	Pad	#5	(RF Dutput)	0.100	X	0.200	(0.004	\times	(800,0
Bond	Pad	#6	(Vdet)	0.100	X	0.100	(0.004	\times	0.004)
Bond	Pad	#7	(Vg4)	0.100	X	0.100	(0.004	×	0.004)
Bond	Pad	#8	(Vg3)	0.100	×	0.100	(0.004	×	0.004)



0.6

0.5

0.4

0.3

0.2

0.1

0

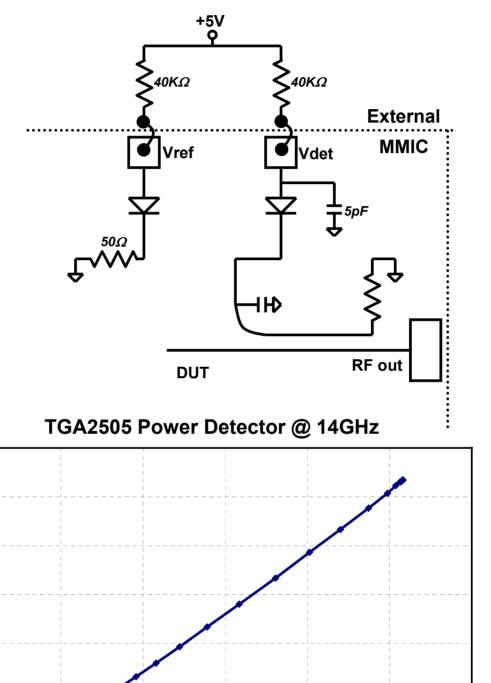
0

10 (20 dBm)

Vref-Vdet (V)

TGA2505-EPU

Power Detector



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

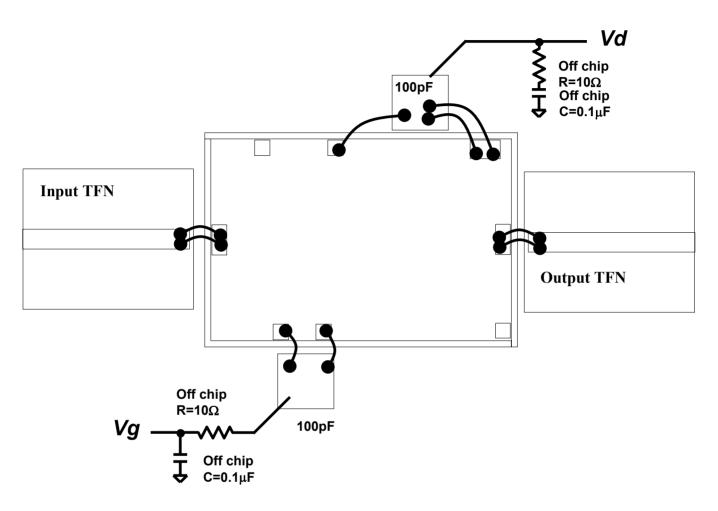
20 (26 dBm) 60

sqrt Pout (mW^0.5)





Chip Assembly & Bonding Diagram



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.



TGA2505-EPU

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C. (30 seconds maximum)
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.