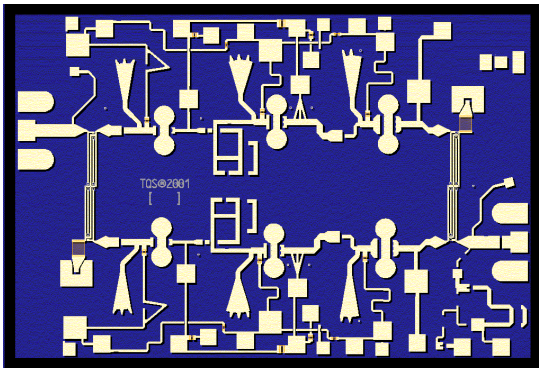
Advance Product Information
November 2, 2004

Q-Band Driver Amplifier

TGA4042-EPU



Key Features

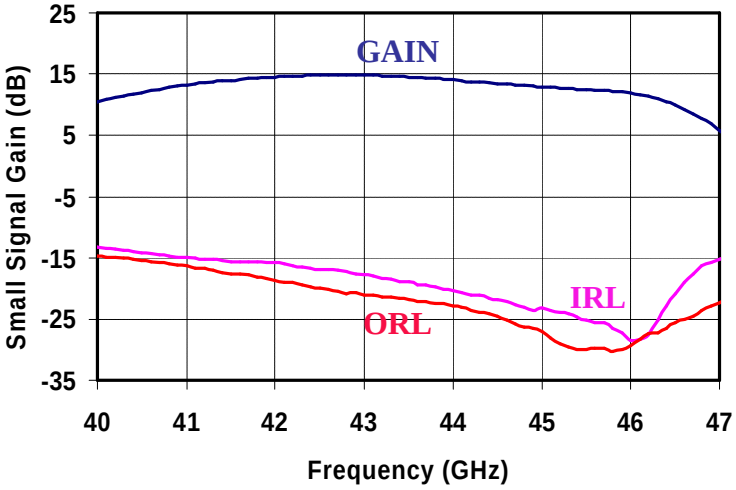
- Typical Frequency Range: 41 - 45 GHz
- 18 dBm Nominal P1dB
- 14 dB Nominal Gain
- 17 dB Nominal Return Loss
- On-Chip Power Detector
- Bias 6 V, 168 mA
- 0.25 um 2MI pHEMT Technology
- Chip Dimensions 3.20 x 2.18 x 0.1 mm
  (0.126 x 0.086 x 0.004) in

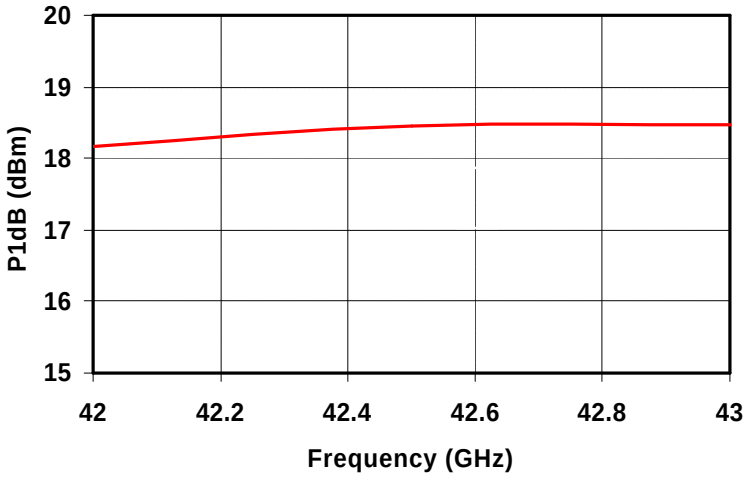
Primary Applications

- Point-to-Point Radio
- Military Radar Systems
- Q Band Sat-Com

Preliminary Measured Data

Bias Conditions: Vd = 6 V, Id = 168 mA





Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
Vd	Drain Voltage	8 V	2/
Vg	Gate Voltage Range	-5 TO 0 V	
Id	Drain Current	294 mA	2/ 3/
$\|Ig\|$	Gate Current	14 mA	3/
P_{IN}	Input Continuous Wave Power	21 dBm	
P_D	Power Dissipation	3.3 W	2/ 4/
T_{CH}	Operating Channel Temperature	150 ^{0}C	5/ 6/
T_M	Mounting Temperature (30 Seconds)	320 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Total current for the entire MMIC.

4/ When operated at this bias condition with a base plate temperature of 70 ^{0}C, the median life is reduced to 1E+6 hrs.

5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

TABLE II
DC PROBE TESTS
(Ta = 25 ^{0}C, Nominal)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
$I_{DSS,Q1}$	Saturated Drain Current	20	57	94	mA
$G_{M,Q1}$	Transconductance	44	75	106	mS
$V_{BVGS,Q1}$	Breakdown Voltage Gate-Source	-30	-21	-8	V
$V_{BVGD,Q1\ \&\ Q3}$	Breakdown Voltage Gate-Drain	-30	-21	-8	V
$V_{P,Q1-Q6}$	Pinch-Off Voltage	-1.5	-1	-0.5	V

Q1& Q2 are 200 um FETs, Q3 & Q4 are 240 um FETs, Q5 & Q6 are 400 um FETs

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TABLE III
ELECTRICAL CHARACTERISTICS
(Ta = 25 ^{0}C, Nominal)

PARAMETER	TYPICAL	UNITS
Frequency Range	41 - 45	GHz
Drain Voltage, Vd	6	V
Drain Current, Id	168	mA
Gate Voltage, Vg	-0.5	V
Small Signal Gain, S21	14	dB
Input Return Loss, S11	17	dB
Output Return Loss, S22	20	dB
Output Power @ 1 dB Compression Gain, P1dB	18	dBm

TABLE IV
THERMAL INFORMATION

PARAMETER	TEST CONDITIONS	T_{CH} (^{O}C)	R_{qJC} (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 6 V I_D = 168 mA Pdiss = 1.008 W	92.58	22.40	2.7E+8

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

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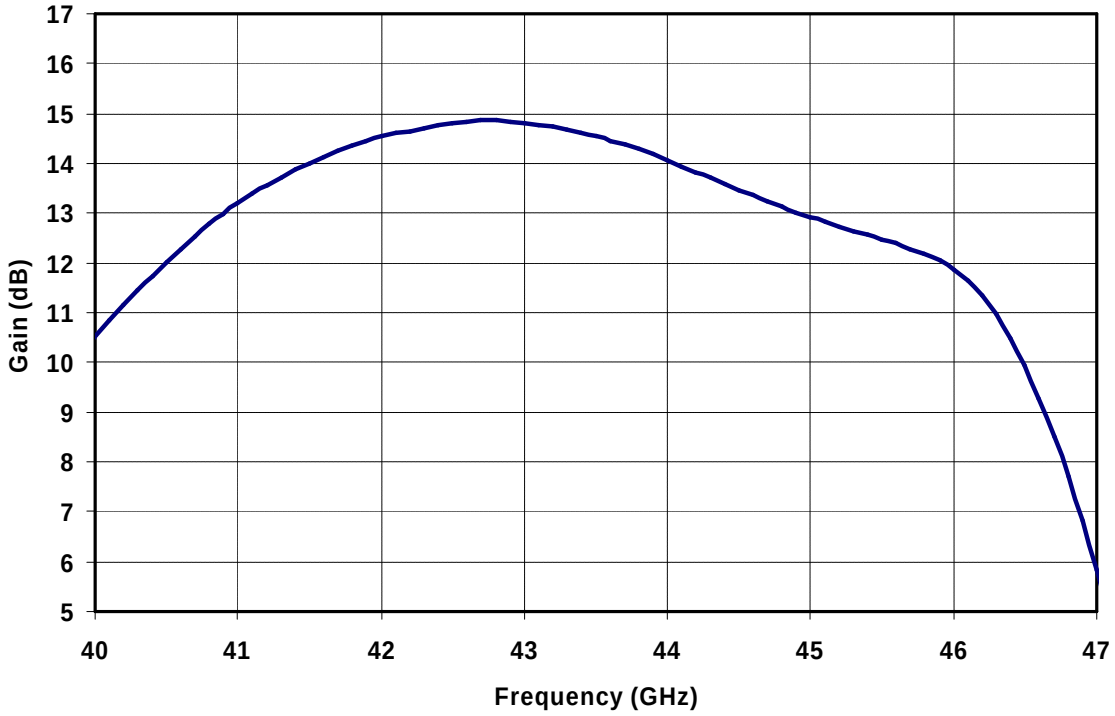
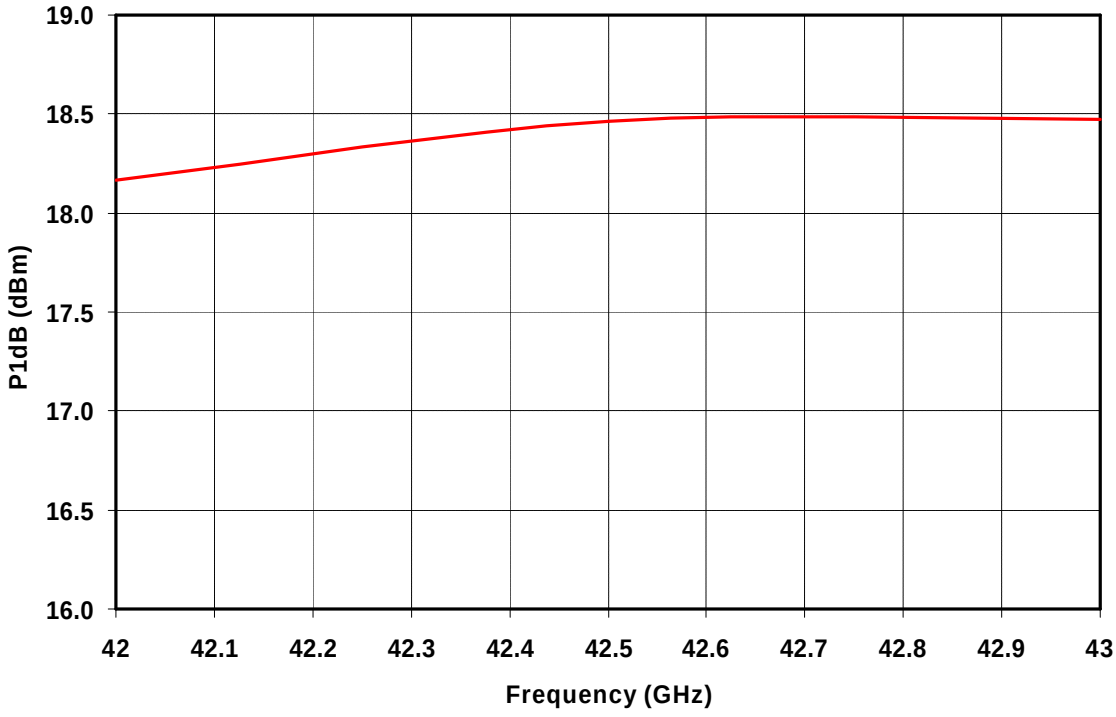
Preliminary Measured Data

Bias Conditions: Vd = 6 V, Id = 168 mA, Room Temp.





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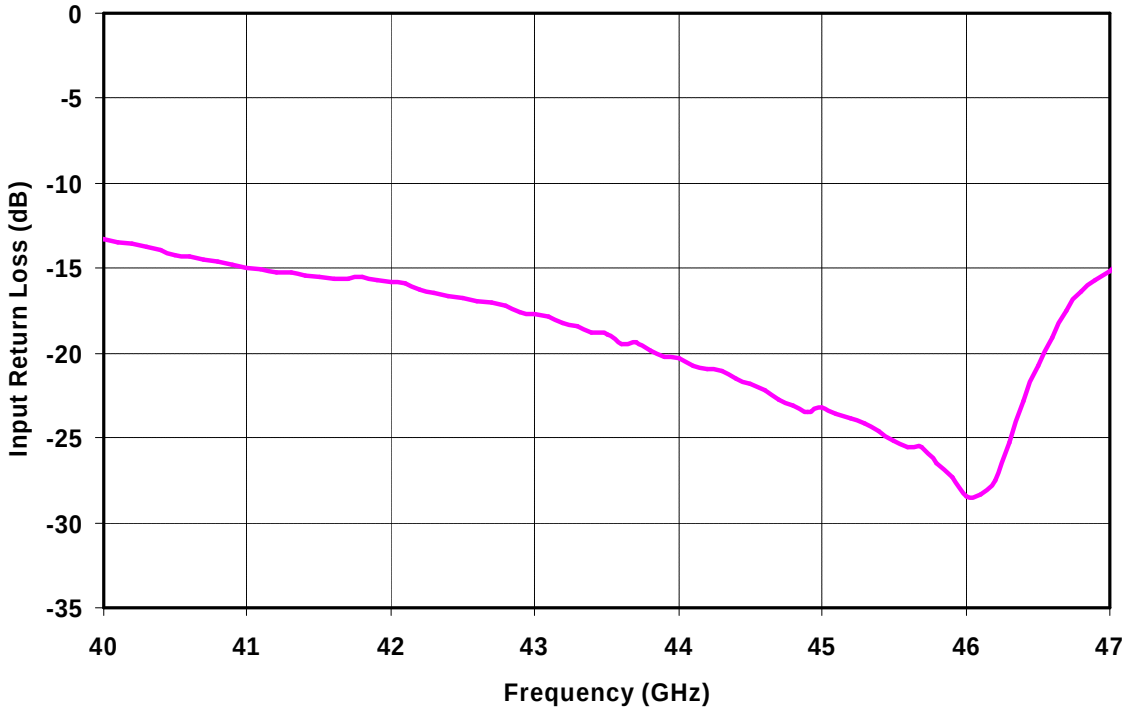

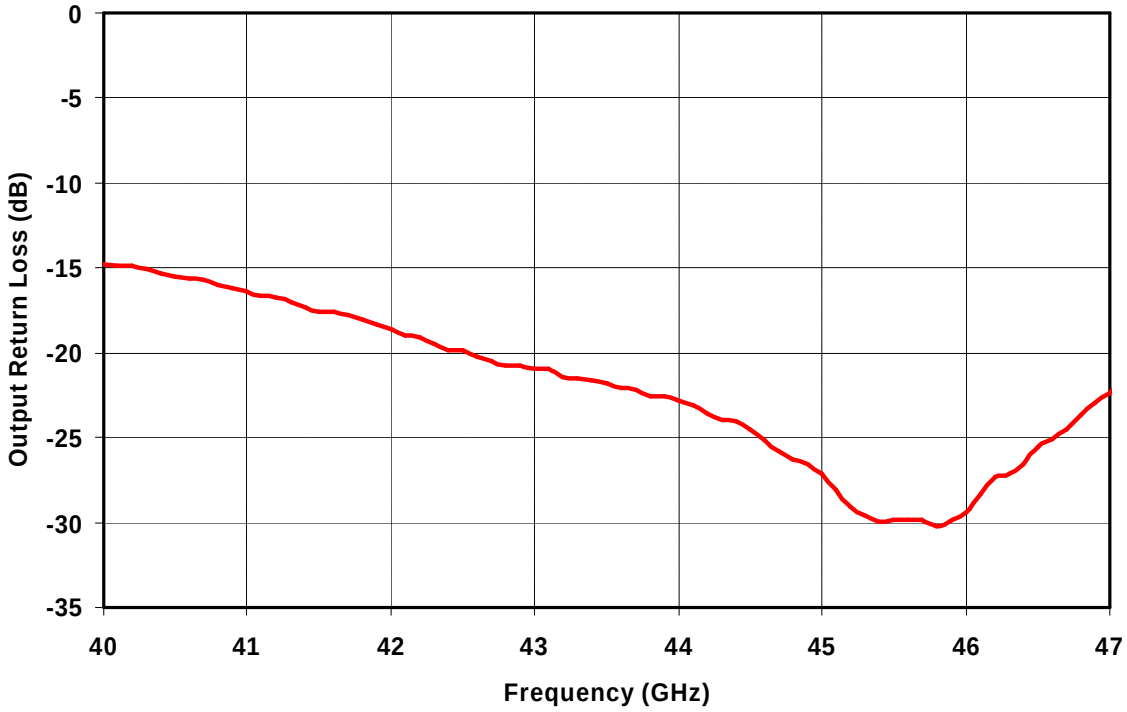

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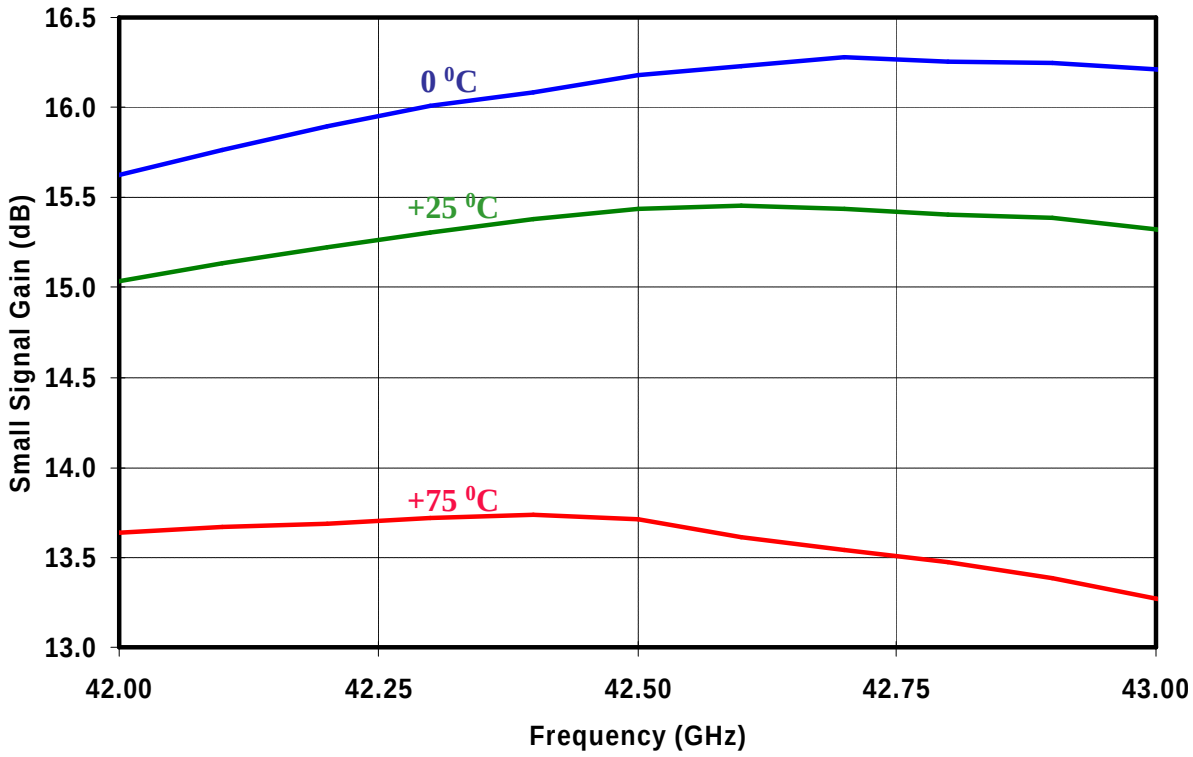

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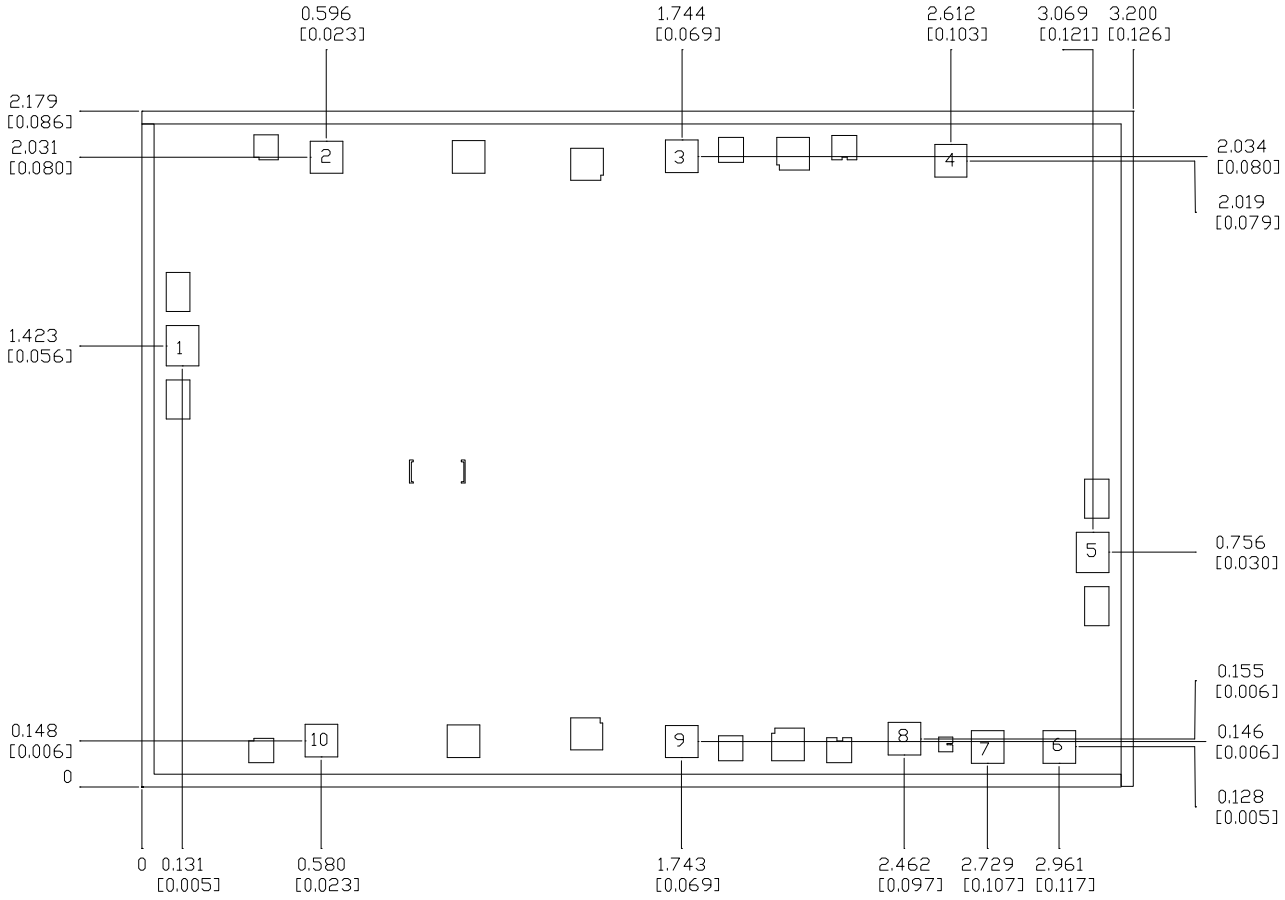
Mechanical Drawing



Units: Millimeters (inches)
Thickness: 0.100 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)
RF Ground is backside of MMIC

Bond pad #1	(RF Input)	0.105 x 0.130	(0.004 x 0.005)
Bond pad #2 & #10	(Vg)	0.105 x 0.105	(0.004 x 0.004)
Bond pad #3, #4, #8, #9	(Vd)	0.105 x 0.105	(0.004 x 0.004)
Bond pad #5	(RF Output)	0.105 x 0.130	(0.004 x 0.005)
Bond pad #6	(Vdet)	0.105 x 0.105	(0.004 x 0.004)
Bond pad #7	(Vcomp)	0.105 x 0.105	(0.004 x 0.004)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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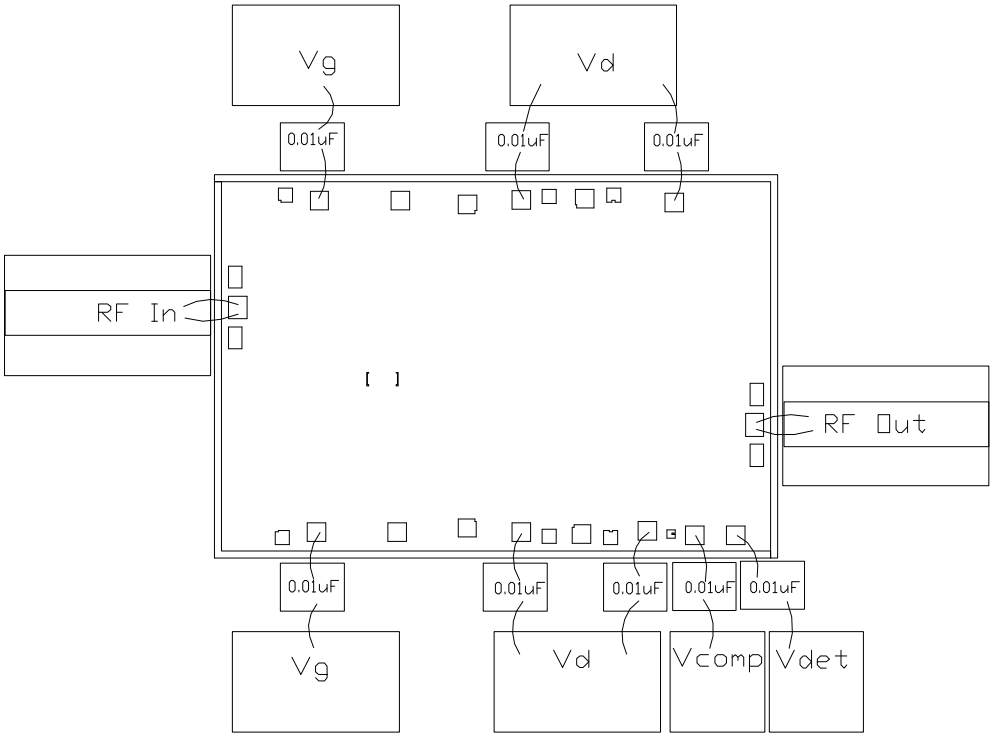
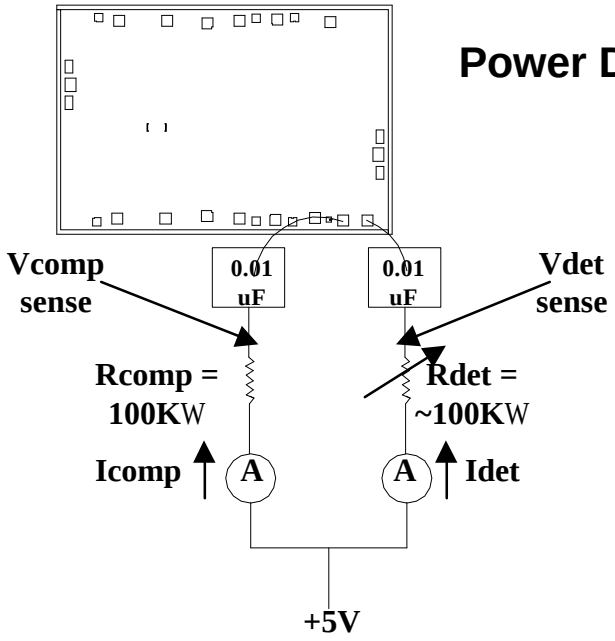
Chip Assembly Diagram



Power Detector Bias Circuit



Note:

1. With no RF power applied, adjust Rdet until Idet = Icomp (approx 41uA) and record Vdet.

2. Record Vdet as Pout increases. Detector sensitivity at a particular Pout is defined as delta between Vdet at Pout of interest and Vdet with no Pout.

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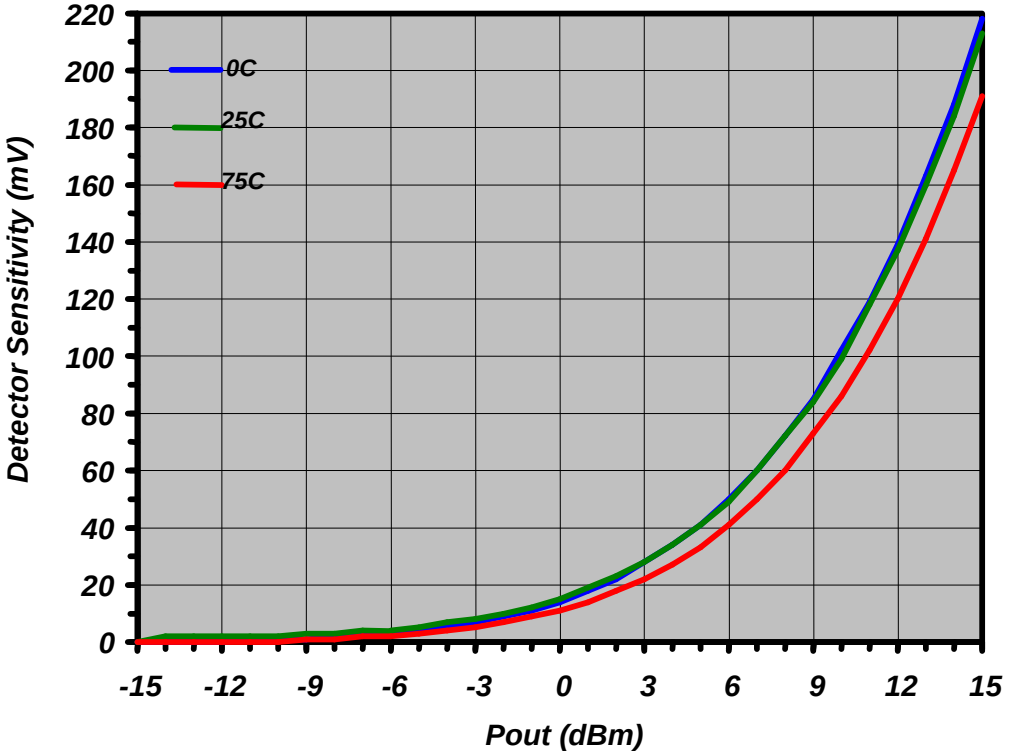
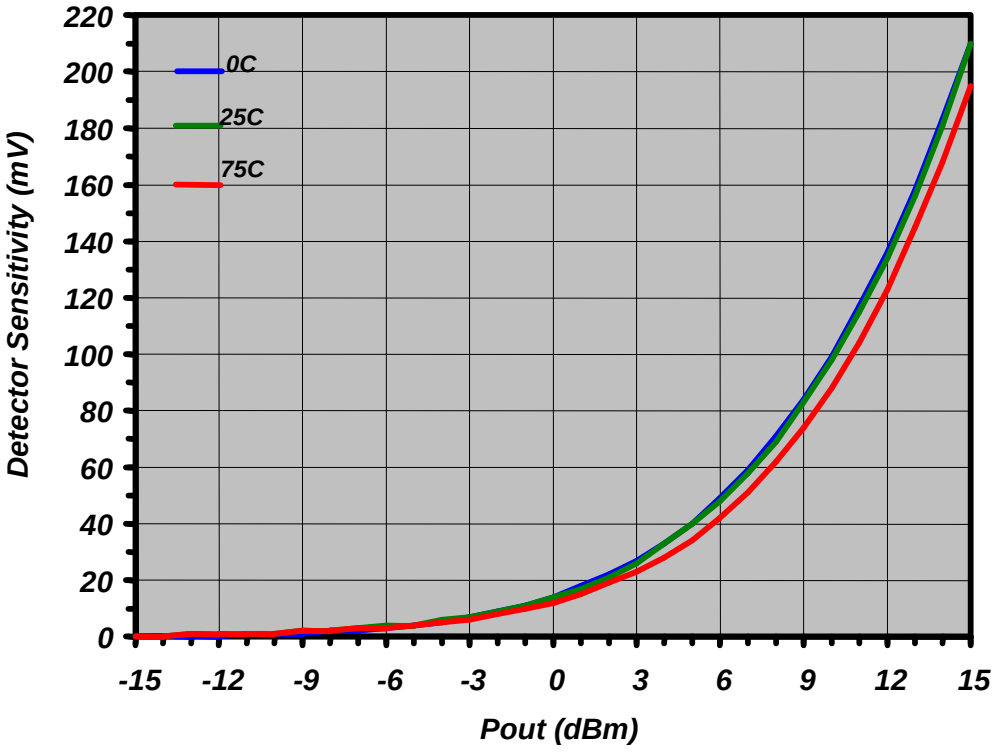
Power Detector performance over temperature





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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300^{0}C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200^{0}C.

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