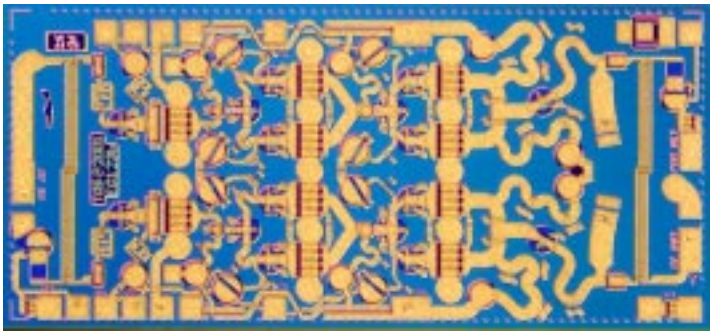
TriQuint SEMICONDUCTOR

Advance Product Information
June 18th, 2002

17 - 27 GHz High Power Amplifier TGA4502-EPU



Chip Dimensions 1.5 mm x 3.3 mm x .1mm

Key Features

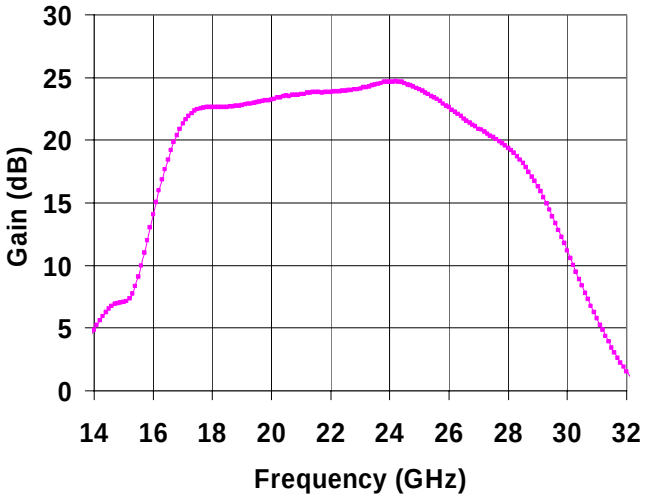
- 0.25 um pHEMT Technology
- 22 dB Nominal Gain
- 29 dBm Nominal P1dB
- 37dBm Nominal OTOI
- 15 dB Nominal Return Loss
- Bias 7V @ 750 mA
- Chip Dimensions 1.5 x 3.3 x .1mm

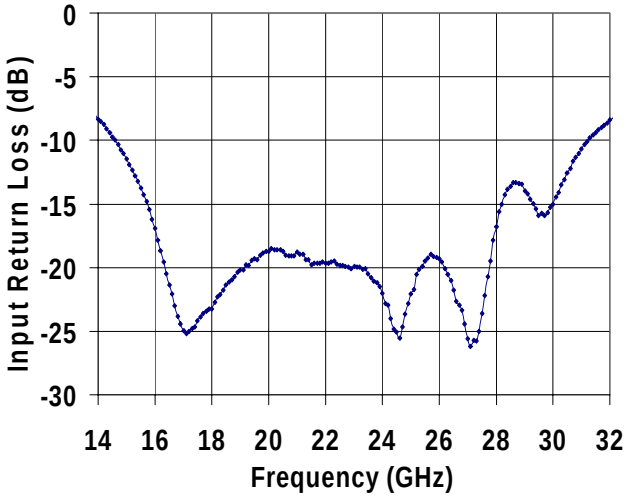
Primary Applications

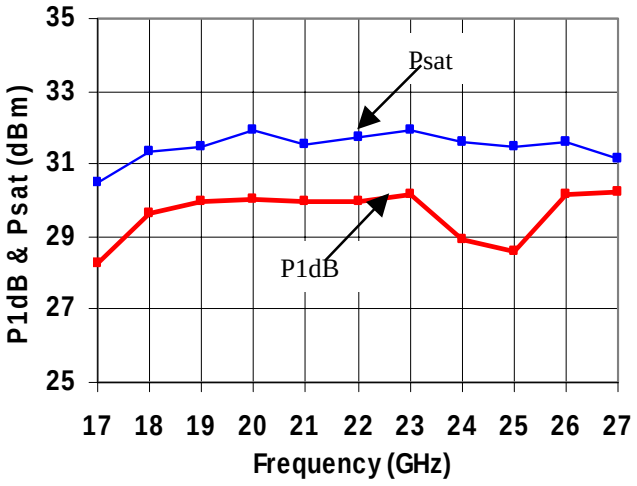
- K Band Sat-Com
- Point-to-Point Radio

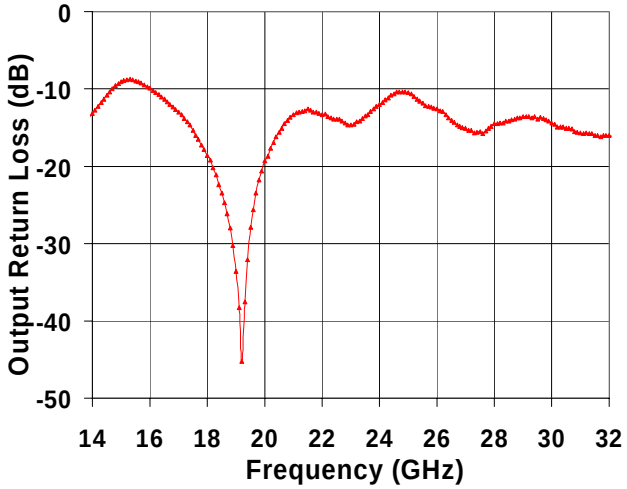
Preliminary Measured Performance

Bias Conditions: Vd = 7V, Id = 750mA









Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

TABLE I
MAXIMUM RATINGS 5/

SYMBOL	PARAMETER	VALUE	NOTES
V^+	Positive Supply Voltage	8 V	4/
V^-	Negative Supply Voltage Range	-5V TO 0V	
I^+	Positive Supply Current	880 mA	4/
$\mid I_G \mid$	Gate Supply Current	28 mA	
P_{IN}	Input Continuous Wave Power	26 dBm	
P_D	Power Dissipation	TBD	3/ 4/
T_{CH}	Operating Channel Temperature	150 ^{0}C	1/ 2/
T_M	Mounting Temperature (30 Seconds)	320 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings apply to each individual FET.

2/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

3/ When operated at this power dissipation with a base plate temperature of 70 ^{0}C, the median life is reduced from TBD to TBD hours.

4/ Current is defined under no RF drive conditions. Under RF drive, the supply current may rise to 1100 mA without damage. Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

5/ These ratings represent the maximum operable values for this device.

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TABLE II
DC PROBE TEST
(TA = 25 °C ± 5 °C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
I_{DSS1}	Saturated Drain Current	60	282	mA
G_m	Transconductance	132	318	mS
$V_{P1,2}$	Pinch-off Voltage	-1.5	-0.5	V
V_{P3-6}	Pinch-off Voltage	-1.5	-0.5	V
V_{P6-10}	Pinch-off Voltage	-1.5	-0.5	V
V_{BVGS1}	Breakdown Voltage Gate-Source	-30	-13	V

TABLE III
RF CHARACTERISTICS
(T_A = 25 °C ± 5°C)
Vd = 7V, I = 750 mA

SYMBOL	PARAMETER	TEST CONDITION	TYPICAL	UNITS
Gain	Small Signal Gain	F = 17 – 18 GHz F = 20 – 24 GHz F = 27 GHz	22 23 20	dB
IRL	Input Return Loss	F = 17 – 27 GHz	-20	dB
ORL	Output Return Loss	F = 17 – 27 GHz	-15	dB
P_{1dB}	Output Power @ 1dB Gain Compression	F = 17 – 27 GHz	30	dBm
OTOI	Output Third Order Intercept	F = 18 – 27 GHz	37	dBm

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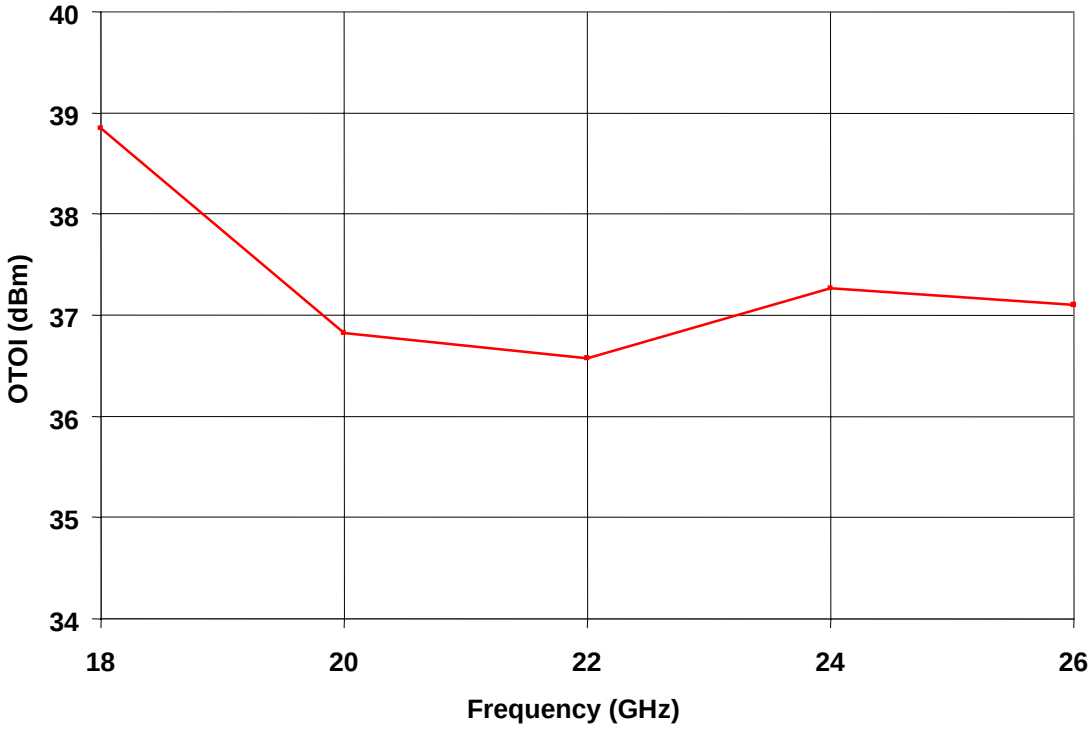
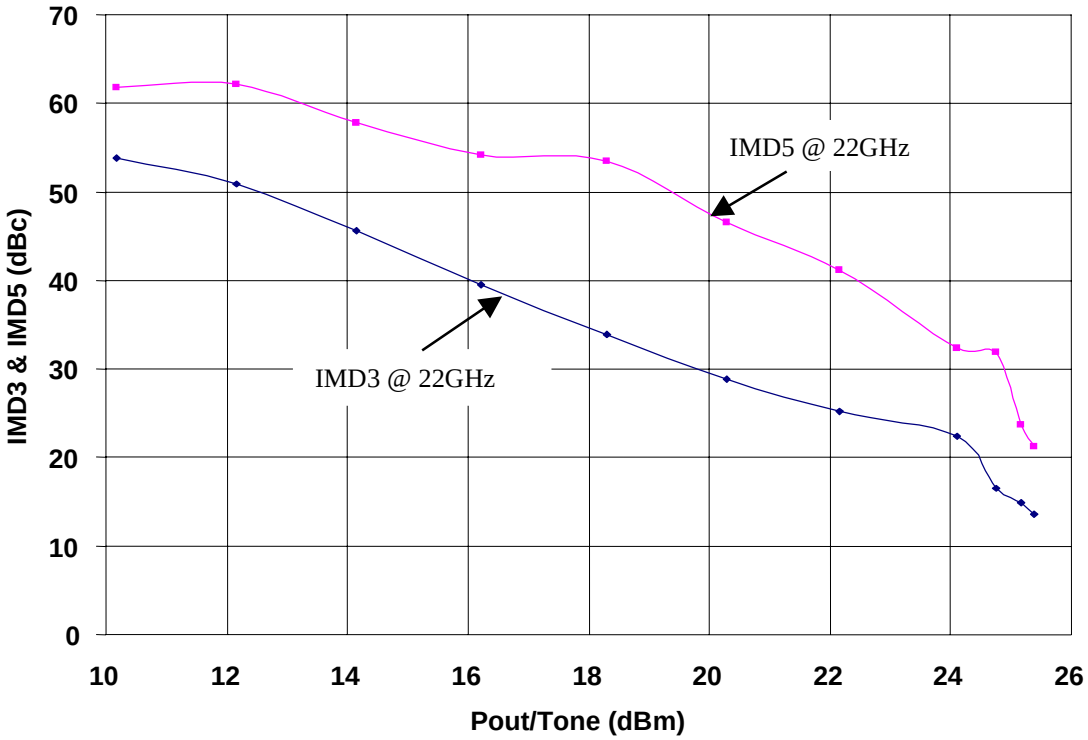
Measured Fixtured Data

Bias Conditions: Vd = 7V, Id = 750mA





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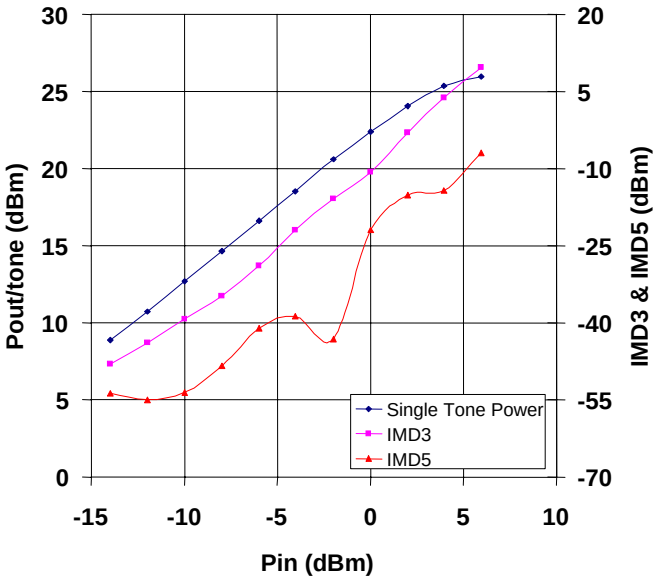
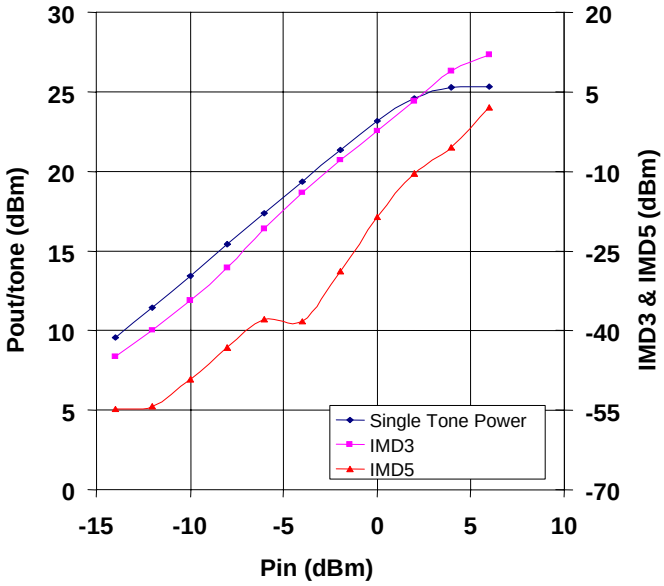
Measured Fixtured Data

Bias Conditions: Vd = 7V, Id = 750mA

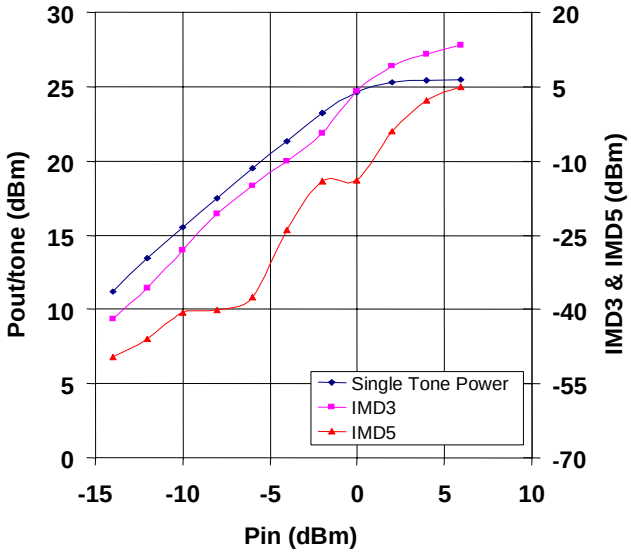
At Frequency: 18GHz



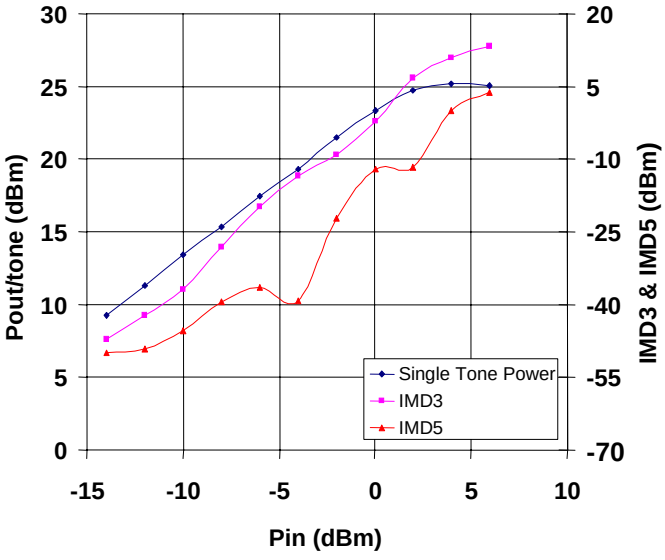
At Frequency: 20GHz



At Frequency: 24GHz



At Frequency: 26GHz



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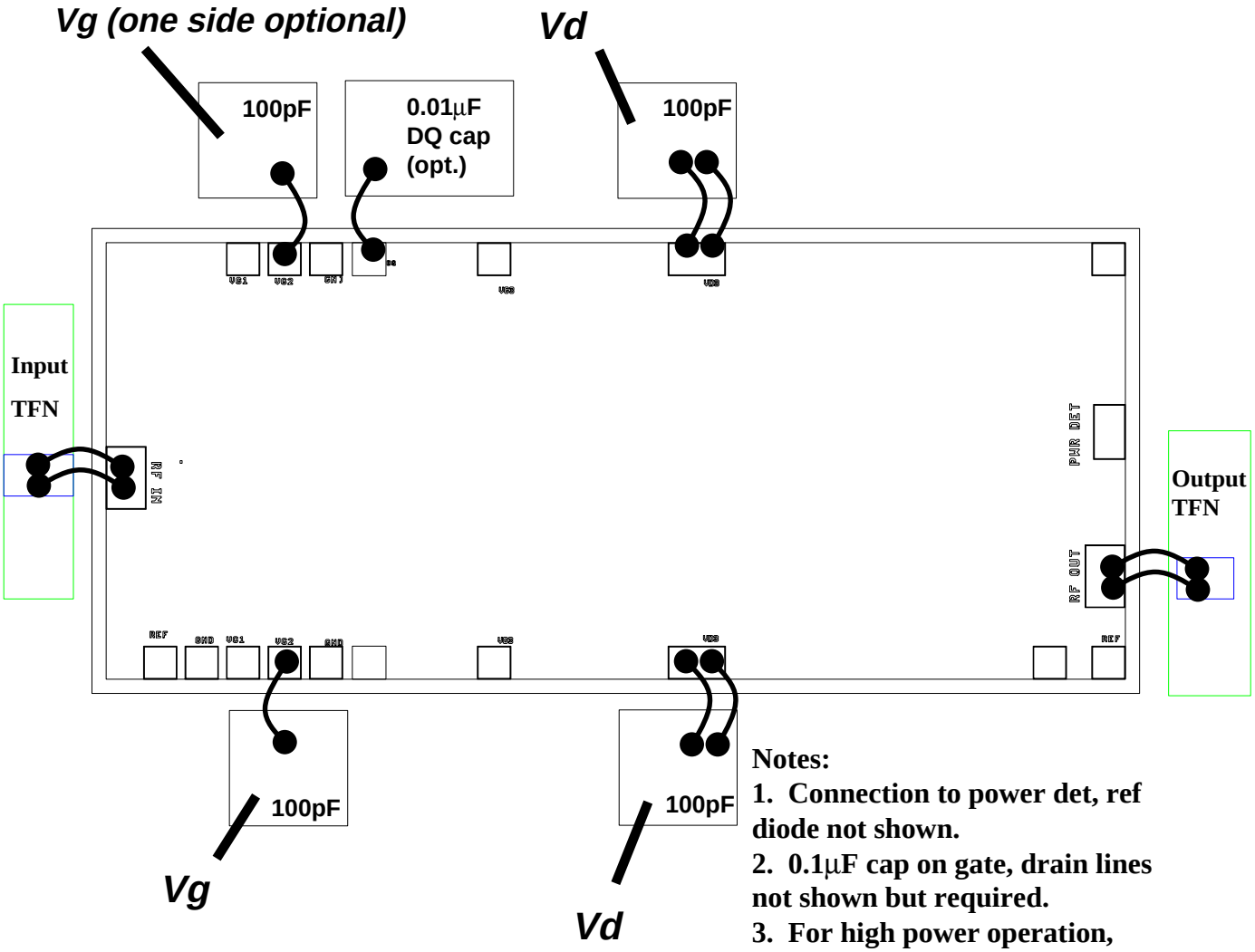
Recommended Assembly Diagram



Notes:

1. **Connection to power det, ref diode not shown.**
2. **0.1µF cap on gate, drain lines not shown but required.**
3. **For high power operation, gate voltage is recommended from both sides.**
4. **Drain voltage is required from both sides for Id > 780mA.**

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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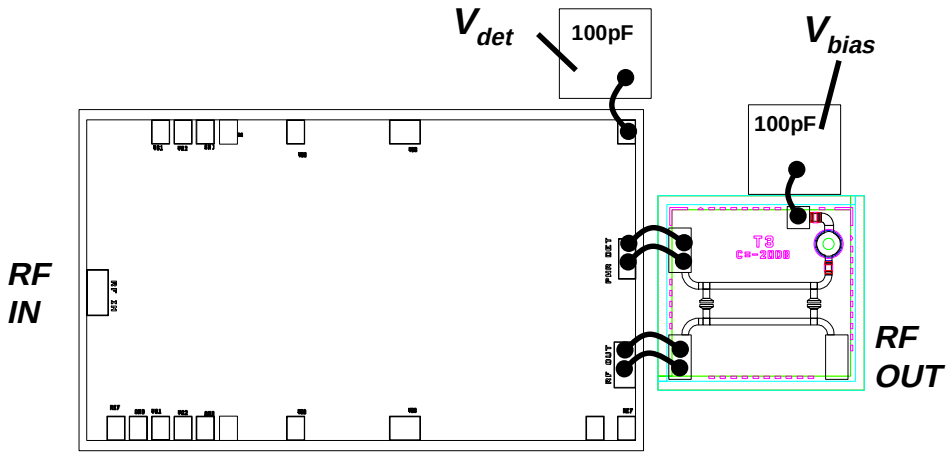
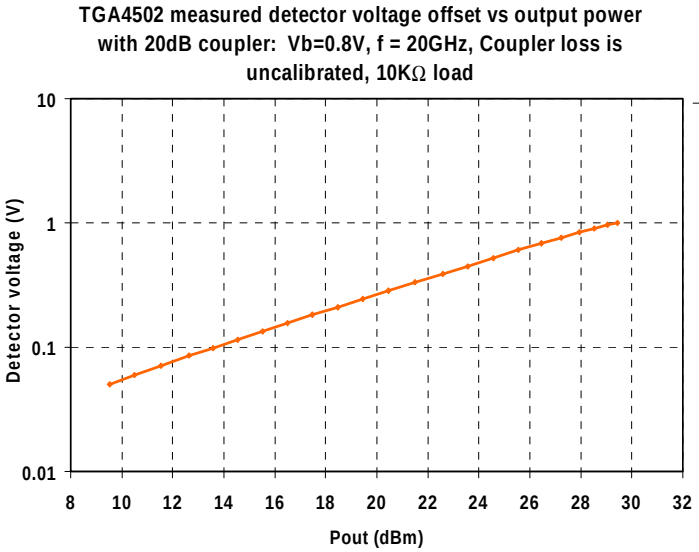
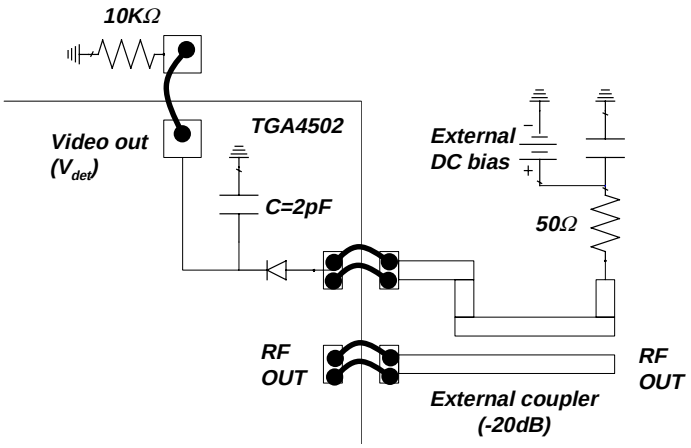
TGA4502 built-in power detector



TGA4502 with external test coupler
(amplifier bias connections not shown)

On-chip diode functions as envelope detector
External coupler and DC bias required





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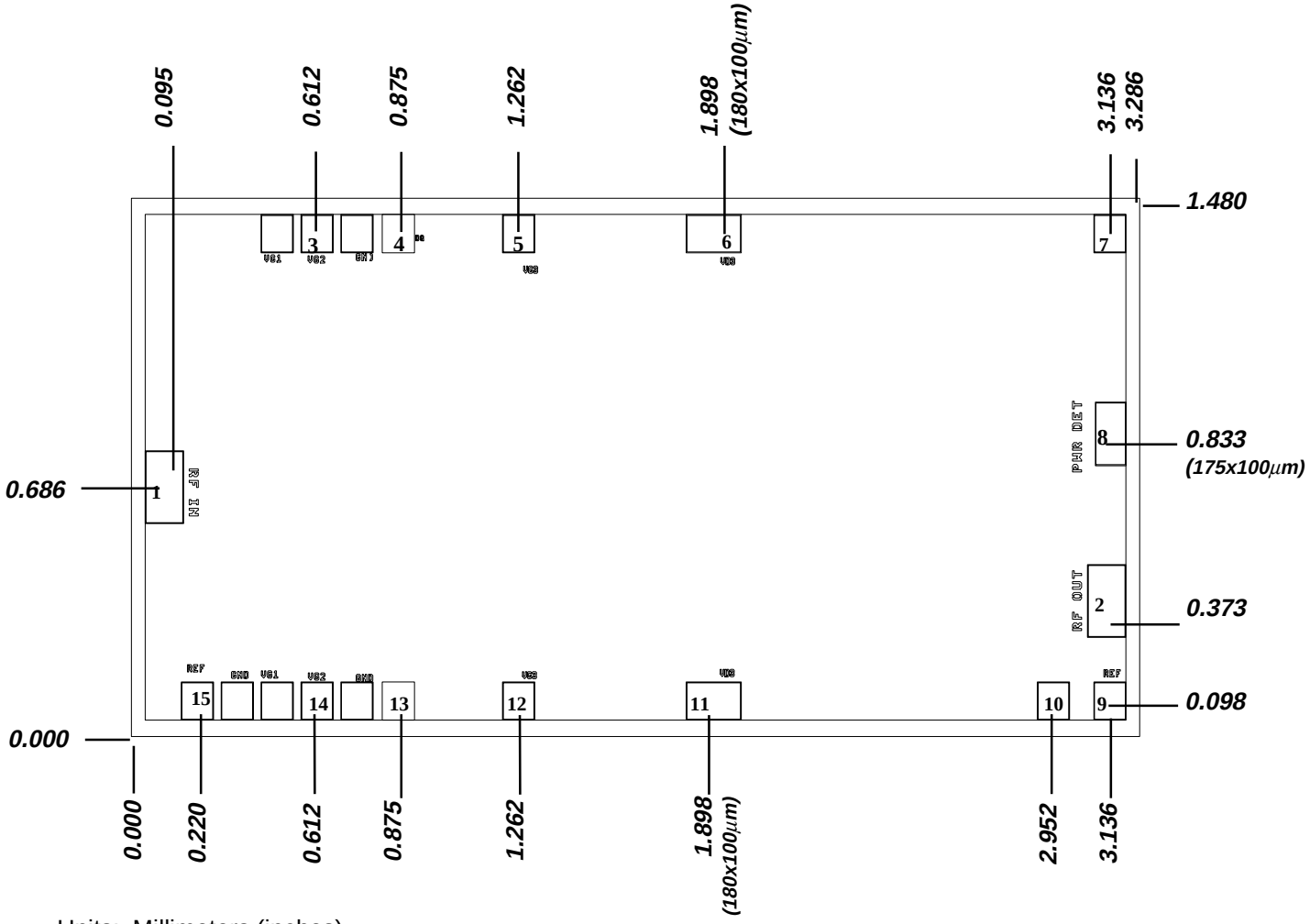
Mechanical Drawing



Units: Millimeters (inches)
Thickness: 0.1016 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance +/- 0.051 (0.002)

Bond pad #1	(RF Input)	200 x 100 µm	Bond pad #8	PWR DET	175 x 100 µm
Bond pad #2	(RF Output)	200 x 100 µm	Bond pad #9	REF2	105 x 105 µm
Bond pad #3	VG2	105 x 105 µm	Bond pad #10	REF1	105 x 105 µm
Bond pad #4	DQ	105 x 105 µm	Bond pad #11	VD3	180 x 100 µm
Bond pad #5	VG3	105 x 105 µm	Bond pad #12	VG3	105 x 105 µm
Bond pad #6	VD3	180 x 100 µm	Bond pad #13	DQ	105 x 105 µm
Bond pad #7	DET OUT	105 x 105 µm	Bond pad #14	VG2	105 x 105 µm
Bond pad #8	PWR DET	175 x 100 µm	Bond pad #15	REF3	105 x 105 µm

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

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