

# 10.7Gb/s Linear Optical Modulator Driver

# TGA4819-SL

OC-192 Metro and Long Haul Applications

Surface Mount Package



## Key Features and Performance

- Up to 10 V<sub>PP</sub> Linear Output Voltage
- 20 dB Gain
- Internal DC Blocks
- Single-ended Input / Output
- Small Form Factor
  - 11.4 x 8.9 x 2 mm
  - 0.450 x 0.350 x 0.080 inches

## Description

The TriQuint TGA4819-SL is part of a series of optical driver amplifiers suitable for a variety of driver applications.

The TGA4819-SL is a medium power wideband AGC amplifier that typically provides 20dB small signal gain with 20dB AGC range.

The TGA4819-SL is an excellent choice for applications requiring high drive combined with high linearity. The TGA4819-SL has demonstrated capability to deliver 10Vpp while maintaining output harmonic levels near -30dBc for a 2GHz fundamental.

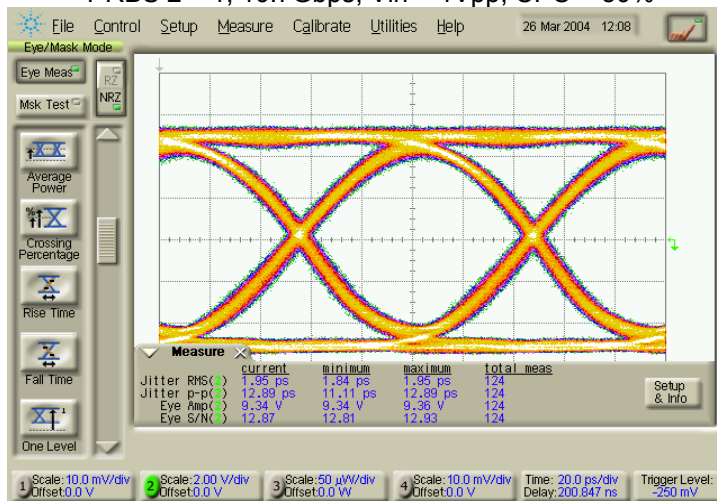
The TGA4819-SL requires a low frequency choke and control circuitry.

## Primary Applications

- Mach-Zehnder Linear Modulator Driver for Metro and Long Haul

## Preliminary Measured Performance

Bias Conditions: V<sub>D</sub> = 8V, V<sub>CTRL</sub> = +1V, I<sub>D</sub> = 310mA  
PRBS 2<sup>31</sup>-1; 10.7Gbps; Vin = 1Vpp; CPC = 50%



*Note: This device is early in the characterization process prior to finalizing all electrical specifications. Specifications are subject to change without notice.*

**TABLE I  
MAXIMUM RATINGS**

Symbol	Parameter	Value	Notes
V <sub>D</sub>	Drain Voltage	9 V	<u>1/</u> <u>2/</u>
V <sub>G</sub>	Gate Voltage Range	-3V to 0V	<u>1/</u>
V <sub>CTRL</sub>	Control Voltage Range	-3V to V <sub>D</sub> /2	<u>1/</u>
I <sub>D</sub>	Drain Supply Current (Quiescent)	400 mA	<u>1/</u> <u>2/</u>
I <sub>G</sub>	Gate Supply Current	5 mA	<u>1/</u>
P <sub>IN</sub>	Input Continuous Wave Power	23 dBm	<u>1/</u> <u>2/</u>
V <sub>IN</sub>	10.7Gb/s PRBS Input Voltage	4 V <sub>PP</sub>	<u>1/</u> <u>2/</u>
P <sub>D</sub>	Power Dissipation	3.1 W	<u>1/</u> <u>2/</u> <u>3/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>4/</u>
T <sub>M</sub>	Mounting Temperature (10 Seconds)	230 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub> at a package base temperature of 70°C
- 3/ When operated at this bias condition with a baseplate temperature of 70°C, the MTTF is reduced to 1.0E+6 hours
- 4/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

**TABLE II  
THERMAL INFORMATION**

Parameter	Test Conditions	T <sub>CH</sub> (°C)	R <sub>θJC</sub> (°C/W)	MTTF (hrs)
R <sub>θJC</sub> Thermal Resistance (Channel to Backside of Package)	V <sub>D</sub> = 8V I <sub>D</sub> = 350mA P <sub>DISS</sub> = 2.8W T <sub>BASE</sub> = 70°C	142.8	25.7	1.9E6

Note: Thermal transfer is conducted through the bottom of the TGA4819-SL package into the motherboard. The motherboard must be designed to assure adequate thermal transfer to the base plate.

**TABLE III**  
**RF CHARACTERIZATION TABLE**  
( $T_A = 25^\circ\text{C}$ , Nominal)  
( $V_D = 8\text{V}$ ,  $V_{CTRL} = +1\text{V}$ ,  $I_D = 310\text{mA} \pm 5\%$ ,  $V_G \approx -0.3\text{V}$ )

Parameter	Test Conditions	Typ	Units	Notes
Small Signal Bandwidth		8	GHz	
Small Signal Gain	100 MHz – 4 GHz 6 GHz 10 GHz 14 GHz	20 19 17 12	dB	<u>1/</u> <u>2/</u>
Input Return Loss	100 MHz – 14 GHz	15	dB	<u>1/</u> <u>2/</u>
Output Return Loss	100 MHz – 14 GHz	13	dB	<u>1/</u> <u>2/</u>
Small Signal AGC Range	Midband	20	dB	
Output Power @ $P_{1dB}$	2 GHz	25.5	dBm	<u>3/</u>

Note: Table III Lists the RF Characteristics of typical devices as determined by fixtured measurements.

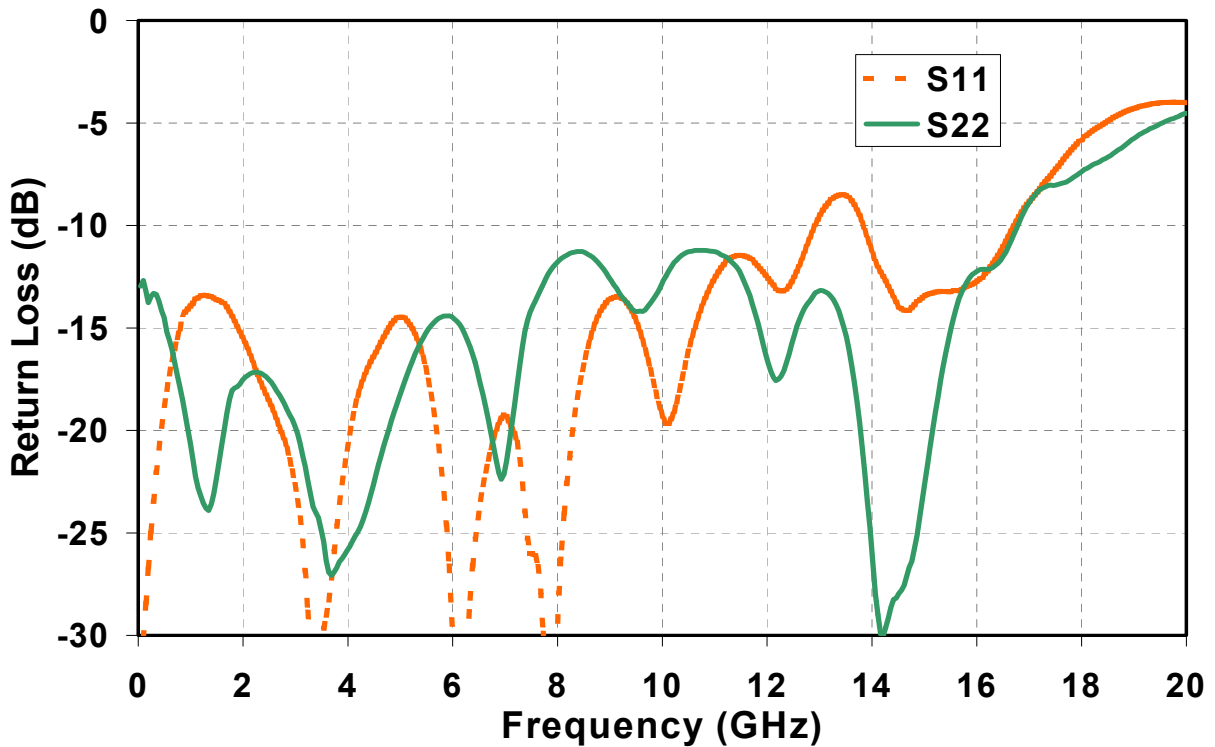
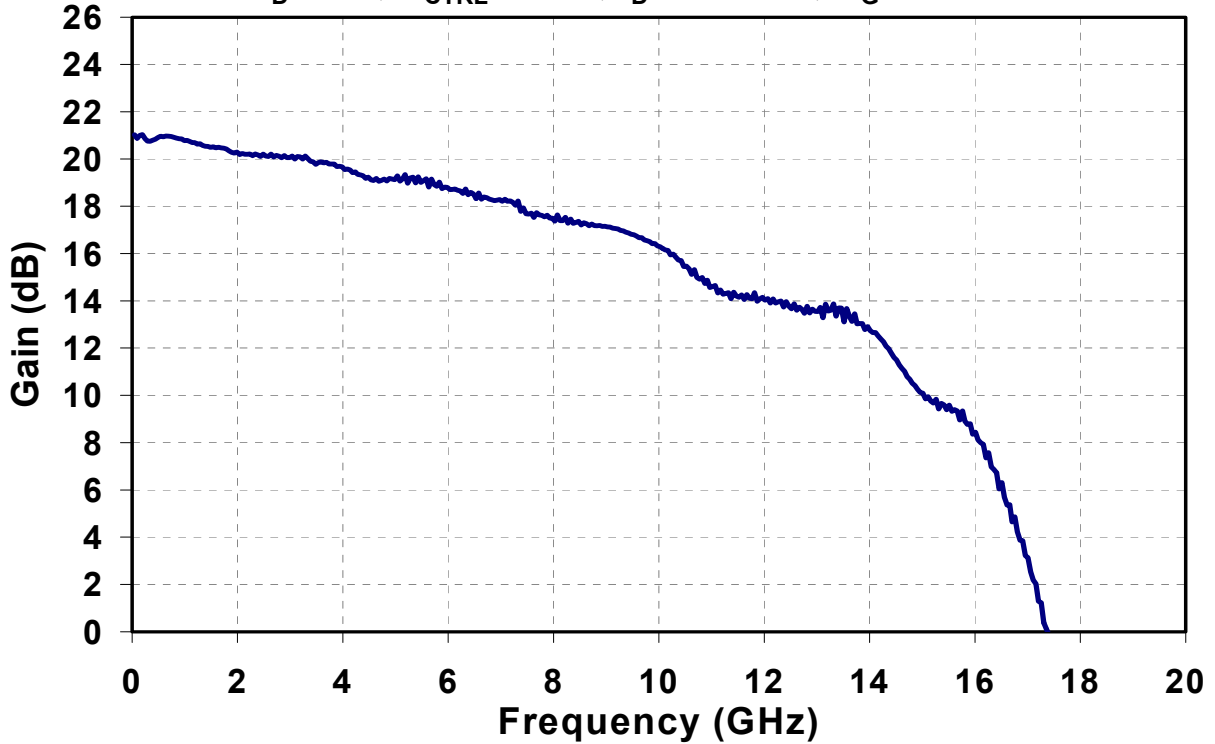
1/ Verified at package level RF test

2/ Package RF Test Bias:  $V_D = 8\text{V}$ ,  $V_{CTRL} = +1\text{V}$ , adjust  $V_G$  to achieve  $I_D = 310\text{mA}$

3/ Verified at die level on-wafer probe

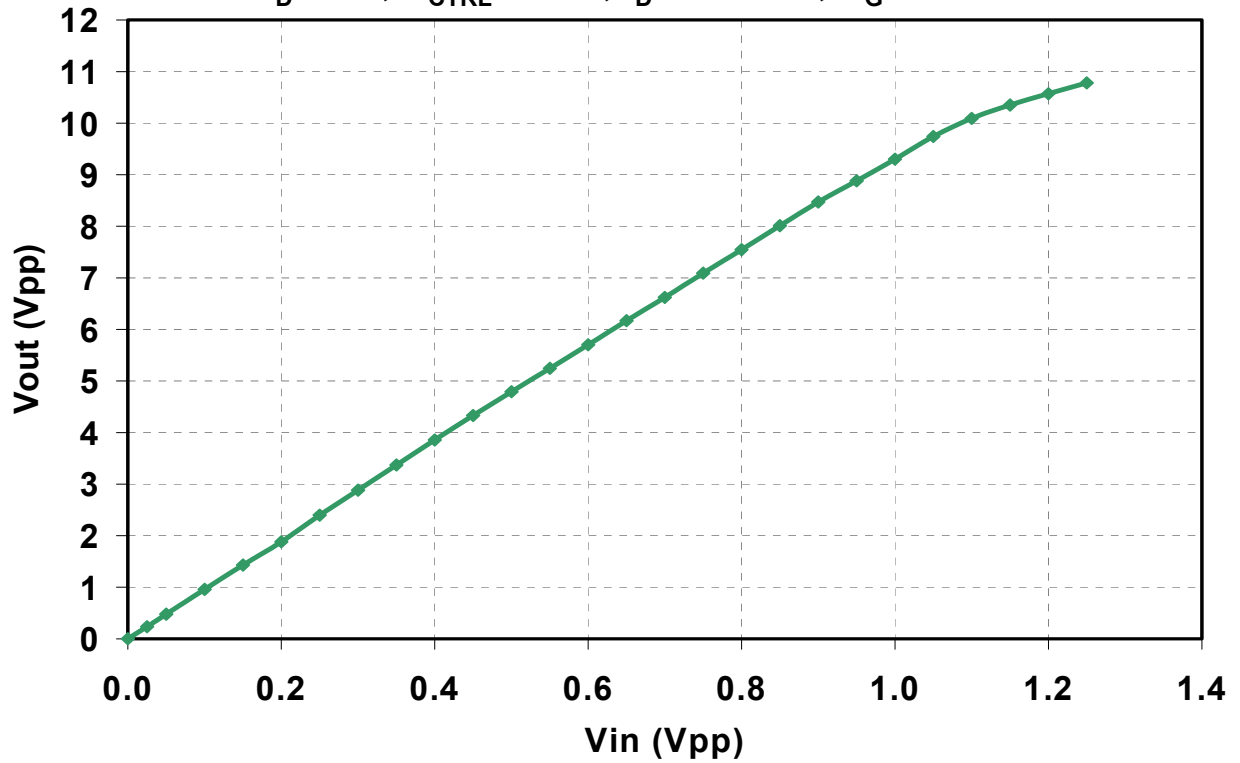
**Measured Performance**

$V_D = 8V$ ;  $V_{CTRL} = +1V$ ;  $I_D = 310mA$ ;  $V_G \approx -0.3V$



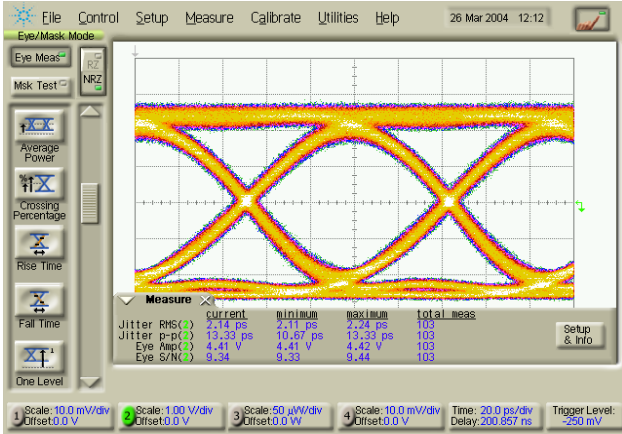
### Measured Performance

$V_D = 8V$ ;  $V_{CTRL} = +1V$ ;  $I_D = 310mA$ ;  $V_G \approx -0.3V$

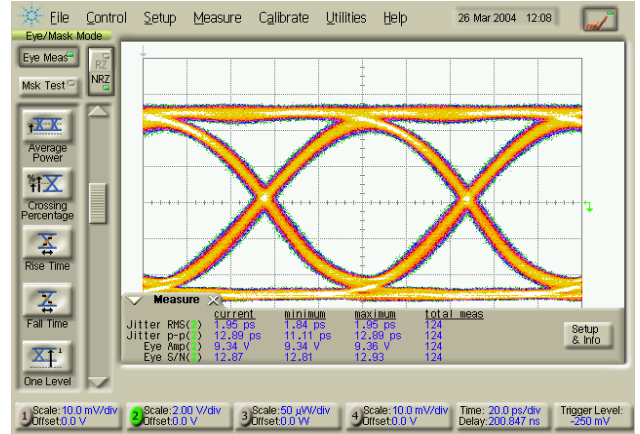


**Measured Performance**

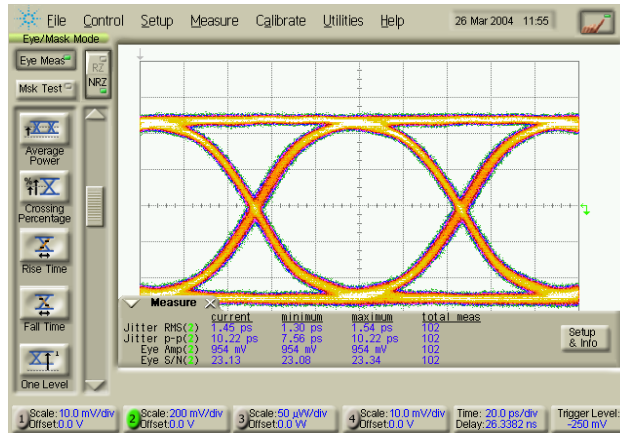
$V_D = 8V$ ;  $V_{CTRL} = +1V$ ;  $I_D = 310mA$ ;  $V_G \approx -0.3V$   
 PRBS 2<sup>31</sup>-1; 10.7Gbps; CPC = 50%



**$V_{in} = 500mV_{PP}$**

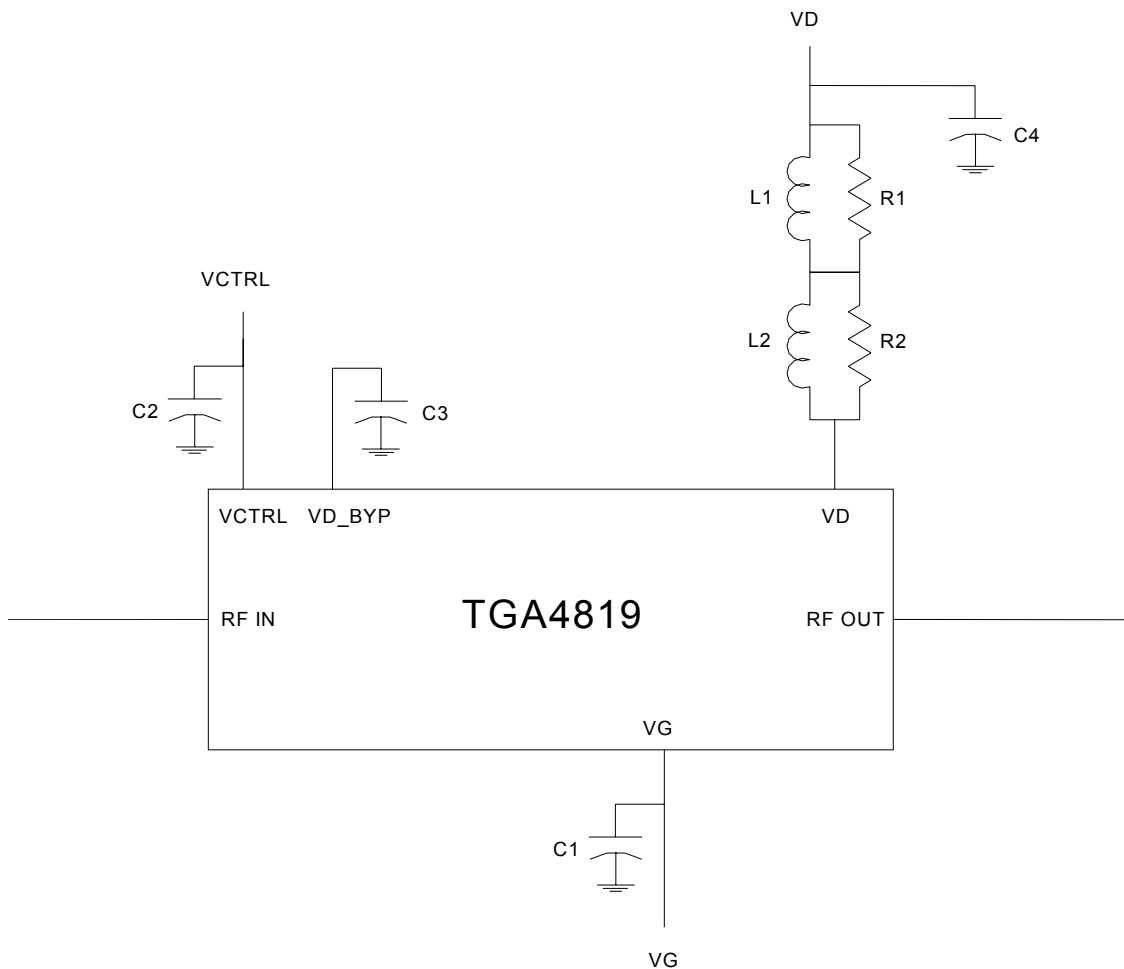


**$V_{in} = 1V_{PP}$**



**Input Signal  $V_{in} = 1V_{PP}$   
Includes 8GHz Bessel Filter**

## Application Circuit



**Note:**

1. C1 extends low frequency performance to 30 KHz. For applications requiring low frequency performance to only 100 KHz, C1 may be omitted
2. C2 is a power supply decoupling capacitor and may be omitted when driven directly with an op-amp.

## Application Circuit (Continued)

### Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C3	10uF Capacitor MLC Ceramic	AVX	0802YC106KAT
C2	0.01 uFCapacitor MLC Ceramic	AVX	0603YC103KAT
C4	10 uF Capacitor Tantalum	AVX	TAJA106K016R
L1	220 uH Inductor	Belfuse	S581-4000-14
L2	330 nH Inductor	Panasonic Coilcraft	ELJ-FAR33MF2 0603LS-331XJB
R1, R2	274 $\Omega$ Resistor	Panasonic	ERJ-2RKF2740X



## Laboratory - Bias ON/OFF Procedure

V<sub>D</sub>=8V, CPC=50%

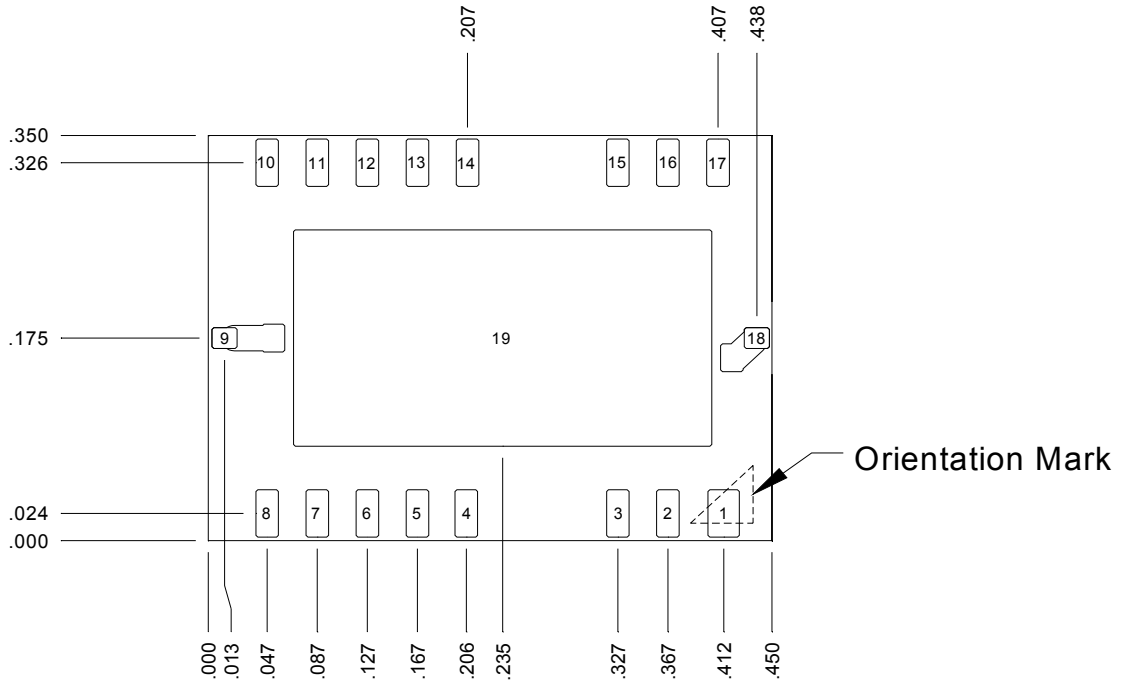
### Bias ON

1. Disable the output of the PPG
2. Set V<sub>D</sub> = 0V, V<sub>CTRL</sub> = 0V & V<sub>G</sub> = 0V
3. Set V<sub>G</sub> = -1.5V
4. Increase V<sub>D</sub> to 8V observing I<sub>D</sub>  
- Assure I<sub>D</sub> = 0mA
5. Set V<sub>CTRL</sub> = +1V  
- I<sub>D</sub> should still be 0mA
6. Make V<sub>G</sub> more positive until I<sub>D</sub> = 310mA.  
V<sub>G</sub> will be approximately -0.3V.
7. Enable the output of the PPG.
8. Output Swing Adjust: Adjust V<sub>CTRL</sub> slightly positive to increase output swing or adjust V<sub>CTRL</sub> slightly negative to decrease the output swing.
9. Crossover Adjust: Adjust V<sub>G</sub> slightly positive to push the crossover down or adjust V<sub>G</sub> slightly negative to push the crossover up.

### Bias OFF

1. Disable the output of the PPG
2. Set V<sub>CTRL</sub> = 0V
3. Set V<sub>D</sub> = 0V
4. Set V<sub>G</sub> = 0V

**Mechanical Drawing**



Bond Pad #1	N/C	0.025" x 0.041"	Bond Pad #11	N/C	0.018" x 0.041"
Bond Pad #2	N/C	0.018" x 0.041"	Bond Pad #12	VD	0.018" x 0.041"
Bond Pad #3	N/C	0.018" x 0.041"	Bond Pad #13	N/C	0.018" x 0.041"
Bond Pad #4	N/C	0.018" x 0.041"	Bond Pad #14	N/C	0.018" x 0.041"
Bond Pad #5	N/C	0.018" x 0.041"	Bond Pad #15	N/C	0.018" x 0.041"
Bond Pad #6	VG	0.018" x 0.041"	Bond Pad #16	VD_BYP	0.018" x 0.041"
Bond Pad #7	N/C	0.018" x 0.041"	Bond Pad #17	VCTRL	0.018" x 0.041"
Bond Pad #8	N/C	0.018" x 0.041"	Bond Pad #18	RF In	0.020" x 0.018"
Bond Pad #9	RF Out	0.020" x 0.018"	Bond Pad #19	GND	0.334" x 0.187"
Bond Pad #10	N/C	0.018" x 0.041"			

**NOTES:**

1. Maximize number of vias on attachment area of PCB for Bond Pad #19. This is required electrical and thermal conduction
2. Pad sizes for RF input and output (#18, #9) are shown for soldermask opening. Solder should not be applied outside of this area.

**Dimensions:** Inches

**Tolerances:** Length & Width: ±0.003"  
 Height: ±0.006"  
 Adjacent Pad to Pad Spacing: ±0.0002"  
 Pad Size: ±0.001"

**Package Backside Material:** Material: RO4003 (0.008" thk) w/ 0.5oz Cu (0.0007" thk)  
 Plating: 100 - 350µin Ni underplate w/ 5 - 10µin Au overplate

## Assembly of a TGA4819-SL Package onto a Motherboard

### Manual Assembly for Prototypes

1. Clean the motherboard with Acetone and rinse with alcohol and DI water. Allow the motherboard to fully dry.
2. Using a standard SN63 or lead-free solder paste, dispense solder paste dots of 5 to 15 mil in diameter to the motherboard. Assure that there is a minimum of 5 mils and a maximum of 10 mils between the edge of each solder paste area and the closest edge of the ground pad.
3. Manually place a TGA4819-SL on the motherboard with correct orientation and good alignment. The alignment can be determined manually by centering the package on the motherboard. The RF traces (pin 1 and pin 10) are located along the center horizontal axis of the package.
4. Reflow the assembly on a hot plate with the surface temperature of the plate near 230 °C for 5 to 6 seconds (for SnPb).
5. Let the assembly completely cool down. *This package has little or no tendency to self-align during the reflow.*
6. Clean the assembly with acetone and rinse with alcohol and DI water.

### Typical Solder Reflow Profiles

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

**CAUTION: The TGA4819-SL contains GaAs MMIC devices that are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**