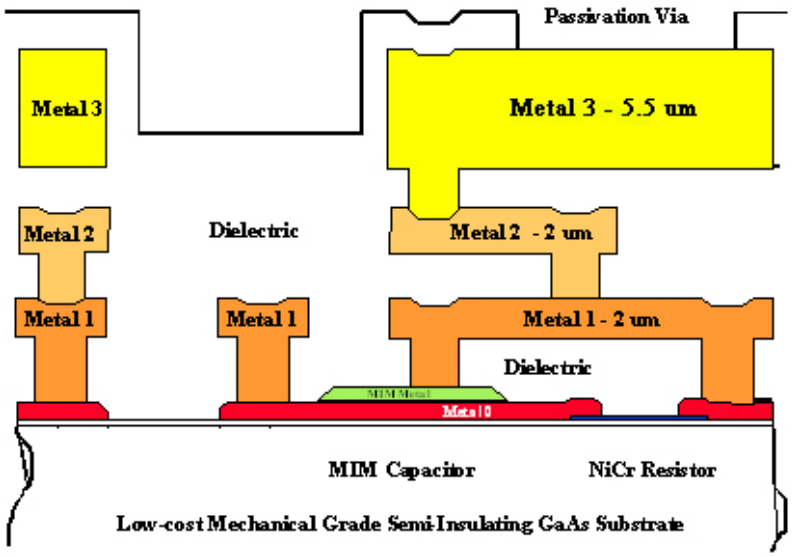
TQRLC

Advanced Passives Foundry Service



TQRLC Process Cross-Section

General Description

TriQuint's TQRLC is a pure passives process. It is targeted at high performance, small size passive-only circuits and utilizes over 9 µm of gold metal. High density interconnections are accomplished with three thick global and one surface metal interconnect layers. The four metal layers are encapsulated in a high performance, low dielectric constant material that allows wiring flexibility and plastic packaging simplicity. Precision NiCr resistors, inductors, and high value MIM capacitors are available. The process is based on the TQTRx process, currently TriQuint's highest volume process. The TQRLC process is available on 150-mm (6 inch) wafers.

Features

- Thick 4 Layer Metal; > 9 µm total thickness
- High Density Interconnects:
  - 3 Global
  - 1 Local
- High-Q Passives; Inductor Q >50 @ 2 GHz
- Low Cost: Passives Only
- Thin Film Resistors
- Dielectric Encapsulated Metals
- Planarized Surface; simplified plastic packaging
- Volume Production Process

Applications

- Passive Components:
  - Phase Shifters
  - Baluns
  - Transformers
  - Couplers
  - Mixers (with off-chip diode arrays)
- Circuits Requiring High-Q Passive Elements
- Matching Circuits
- RF Module Front-End Filters
- General RF and Microwave Impedance Matching

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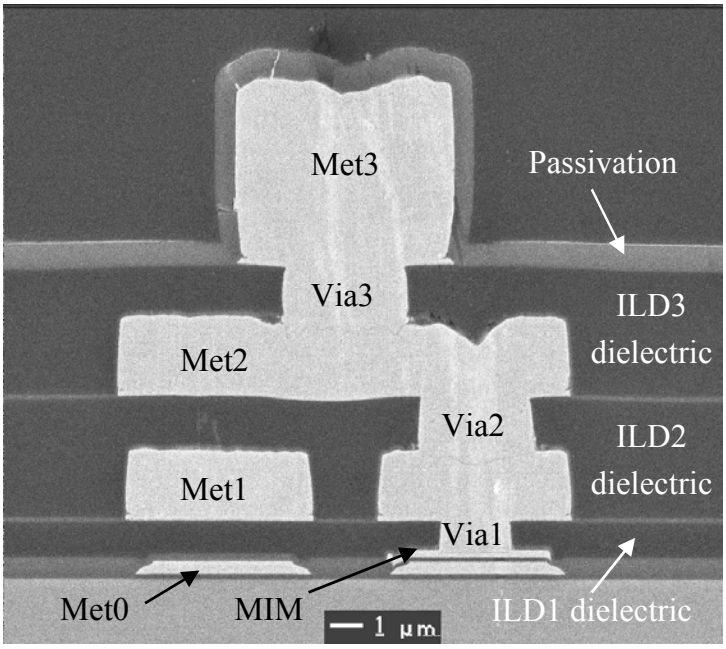
TQRLC Process Details

Element	Parameter	Value	Units
Interconnects	Metal Layers	Four: 0.4,2,2,5.5	µm
	Space Width	Met3= 5; Met1&2= 3	µm
	Trace Width	Met3= 5; Met1&2= 2	µm
BCB Dielectric	Nom. Thickness	ILD1= 1 +/-0.1; ILD2&3= 3.2 +/- 0.2	µm
	Dielectric Constant	2.8	
MIM Caps	Values	600	pF/mm2
Resistors	NiCr	50+/-3	Ohms/sq
Vias		No	
Mask Layers	No Vias	10	

Maximum Ratings

Capacitor Breakdown Voltage	40	V



Example of Metal Stack Configurations Possible with TQRLC Process; Edge- or Parallel-Coupled Structures Through The ILD Layers Are Also Possible.

Specifications Subject to Change

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Prototyping and Development

- Prototype Development Quickturn (PDQ):
  - Shared Mask Set;
  - Run Monthly;
  - Hot Lot Cycle Time;
- Prototype Wafer Option (PWO):
  - Customer-specific Masks, Customer Schedule
  - 2 wafers delivered
  - With thinning and sawing

Process Qualification Status

- TQRLC is a fully-released process
- Reliability Reports
  - TQRLC Process Qualification
  - TQTRx Element Qualification Report
- For more information on Quality and Reliability, contact TriQuint or visit: www.tqs.com/Manufacturing/QR/bdy_qr-pubs.htm.

Design Tool Status

- Design Manual Available Now
- Device Library of Circuit Elements includes Thin Film Resistors, Capacitors, Inductors
- Agilent ADS Definition File for E-M Simulation Now
- Layout/Verification Kit for ICEditors
- Cadence Layout Library Available Now

Applications Support Services

- Tiling of GDSII Stream Files including PCM
- Design Rule Check Services
- Layout versus Schematic Check Services
- Engineering Services:
  - Packaging Development
  - Test Development Engineering (on-wafer and packaged parts)
  - Thermal Analysis Engineering
  - Yield Enhancement Engineering
- Part Qualification Services
- Failure Analysis

Training

- GaAs Design Classes:
  - Half Day Introduction; Upon Request
  - Four Day Technical Training; Fall & Spring at TriQuint Oregon facility
- For Training Schedules, please visit: www.triquint.com/foundry/

Manufacturing Services

- Mask Making
- Production 150 mm Wafer Fab
- Wafer Thinning
- Wafer Sawing
- DC Die Sort Testing
- RF On-Wafer Testing
- Plastic Packaging
- RF Packaged Part Testing

Please contact your local TriQuint Semiconductor Representative or Foundry Services Staff for additional information:
E-mail: sales@triquint.com Phone: (503) 615-9000 Fax: (503) 615-8905