28-35 GHz Power Amplifier

GaAs Monolithic Microwave IC

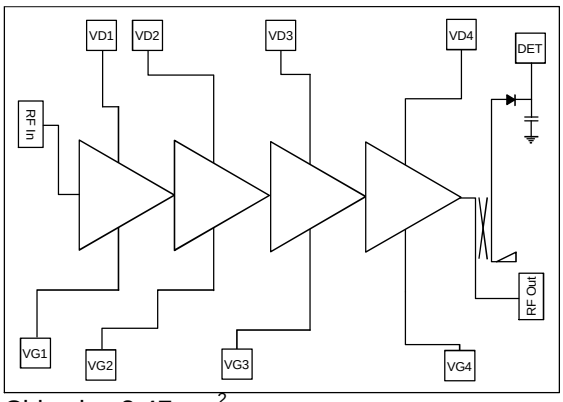
Preliminary

Description

The CHA5130 is a compact four-stage PHEMT HPA MMIC designed for VSAT ground terminals and other radio applications. It provides typically 28dBm nominal output power at 1dB gain compression over the 28-35 GHz frequency range, and 18dB small signal gain.

The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

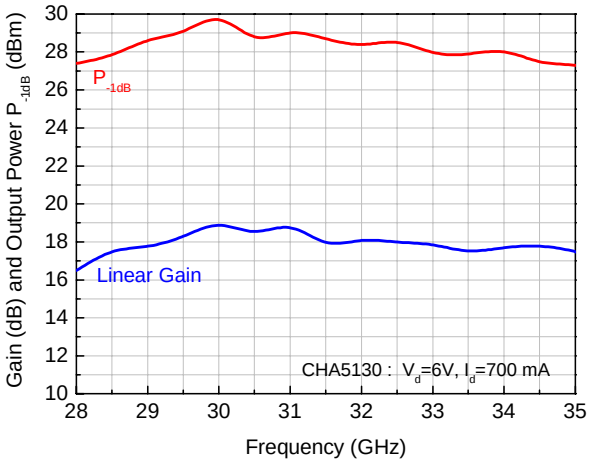
The circuit is manufactured with a 0.25µm gate length power PHEMT process on 70µm substrate, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Chip size 2.47mm^2

Main Features

- Broadband performances : 28-35GHz
- 18dB ± 1 dB linear gain
- 28dBm output power at 1dB comp
- Integrated output power detector
- Chip size : 1.32 X 1.87 X 0.07mm^3



Typical in JIG test fixture measurements

Main Characteristics

Tamb = +25°C, Vd = 6V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	28		35	GHz
G	Small signal gain	17	18		dB
P1dB	CW output power at 1dB gain compression	27	28.5		dBm
Vd	Drain bias voltage		6		V
Id	Bias current		700	1000	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical characteristics in JIG test fixture

Tamb = +25°C, Vd = 6V, Id=700mA (typically Vg=-0.4V)

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	28		35	GHz
G	Small signal gain (1)	17	18		dB
ΔG	Small signal gain flatness		± 1		dB
P1dB	CW output power at 1dB gain compression (1)	27	28.5		dBm
Psat	Saturated output power (1)	28	29.5		dBm
IP3	3rd order intercept point (1)		34		dBm
RLin	Input return loss (1)		-10	-8	dB
RLout	Output return loss (1)		-10	-8	dB
Is	Reverse Isolation (1)		35		dB
Vd	Drain bias voltage		6		V
Vg	Gate bias voltage		-0.4		V
Id	Bias current		700		mA

(1) These values are representative for CW JIG test fixture measurements, that are made with bond wires at RF ports. The given values include the test fixture loss correction.

Absolute Maximum Ratings (2)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5	V
Id	Bias current	1000	mA
Vg	Min. and max. gate bias voltage	-2.5 ~ 0	V
Pin	Maximum peak input power overdrive (3)	+15	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(2) Operation of this device above anyone of these parameters may cause permanent damage.
(3) Duration < 1s.

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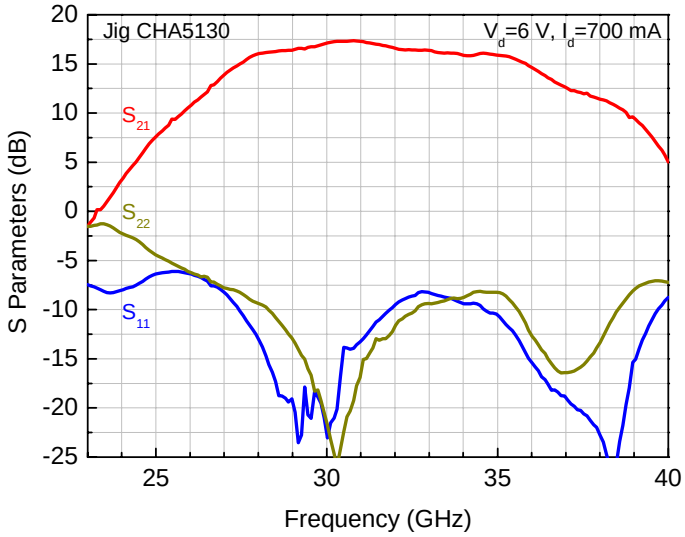
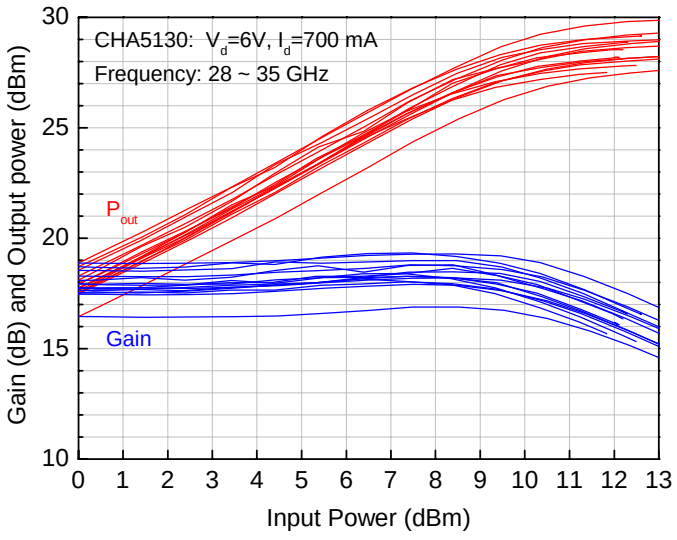
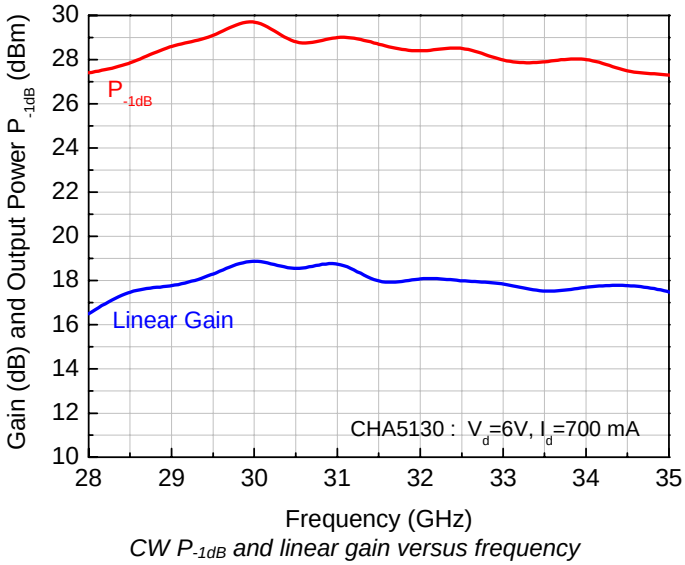
Typical CW performance in JIG test fixture @ Tamb=25°C



Typical in JIG test fixture S-parameters measurements



Typical CW P_{out} versus P_{in} characteristics



CW P_{-1dB} and linear gain versus frequency

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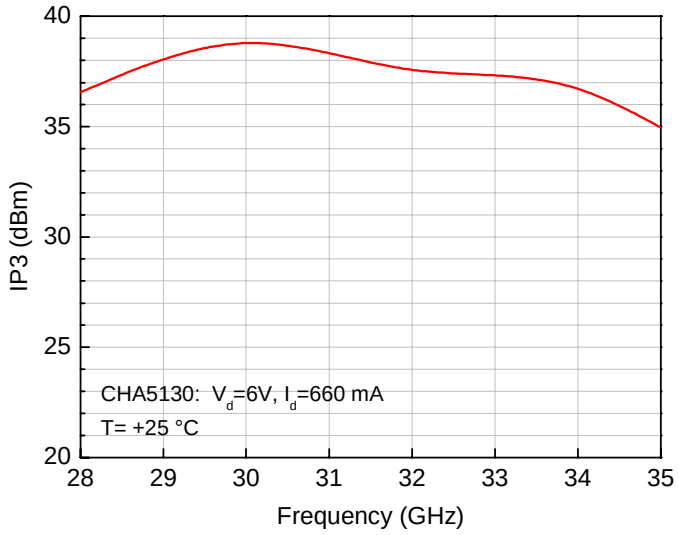
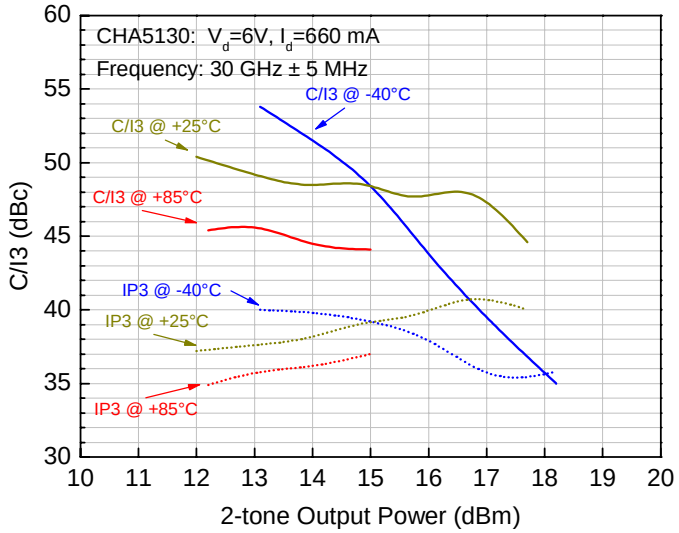
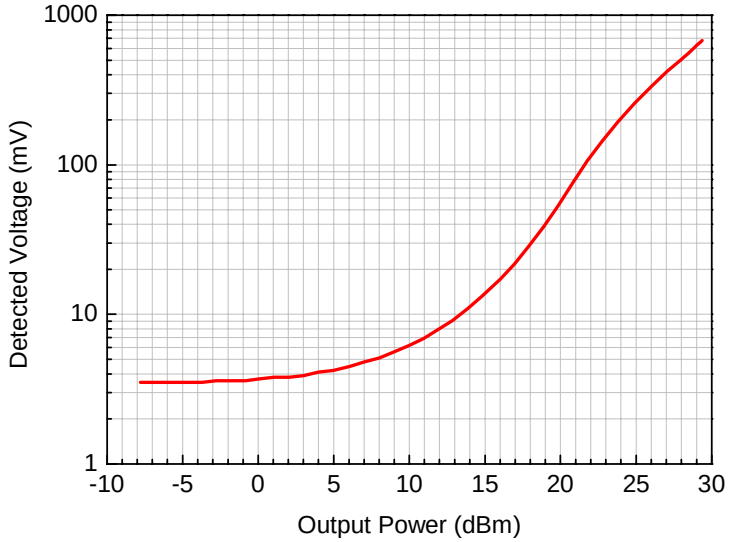


Typical CW IP3 versus frequency at optimum bias for linearity (V_d=6.0V, I_d=660 mA)



C/I3 and IP3 over P_{out} and temperature at 30 GHz and optimum bias for linearity (V_d=6.0V, I_d=660 mA)



Output power detector characteristic @ 30 GHz, V_d=6.0V, I_d=700 mA)

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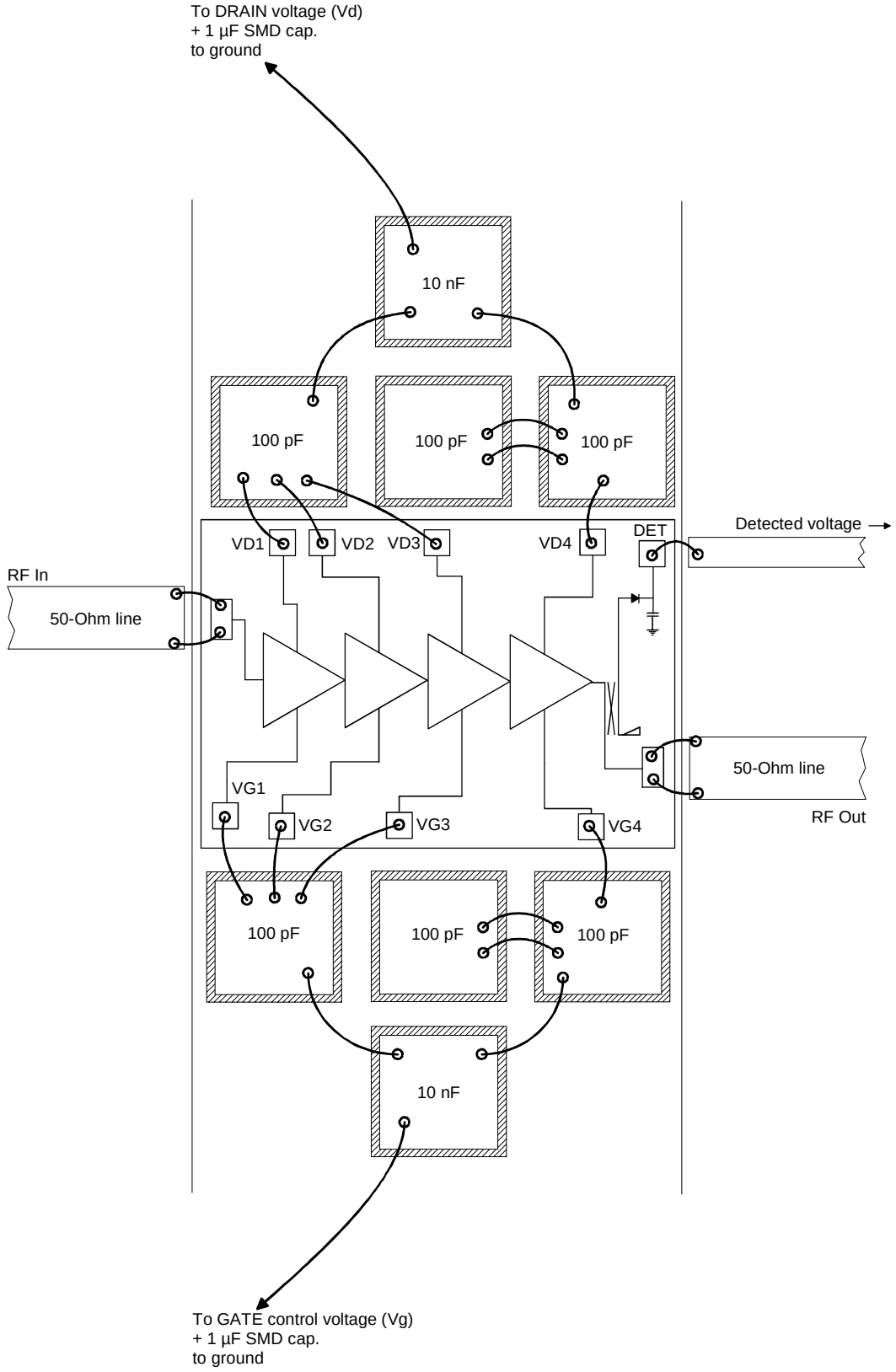
Recommended Chip Assembly



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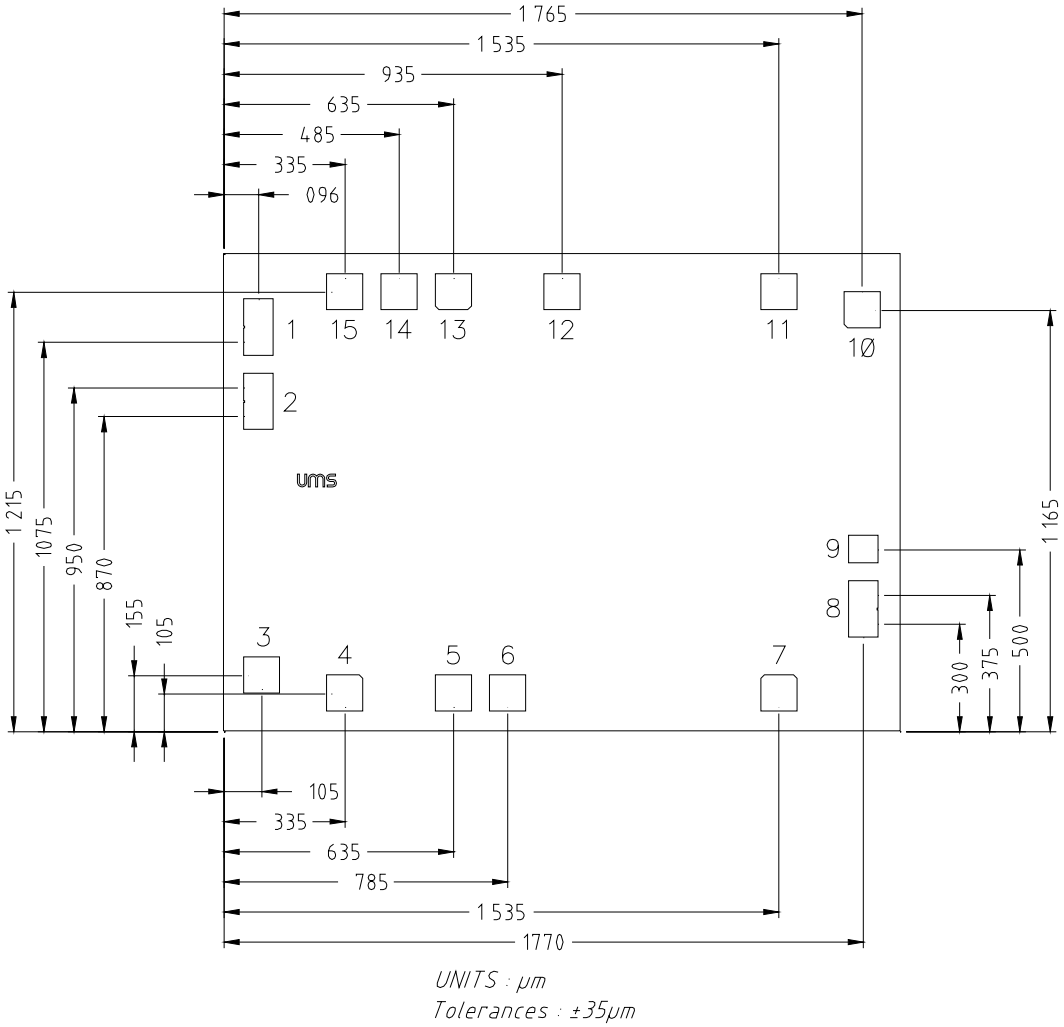
Chip Mechanical Data and Pin References



Chip thickness = 70 ± 10 µm
HF Pads (2,8) = 82 x 155 µm^2
DC Pads (3,4,6,7,11,12,14,15) = 100 x 100 µm^2

Pin number	Pin name	Description
1,9		Ground: should not be bonded. If required, please ask for more information.
5,13	**GND**	
2	**RF IN**	Input RF port
8	**RF OUT**	Output RF port
3,4,6,7	**VG**	Negative supply voltage
11,12,14,15	**VD**	Positive supply voltage
10	**DET**	Power detector output

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Ordering Information

Chip form : CHA5130-99F/00

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