

13.5-17 GHz Power Amplifier

GaAs Monolithic Microwave IC

Preliminary

Description

The CHA6042 is a compact four-stage PHEMT HPA MMIC designed for VSAT ground terminals and other radio applications. It provides typically 31dBm nominal output power at 1dB gain compression over the 13.5-17 GHz frequency range, and more than 30dB small signal gain.

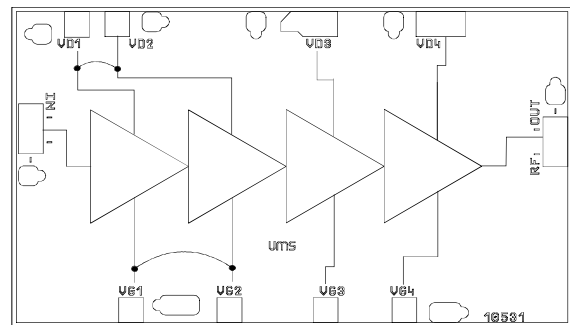
The circuit is manufactured with a 0.25µm gate length power PHEMT process on 70µm substrate, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form. The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

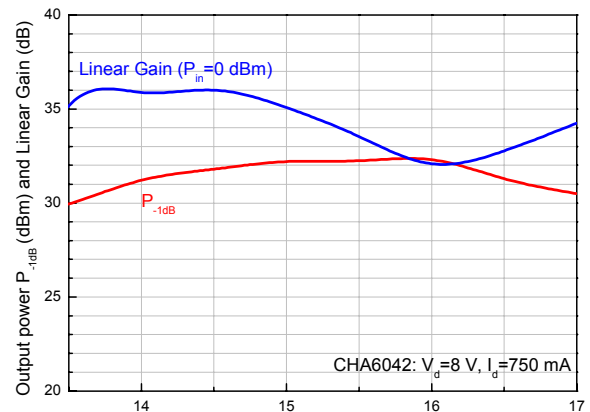
Main Features

- Broadband performances : 13.5-17GHz
- 32dB ± 2dB linear gain
- 31dBm output power at 1dB comp

- Chip size : 2.34 X 1.36 X 0.07mm³



Chip size 3.18mm²



Typical CHA6042 MMIC characteristic

Main Characteristics

Tamb = +25°C, Vd = 8V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	13.5		17	GHz
G	Small signal gain		32		dB
P1dB	CW output power at 1dB gain compression		31		dBm
Vd	Drain bias voltage		8		V
Id	Bias current		750		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical characteristics in JIG test fixture

Tamb = +25°C, Vd = 8V, Id=750 mA (typically Vg=-0.45V)

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	13.5		17	GHz
G	Small signal gain (1)		32		dB
ΔG	Small signal gain flatness		± 2		dB
P1dB	CW output power at 1dB gain compression (1)	30	31		dBm
Psat	Saturated output power (1)		32		dBm
RLin	Input return loss (1)		-15	-12	dB
RLout	Output return loss (1)		-12	-7	dB
Is	Reverse Isolation (1)		40		dB
Vd	Drain bias voltage (2)		8	9	V
Id	Bias current (2)		750	1000	mA
Vg	Gate bias voltage		-0.45		V

(1) These values are representative for CW measurements in JIG test fixture (losses uncorrected).

(2) Adjusting Vd from 8- to 9V or Id from 750- to 1000mA increases by approx. 0.5dB the P_{-1dB} over the bandwidth.

Absolute Maximum Ratings (2)

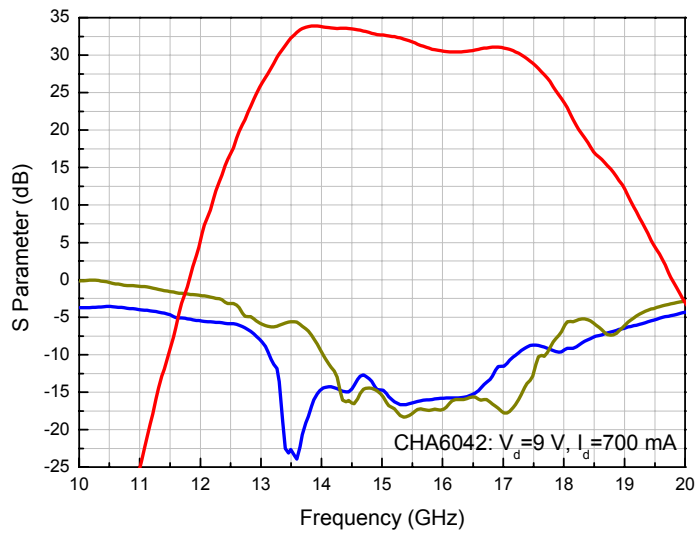
Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	9	V
Id	Maximum bias current	1.2	A
Vg	Min. and max. gate bias voltage	-2.5 ~ 0	V
Pin	Maximum peak input power overdrive (3)	+8	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

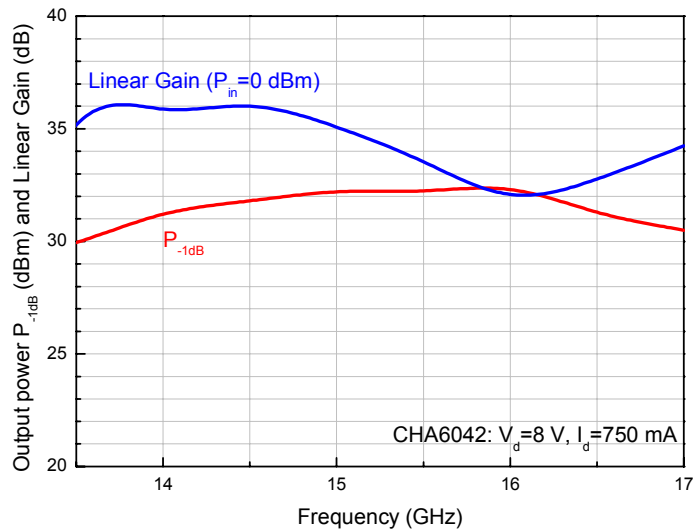
(2) Operation of this device above any one of these parameters may cause permanent damage.

(3) Duration < 1s.

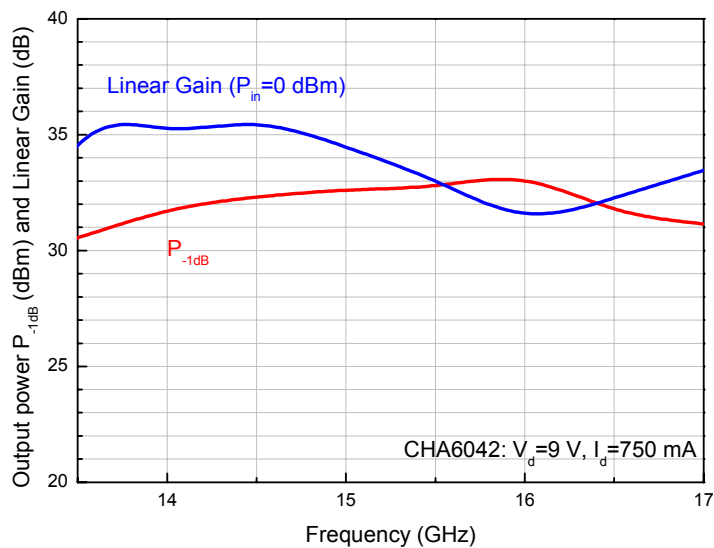
Typical CW performance @ Tamb=25°C



Typical JIG test-fixture S-parameters at $V_d=9\text{ V}$ and $I_d=700\text{ mA}$

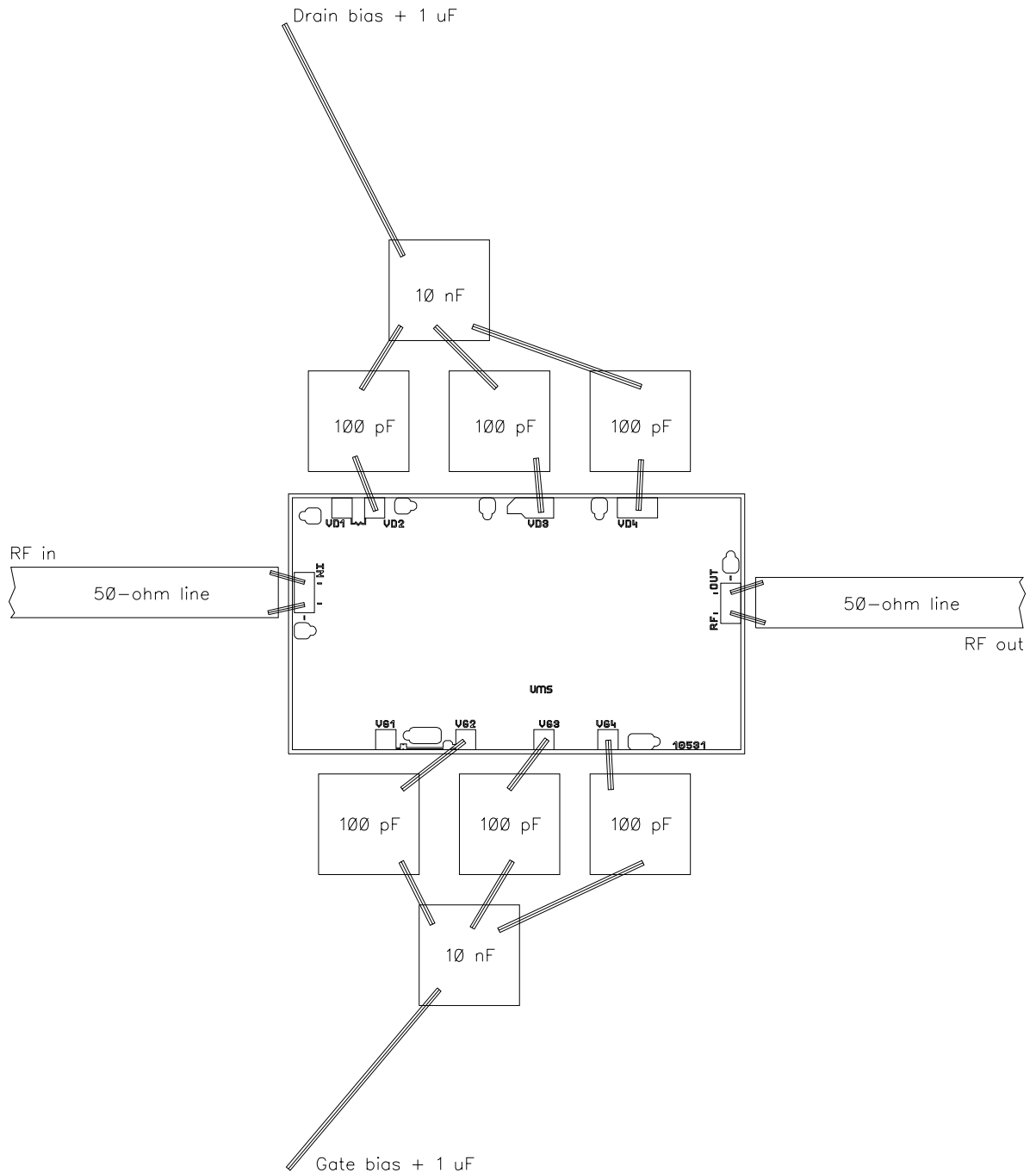


Typical CW output power at 1-dB gain compression (JIG test-fixture) at $V_d=8\text{ V}$ and $I_d=750\text{ mA}$



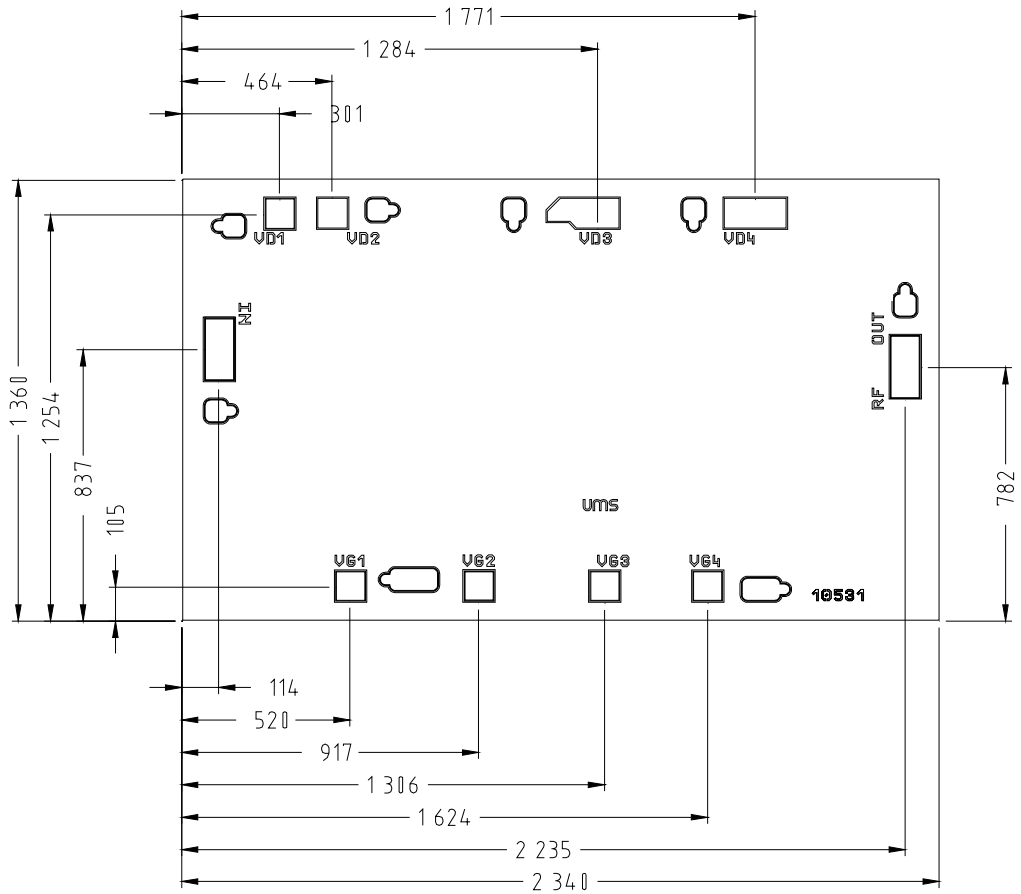
Typical CW output power at 1-dB gain compression (JIG test-fixture) at $V_d=9\text{ V}$ and $I_d=750\text{ mA}$

Chip Assembly and Mechanical Data



Remark: Wire bonding of VG1 is optional; VG1 and VG2 are connected on-chip, as well as VD1 and VD2.

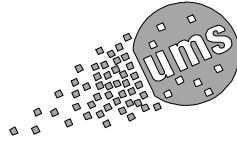
Bonding pad positions



Dimensions : (units µm)

2340±35 × 1360±35

Thickness 70



Ordering Information

Chip form : CHA6042-99F/00

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