

UTC L2949E LINEAR INTEGRATED CIRCUIT

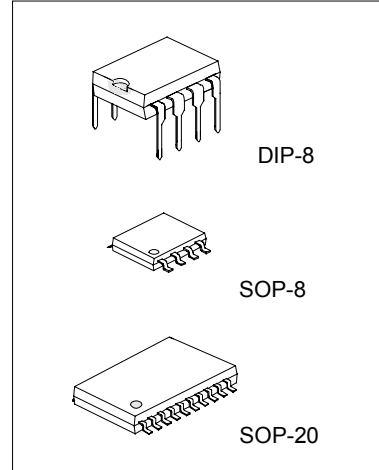
MULTIFUNCTION VERY LOW DROP VOLTAGE REGULATOR

DESCRIPTION

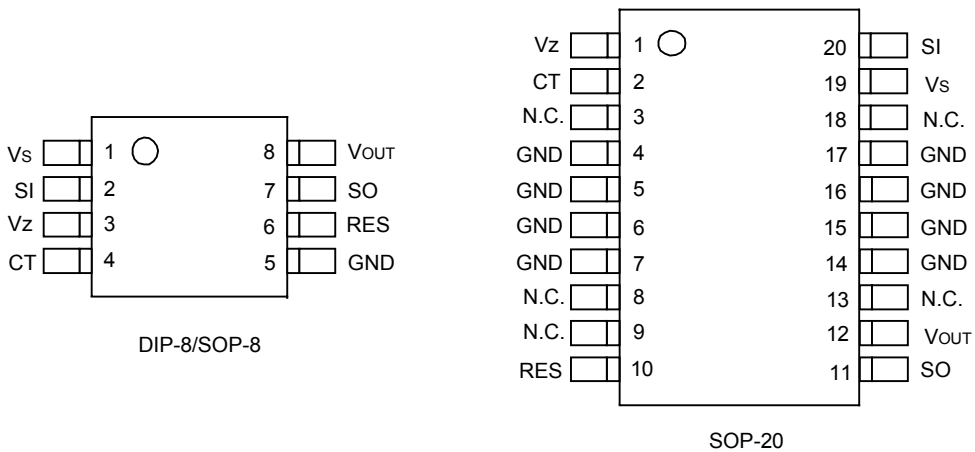
The UTC L2949E is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense. It is designed for supplying the microcomputer controlled systems especially in automotive applications.

FEATURES

- *Operating dc supply voltage range 5V to 28V.
- *Transient supply voltage up to 40V.
- *Extremely low quiescent current in standby mode.
- *High precision standby output voltage $5V \pm 1\%$
- *Output current capability up to 100mA.
- *Very low dropout voltage less than 0.5V.
- *Reset circuit sensing the output voltage
- *Programmable reset pulse delay with external capacitor
- *Voltage sense comparator.
- *Thermal shutdown and short circuit protections.

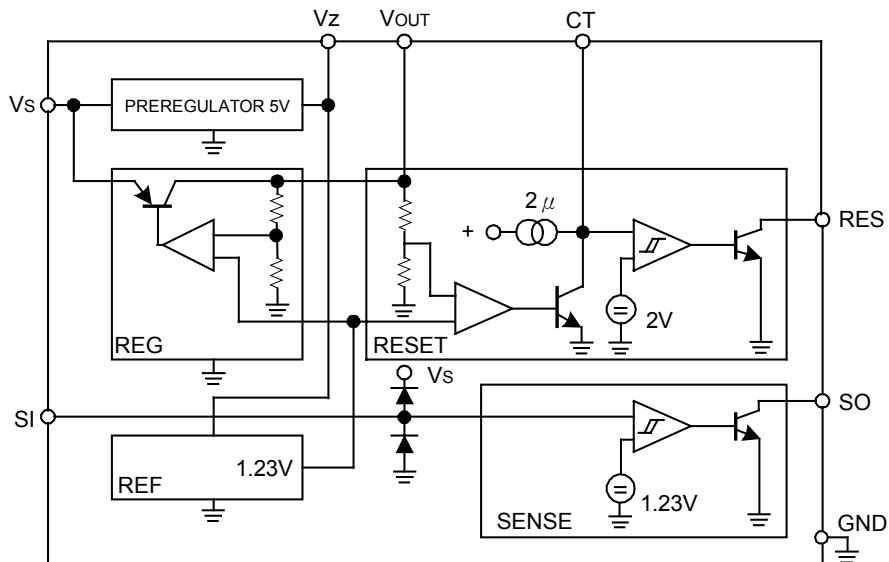


PIN CONNECTIONS



UTCL2949E LINEAR INTEGRATED CIRCUIT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|--------------------------------|--------------------|--------------------|------|
| DC Operating Supply Voltage | V _{CC} | 28 | V |
| Transient Supply Voltage(T<1s) | V _{CC TR} | 40 | V |
| Output Current | I _o | Internally Limited | |
| Output Voltage | V _o | 20 | V |
| Output Voltage Reset Output | V _{RES} | 20 | V |
| Sense Output | V _{so} | 20 | |
| Output Current Reset Output | I _{RES} | 5 | mA |
| Sense Output | I _{so} | 5 | |
| Preregulator Output Voltage | V _Z | 7 | V |
| Preregulator Output Current | I _Z | 5 | mA |
| Junction Temperature | T _J | -40~+150 | °C |
| Storage Temperature Range | T _{stg} | -55~+150 | °C |

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THERMAL DATA

| DESCRIPTION | SYMBOL | RATING | UNIT |
|---|------------|------------------|------|
| Thermal Resistance Junction-ambient DIP-8 SOP-8 SOP-20 | Rth j-amb | 100 200 50 | °C/W |
| Thermal Resistance Junction-pin (SOP-20) | Rth j-pins | 15 | °C/W |
| Thermal Shutdown Junction temperature | TJSD | 165 | °C |

ELECTRICAL CHARACTERISTICS (Vs=14V; -40°C<Tj<125°C unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP. | MAX | UNIT |
|--|----------------------|--|------------|-------------------|--------------------|------|
| Output Voltage | Vo | Tj=25°C; Io=1mA | 4.95 | 5 | 5.05 | V |
| Output Voltage | Vo | 6V<VIN<28V, 1mA<Io<50mA | 4.90 | 5 | 5.10 | V |
| Output Voltage | Vo | VIN=40V; T<1s 5mA<Io<100mA | 4.75 | | 5.25 | V |
| Dropout voltage | V _D | Io=10mA Io=50mA Io=100mA | | 0.1 0.2 0.3 | 0.25 0.4 0.5 | V |
| Input to Output Voltage Difference in Undervoltage Condition | V _{IO} | VIN=4V, Io=35mA | | | 0.4 | V |
| Max Output Leakage | I _{OUTH} ** | VIN=25V, Vo=5.5V | 20 | 50 | 80 | μA |
| Line Regulation | V _{OL} | 6V<VIN<28V, Io=1mA | | | 20 | mV |
| Load Regulation | V _{LO} | 1mA<Io<100mA | | | 30 | mV |
| Current Limit | I _{LIM} | Vo=4.5V Vo=4.5V, Tj=25°C Vo=0V(note 1) | 105 120 | 200 100 | 400 400 | mA |
| Quiescent Current | I _{QSE} | Io=0.3mA; Tj<100°C | | 200 | 300 | μA |
| Quiescent Current | I _Q | Io=100mA | | | 5 | mV |

** With this test we guarantee that with no output current the output voltage will not exceed 5.5V

RESET

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP. | MAX | UNIT |
|---------------------------------------|----------------------------|------------------------|-----|---------|-----|------|
| Reset Threshold Voltage | V _{RT} | | | Vo-0.5V | | V |
| Reset Threshold Hysteresis | V _{RTH} | | 50 | 100 | 200 | mV |
| Reset Pulse Delay | t _{RD} | CT=100nF; TR ≥ 100 μs | 55 | 100 | 180 | ms |
| Reset Output Low Voltage | V _{R_L} | RRES=10KΩ to Vs ≥ 1.5V | | | 0.4 | V |
| Reset Output High Leakage Current | I _{RH} | VRES=5V | | | 1 | μA |
| Delay Comparator Threshold | V _{CTH} | | | 2 | | V |
| Delay Comparator Threshold Hysteresis | V _{CTH,hy} | | | 100 | | mV |

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SENSE

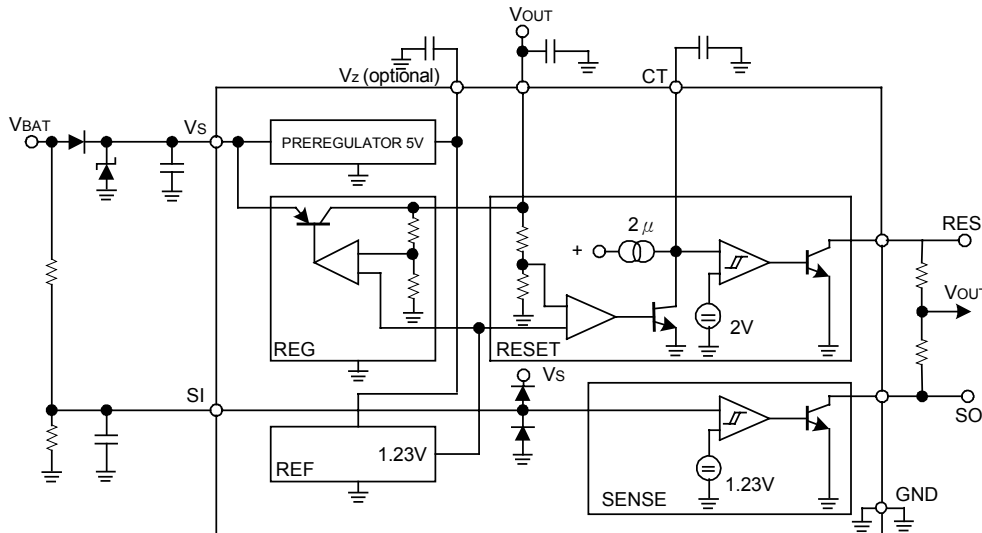
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP. | MAX | UNIT |
|----------------------------|-----------------|---|------|------|------|---------|
| Sense Low Threshold | Vst | | 1.16 | 1.23 | 1.35 | V |
| Sense Threshold Hysteresis | Vsth | | 20 | 100 | 200 | mV |
| Sense Output Low Voltage | VSL | $V_{SI} \leq 1.16V; V_S \geq 3V$ $R_{SO} = 10K \Omega \text{ to } V_O$ | | | 0.4 | V |
| Sense Output Leakage | I _{SH} | $V_{SO} = 5V; V_{SI} \geq 1.5V$ | | | 1 | μA |
| Sense Input Current | I _{SI} | $V_{SI} = 0$ | -20 | -8 | -3 | μA |

PREREGULATOR

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP. | MAX | UNIT |
|-----------------------------|--------|------------------|-----|------|-----|---------|
| Preregulator Output Voltage | Vz | $I_z = 10 \mu A$ | 4.5 | 5 | 6 | V |
| Preregulator Output Current | Iz | | | | 10 | μA |

Note 1: Foldback characteristic

APPLICATION CIRCUIT



For stability: $C_s \geq 1 \mu F$, $C_o \geq 4.7 \mu F$, $ESR < 10 \Omega$ at 10KHz

Recommended for application: $C_s = C_o = 10 \mu F$ to $100 \mu F$

APPLICATION INFORMATION

Suppl Voltage Transient

High supply voltage transients can cause a reset output signal disturbance.

For supply voltage greater than 8V the circuit shows a high immunity of the reset output against supply transients of the reset output against supply transients of more than $100V/\mu s$.

For supply voltages less than 8V supply transients of more than $0.4V/\mu s$ can cause a reset signal disturbance.

To improve the transient behaviour for supply voltages less than 8V a capacitor at pin 3 can be used.

A capacitor at pin 3 ($C_3 \geq 1 \mu F$) reduces also the output noise.

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FUNCTIONAL DESCRIPTION

The UTC L2949E is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

Voltage Regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element.

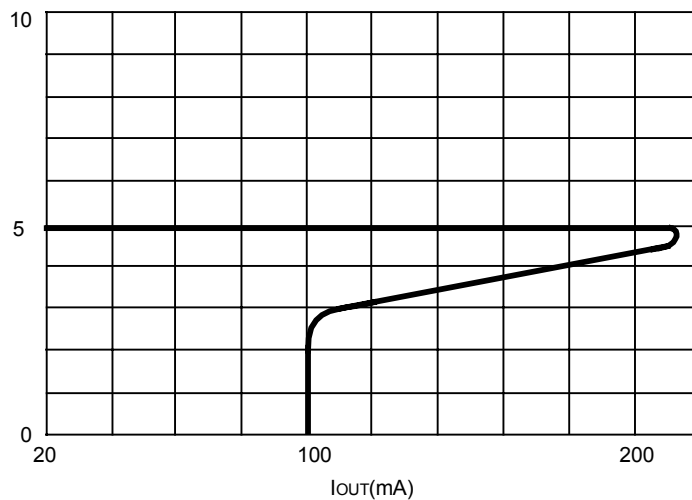


Figure 1: Foldback Characteristic of V_o

With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 4V. With this feature no functional interruption due to overvoltage pulses is generated. The typical curve showing the standby output voltage as a function of the input supply voltage is shown in Fig. 2. The current consumption of the device (quiescent current) is less than 300 μ A.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in Fig. 3.

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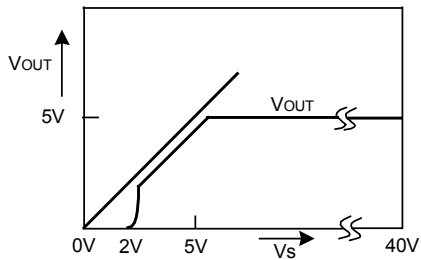


Figure 2: Output Voltage vs. Input voltage

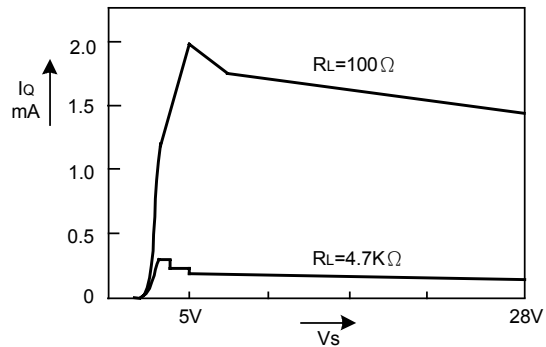


Figure 3: Quiescent Current vs. Supply Voltage

Preregulator

To improve the transient immunity a preregulator stabilized the internal supply voltage to 5V. This internal voltage is present at Pin3 (Vz). This voltage should not be used as an output because the output capability is very small ($\cong 10 \mu\text{A}$).

This output may be used as an option when a better transient behaviour for supply voltages less than 8V is required (see also application note).

In this case a capacitor (100nF - 1 μF) must be connected between Pin3 and GND. If this feature is not used Pin3 must be left open.

Reset Circuit

The block circuit diagram of the reset circuit is shown in Fig. 4. The reset circuit supervises the output voltage.

The reset threshold of 4.5V is defined with the internal reference voltage and standby output divider.

The reset pulse delay time TRD , is defined with the charge time of an external capacitor C_T :

$$\text{TRD} = \frac{C_T \cdot 2V}{2 \mu\text{A}}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional of the reset capacitor C_T and is proportional to the value of C_T .

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50 μs .

The typical reset output waveforms are shown in Fig. 5.

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator flexible in the application.

It can be used to supervise the input voltage either before or after the protection diode and to give additional information to the microprocessor like low voltage warnings.

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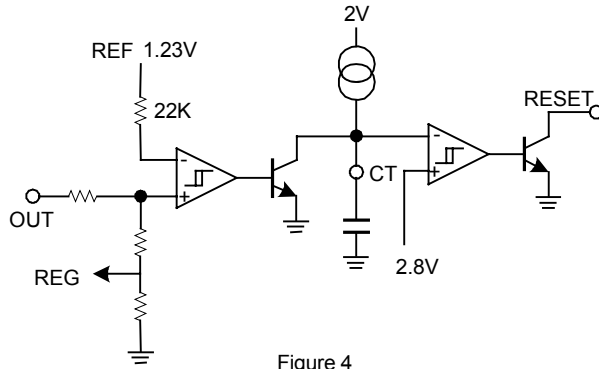


Figure 4

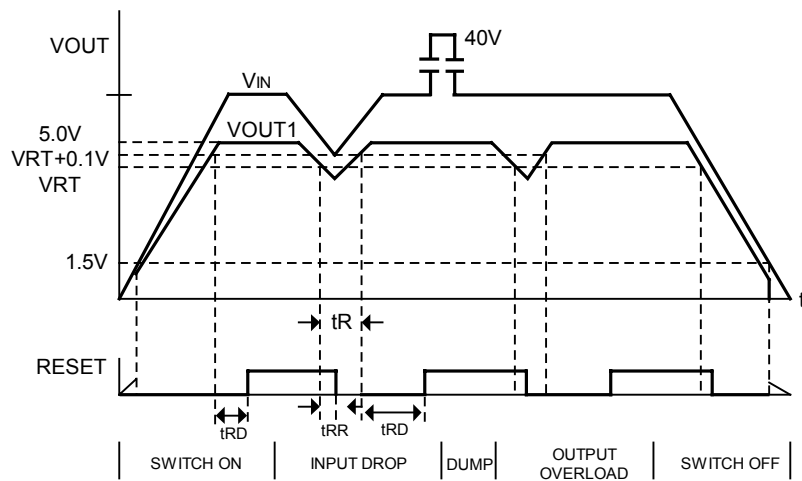


Figure 5

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