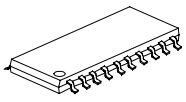
UTC TA31142 LINEAR INTEGRATED CIRCUIT

LOW POWER IF RECEIVER IC



TSSOP-20

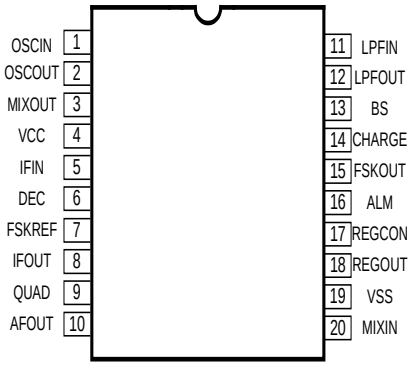
DESCRIPTION

The UTC TA31142 is a low power IF receiver IC and is suitable for use as the second IF downconverter in double-conversion paging systems. It is well-suited for POCSAG paging applications and incorporates a 2-level FSK demodulator consisting of a quadrature FM demodulator, on-chip bit-rate filter, and 1-bit comparator. An on-chip 1V regulator is provided for convenient biasing of off-chip circuitry.

FEATURES

*Extremely low power operation with power-down feature
*Built-in crystal oscillator for mixer local oscillator
*Mixer input frequency: 10-50 MHz
*Quadrature detector
*On-chip bit-rate filter
*Audio output
*1-bit comparator with open collector output
*1V regulator
*1.1V low battery alarm

PIN CONFIGURATIONS



NUMBER	SYMBOL	DESCRIPTION	NUMBER	SYMBOL	DESCRIPTION
1	OSCIN	Oscillator input (base)	11	LPFIN	LPF operational amplifier input
2	OSCOUT	Oscillator output (emitter)	12	LPFOUT	LPF operational amplifier output
3	MIXOUT	Mixer output (2KΩ output impedance)	13	BS	Two-state logic input to control receiver power up/down. (BS=high=normal operation; BS=low=stand-by mode)
4	VCC	Nominal 1.4V supply	14	CHARGE	Two-state logic input to control charge-discharge circuit. (CHARGE=high=fast charge; CHARGE=low=slow charge)
5	IFIN	IF amplifier input (2KΩ input impedance)	15	FSKOUT	Open collector NRZ comparator output (requires pull-up resistor)
6	DEC	IF amplifier de-coupling capacitor connection	16	ALM	Open collector low battery alarm output (requires pull-up resistor)
7	FSKREF	1-bit comparator reference input (requires external capacitor)	17	BEGCON	1.0V regulator control output for connection to external PNP base
8	IFOUT	IF amplifier output	18	REGOUT	1.0V regulator input for connection to external PNP collector
9	QUAD	Quadrature FM demodulator input	19	VSS	Ground
10	AFOUT	Quadrature FM demodulator output	20	MIXIN	Mixer input (5KΩ input impedance)

ABSOLUTE MAXIMUM RATINGS (Vss=0V)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	Vss-0.3 to Vss+3.5	V
Operating temperature range	T_{OPR}	-30 to 85	°C
Storage temperature range	T_{STG}	-55 to 150	°C
Soldering temperature range	T_{SLD}	255	°C
Soldering time range	t_{SLD}	10	s

RECOMMENDED OPERATING CONDITIONS (Vss=0V)

PARAMETER	SYMBOL	VALUE			UNIT
		Min.	Typ.	Max.	
Supply voltage range	Vcc	1.1	1.35	1.6	V
MIXIN input frequency	f_{MIXIN}			50	MHz
Operating temperature	T_A	-10	25	60	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C, Vcc=1.4V,Vss=0V, BS=high unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent current consumption	$I_{CC,total}$			1.1	1.6	mA
Standby current consumption	$I_{CC,modby}$	V_{BS}=0V			5	μA
Mixer conversion gain	Gc	Measured after 455 KHz ceramic filter	9	12.5	16	dB
Mixer output intermodulation intercept point	OIP3			-10		dBm
Mixer input resistance	$R_{in,MIX}$			5		kΩ
Mixer output resistance	$R_{out,MIX}$			2		kΩ
IF amplifier input resistance	$R_{in,IF}$			2		kΩ
S/N ratio I	SNI	-53 dBm at MIXIN		63		dB
S/N ratio 2	SN2	-53 dBm at IFIN		63		dB
S/N ratio 3	SN3	-91 dBm at IFIN		25		dB
Demodulation output level	VOD	-53 dBm at IF|N		45		mVrms
AM rejection ratio	AMR	-53 dBm at IFIN AM=30%		50		dB
FSK output duty ratio	DR		40	50	60	%
Low battery alarm threshold voltage	V_{ALM}		1.05	1.1	1.15	V
Regulator output voltage	V_{REGOUT}	430Ω load resistor	0.95	1.0	1.05	V
Charging / discharging current	I_{CH}	V_{FSKREF}=0V, V_{LPFOUT}=0.18V	35	70	110	μA
ALM logic HIGH output current	$I_{OH,ALM}$				2	μA
ALM logic LOW output voltage	$I_{OL,ALM}$				0.4	V
FSKOUT logic HIGH output current	$I_{OH.FSK.OUT}$				2	μA
FSKOUT logic LOW output vlotage	$V_{OL,PSK,OUT}$				0.4	V

FUNCTIONAL DESCRIPTION

The UTC TA31142 IF receiver IC incorporates a mixer, crystal-based local oscillator, IF amplifier, quadrature FM demodulator, bit-rate filter, and 1–bit comparator and is capable of demodulating 2-level FSK input signals. In addition, 1.0V regulator and 1.1V low battery alarm functions are provided.

POWER-DOWN FUNCTION

The entire receiver IC may be powered up and down through the control of the BS input (pin13). During power down operation, the quiescent current consumption of the IC drops to approximately 0μA. The high input impedance of the BS pin allows for direct interfacing with the CMOS output of an off-chip micro controller.

CHARGE / DISCHARGE CIRCUITRY

The function of the charge / discharge circuitry is for both fast and slow charging / discharging of the capacitor used for storing the voltage reference level of the FSKREF pin. The CHARGE input (pin14) should be enabled (CHARGE=high=fast charge) immediately after transition of the receiver IC from power-down to normal operation in order to reduce the charging / discharging time for coarse adjustment of the FSKREF voltage to the appropriate dc level (i.e. dc level of LPFOUT pin) and consequently to minimize the erroneous output of the 1-bit comparator. During actual data reception, the CHARGE pin should be set to low (CHARGE=low=slow charge) for fine adjustment of the FSKREF voltage.

1-bit COMPARATOR

The integrated 1-bit comparator operates as a data slicer and “squares up” the bit-rate filtered output from the quadrature demodulator. The decision threshold voltage level for the 1-bit comparator is stored on an external capacitor connected to the FSKREF pin.

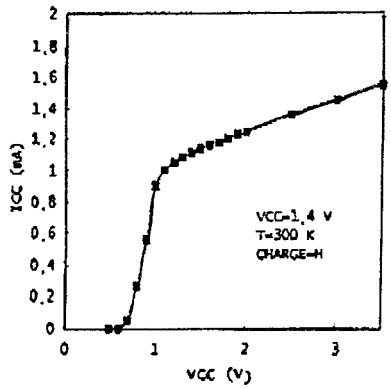
REGULATOR

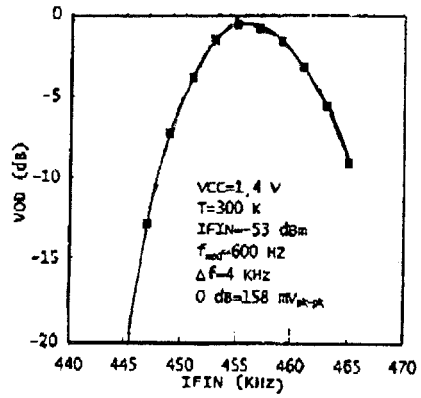
The on-chip 1.0V regulator requires a suitable off-chip PNP transistor to achievc regulation. The external PNP transistor should have an hFE>200 for V_{CE}>=0.1V.

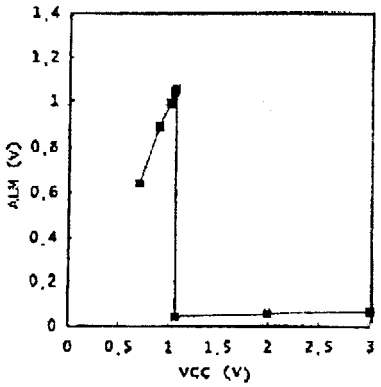
LOW BATTERY ALARM

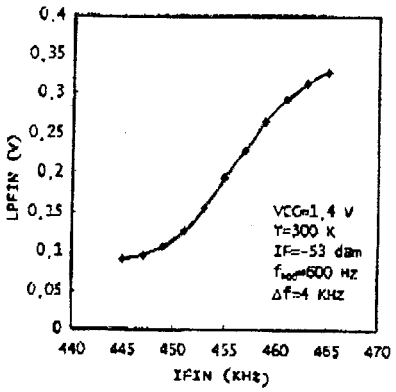
The low battery alarm output, ALM, is normally low, but rises to 1.1V (=VCC) when the VCC voltage falls below approximately 1.1V.

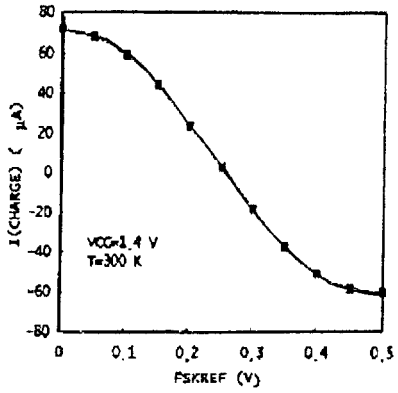
TYPICAL CHARACTERISTICS











TEST CIRCUIT