SRAM Memory Card 128 kB through512 kB

General Description

The WEDC **SEA** SRAM Series memory cards offer a high performance nonvolatile storage solution for code and data storage, disk caching, and write intensive mobile and embedded applications.

Packaged in PCMCIA type I housing the WEDC SRAM SEA series is based on 1 or 4Mbit SRAM memories, providing densities from 128 Kbytes to 512 Kbytes.

The SEA series of SRAM memory cards requires a 5V power supply and operates at speeds to 150ns. The cards are based on advanced CMOS technology providing very low power and reliable data retention characteristics. WEDC's SRAM cards contain a rechargeable lithium battery and recharge circuitry, eliminating the need for replaceable batteries found in many SRAM cards.

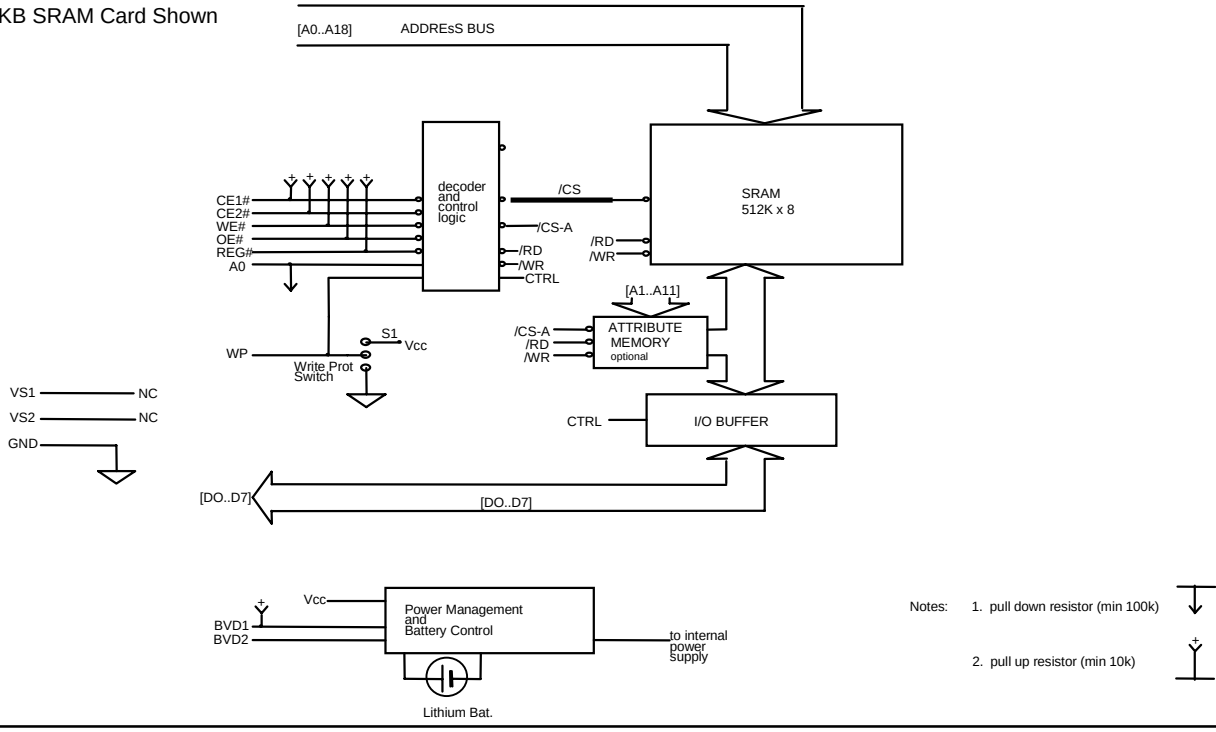
WEDC's standard cards are shipped with WEDC's SRAM Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

Features

- High Performance SRAM Memory Card
- Single 5 Volt Supply
- Fast Access Times: 150ns
- x8 Interface (subset of PCMCIA standard)
- Low Power CMOS technology provides very low power and reliable data retention characteristics
  - operating current 80mA maximum
  - standby current < 100µA typical
- Rechargeable Lithium battery with recharge circuitry
  - eliminates the need for replaceable batteries
  - standby current during recharge typically < 2mA
  - battery backup time
- 18 months - typical
  typical based on 512kB (lower densities will have greater storage times)
- Unlimited write cycles, no endurance issues
- 2KB EEPROM attribute memory containing CIS (optional)
- Optional Hardware Write Protect Switch
- PC Card Standard Type I Form Factor

Block Diagram

512KB SRAM Card Shown



Pinout

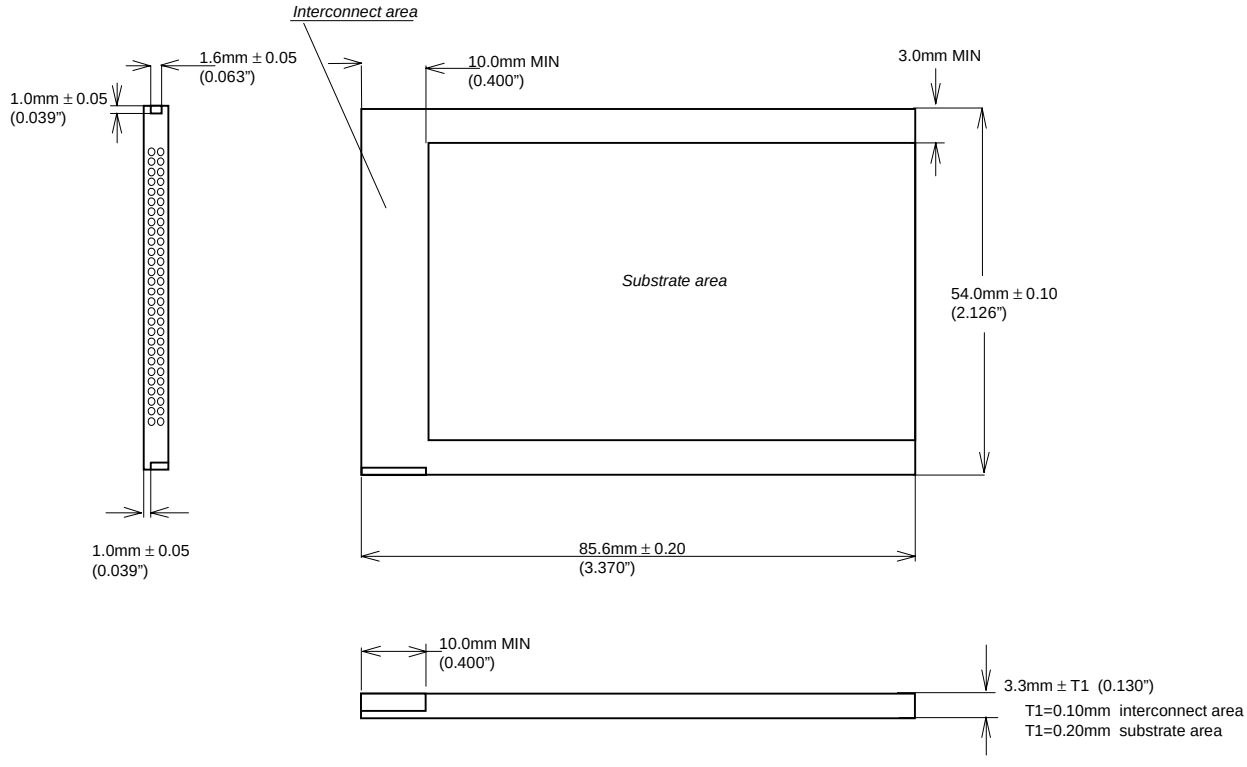
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	N.C.			
17	Vcc		Supply Voltage	
18	N.C.			
19	A16	I	Address bit 16	128KB(2)
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	NC	I/O	Data bit 11	
38	NC	I/O	Data bit 12	
39	NC	I/O	Data bit 13	
40	NC	I/O	Data bit 14	
41	NC	I	Data bit 15	
42	NC	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	N.C.			
45	N.C.			
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	512KB(2)
48	N.C.	I	Address bit 19	
49	N.C.	I	Address bit 20	
50	N.C.	I	Address bit 21	
51	Vcc		Supply Voltage	
52	N.C.			
53	N.C.		Address bit 22	
54	N.C.		Address bit 23	
55	N.C.		Address bit 24	
56	N.C.		Address bit 25	
57	VS2	O	Voltage Sense 2	N.C.
58	N.C.			
59	N.C.	O	Extended Bus Cycle	Low
60	N.C.			
61	REG#	I	Attrib Mem Select	Low
62	BVD2	O	Bat. Volt. Detect 2	
63	BVD1	O	Bat. Volt. Detect 1	(3)
64	NC	I/O	Data bit 8	
65	NC	I/O	Data bit 9	
66	NC	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:
1. CD1# and CD2# are grounded internal to PC Card.
2. Shows density for which specified address bit is MSB.
   Higher order address bits are no connects (ie 512KB A18 is MSB, A19 - A21 are NC).
3. BVD1 is an open drain output with a 10K ohm internal pull-up resistor.

Mechanical

Type I



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit. (address pins used are based on card density,see pinout for highest used address pin)
DQ0 – DQ7 DQ8 – DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 - DQ7 constitute the lower (even) byte and DQ8 - DQ15 the upper (odd) byte. Upper byte is Not Connected on this card.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# control signal in PCMCIA standard, to access high byte, - not used on this card
OE#	INPUT	**OUTPUT ENABLE:** Active low signal enabling read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Not used for SRAM cards
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** Follows hardware Write Protect Switch. When Switch is placed in on position, signal is pulled high (10K ohm). When switch is off signal is pulled low.
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Not used for SRAM cards.
VCC		**CARD POWER SUPPLY:** 5.0V for all internal circuitry.
GND		**GROUND:** for all internal circuitry.
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** only used with cards built with optional attribute memory.
RST	INPUT	**RESET:** Not used for SRAM cards
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** Provides status of Battery voltage. BVD2 = BVD1 = Voh (battery voltage is guaranteed to retain data) BVD2 = Vol, BVD1 = Voh (data is valid, battery recharge required) BVD2 = BVD1 = Vol (data may no longer be valid, battery requires extended recharge)
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

FUNCTIONAL TRUTH TABLE

READ function

					Common Memory			Attribute Memory		
Function Mode	/CE2	/CE1	/OE	/WE	/REG	D15-D8	D7-D0	/REG	D15-D8	D7-D0
Standby Mode	X	H	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	X	L	L	H	H	High-Z	Data Out	L	High-Z	Data Out

WRITE function

Standby Mode	X	H	X	X	X	X	X	X	X	X
Byte Access (8 bits)	X	L	H	L	H	X	Data In	L	X	Data In

Absolute Maximum Ratings (2)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V (1)
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Notes:
(1) During transitions, inputs may undershoot to -2.0V or overshoot to VCC +2.0V for periods less than 20ns.

(2) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics (1)

CMOS Test Conditions: VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Sym	Parameter	Density	Notes	Min	Typ(3)	Max	Units	Test Conditions
ICC	VCC Active Current	128KB	1		40	80	mA	VCC = 5.25V tcycle = 150ns
		512KB			40	80		
ICCS	VCC Standby Current	All	2,4	< 0.1	< 1	10	mA	VCC = 5.25V Control Signals = VCC
ILI	Input Leakage Current	All	5,6			±20	µA	VCC = VCCMAX Vin =VCC or VSS
ILO	Output Leakage Current	All	6			±20	µA	VCC = VCCMAX Vout =VCC or VSS
VIL	Input Low Voltage	All	6	0		0.8	V	
VIH	Input High Voltage	All	6	3.85		VCC +0.5	V	
VOL	Output Low Voltage	All	6			0.4	V	IOL = 3.2mA
VOH	Output High Voltage	All	6	VCC-0.4		VCC	V	IOH = -2.0mA

Notes:
1. All currents are for x8 mode and are RMS values unless otherwise specified.
2. Control Signals: CE_1#, CE_2#, OE#, WE#, REG#.
3. Typical: VCC = 5V, T = +25C.
4. ICCS includes battery recharge current. Value depends on battery discharge level. ICCS min is specified for fully charged battery. ICCS typical value is specified for battery discharge to 2.7V. ICCS max is specified for a fully discharged battery (0V). Battery will recharge to 1.5V in 20 sec.
5. Values are the same for byte and word wide modes for all card densities.
6. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors.

Battery Characteristics

Parameter	Density	Notes	Type I	Units	Conditions
Battery Life	All	(1)	10	years	Normal operation, T=25C
Battery Backup Time	128KB	(2)	24	months (typical)	T=25C Battery backup time is a calculated value and is not guaranteed. This should not be used to schedule battery recharging.
	512KB		18		

Notes:
1. Battery Life refers to functional lifetime of battery.
2. Battery backup time is density and temperature dependent.

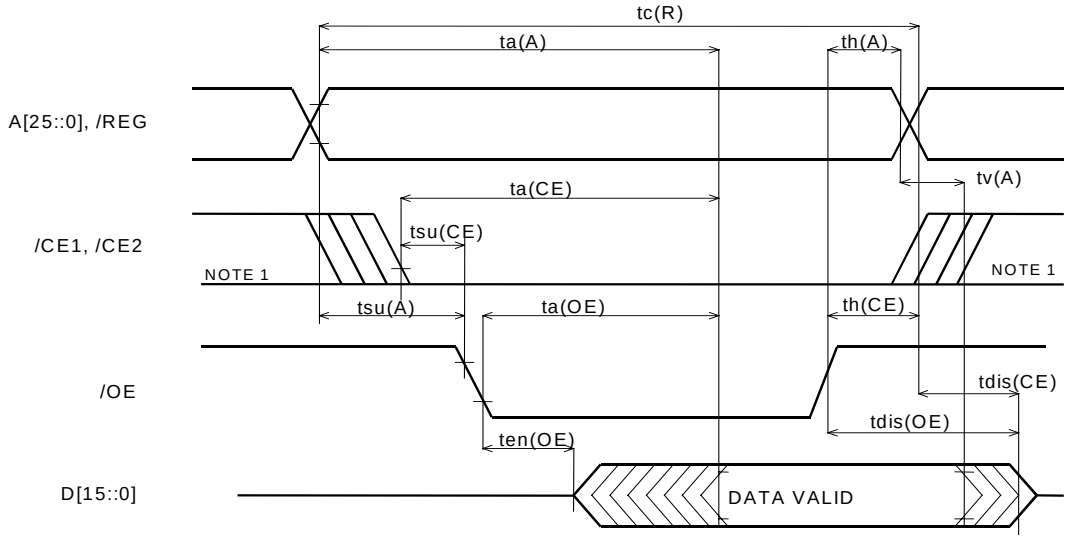
AC Characteristics

Read Timing Parameters

		150ns		
SYM (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_{RC}	Read Cycle Time	150		ns
$t_a(A)$	Address Access Time		150	ns
$t_a(CE)$	Card Enable Access Time		150	ns
$t_a(OE)$	Output Enable Access Time		75	ns
$t_{su}(A)$	Address Setup Time	20		ns
$t_{su}(CE)$	Card Enable Setup Time	0		ns
$t_h(A)$	Address Hold Time	20		ns
$t_h(CE)$	Card Enable Hold Time	20		ns
$t_v(A)$	Output Hold from Address Change	0		ns
$t_{dis}(CE)$	Output Disable Time from CE#		75	ns
$t_{dis}(OE)$	Output Disable Time from OE#		75	ns
$t_{dis}(CE)$	Output Enable Time from CE#	5		ns
$t_{dis}(CE)$	Output Enable Time from OE#	5		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



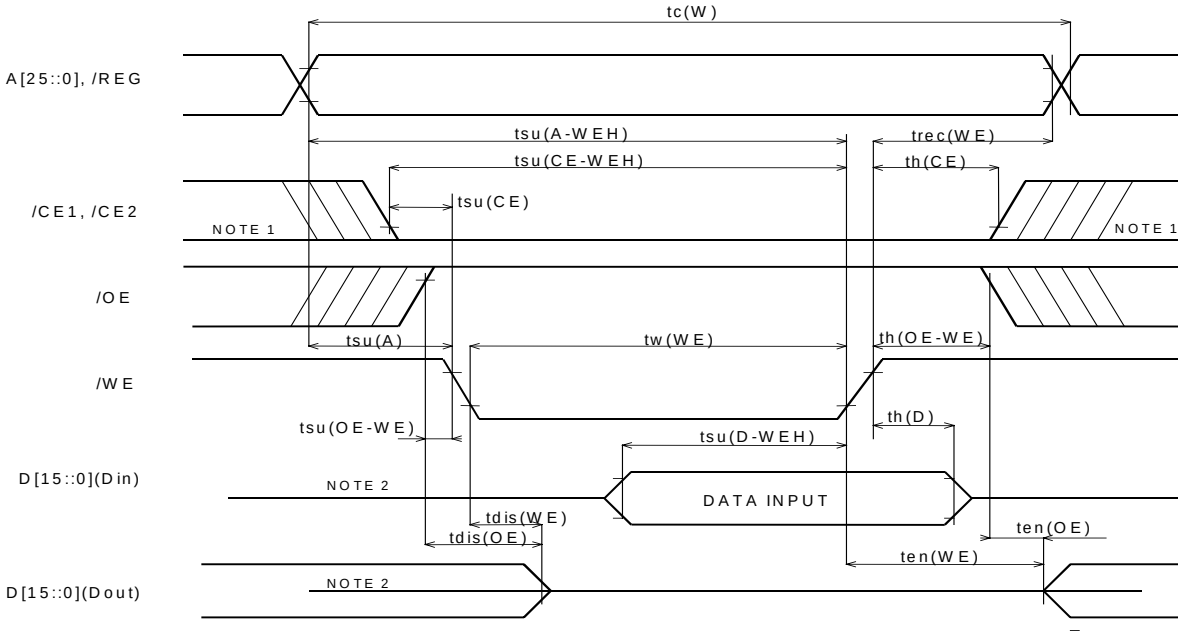
Note: Signal may be high or low in this area.

Write Timing Parameters

		150ns		
SYM (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_CW	Write Cycle Time	150		ns
t_w(WE)	Write Pulse Width	80		ns
t_{su}(A)	Address Setup Time	20		ns
t_{su}(A-WEH)	Address Setup Time for WE#	100		ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	100		ns
t_{su}(D-WEH)	Data Setup Time for WE#	50		ns
t_h(D)	Data Hold Time	20		ns
t_{rec}(WE)	Write Recover Time	20		ns
t_{dis}(WE)	Output Disable Time from WE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(WE)	Output Enable Time from WE#	5		ns
t_{dis}(OE)	Output Enable Time from OE#	5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		ns
t_h(OE-WE)	Output Enable Hold from WE#	10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		ns
t_h(CE)	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



Notes:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

PRODUCT MARKING

WED 8P512SEA0100C15 C995 9915

- **EDI** — Company Name
- **8P512SEA0100C15** — Part number
- **C995** — Lot code / trace number
- **9915** — Date code

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

8 P 512 SEA01 00 C 15

Card access time

15	150ns
25	250ns

Temperature range

C	Commercial	0°C to +70°C
I	Industrial	-40°C to +85°C

Packaging option

00	Standard, type 1

Card family and version

- See Card Family and Version Info. for details (next page)

Card capacity

512	512KB

PC card

P	Standard PCMCIA
R	Ruggedized PCMCIA

Card technology

7	FLASH
8	SRAM

Ordering Information

8P XXX SEA YY SS T ZZ

where

XXX:	**128**	**128KB**
	512	**512KB**
YY:	**01**	**no attribute memory, no Write Protect Switch**
	02	**with attribute memory, no Write Protect Switch**
	03	**with Write Protect Switch, no attribute memory**
	04	**with attribute memory, with Write Protect Switch**
SS:	**00**	**WEDC SRAM Logo Type I**
	01	**Blank Housing, Type I**
	02	**Blank Housing, Type I Recessed**
T:	**C**	**Commercial**
	I	**Industrial**
ZZ:	**15**	**150ns**

REVISION HISTORY

Date of revision	Version	Description
1-Jun-98	-001	Initial release
27-May-99	-002	Company/Logo change
1-Jun-00	-003	Added page 8, Page Header Change

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