36Mb, 512Kx72 Synchronous Pipeline Burst NBL SRAM *Preliminary**

FEATURES

- Fast clock speed: 225, 200, 166 and 150MHz
- Fast access times: 2.8, 3.0, 3.5 and 3.8ns
- Fast $\overline{OE}$ access times: 2.8, 3.0, 3.5 and 3.8ns
- Separate Core and I/O Power Supply
- Snooze Mode for reduced-standby power
- Individual Byte Write control
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - • 209-bump BGA package, JEDEC Pin Definition
- Low capacitive bus loading

DESCRIPTION

The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 72Mb SyncBurst SRAMs integrate two 512Kx36 SRAMs into a single BGA package to provide a 512Kx72 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The NBL or No Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ) and Output Enable (OE). Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

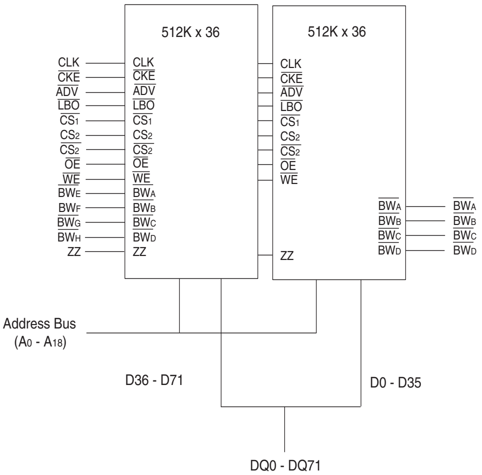
** This data sheet describes a product that may not be fully qualified or characterized and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	DQ_G	DQ_G	A	CS_2	A	ADV	A	$\overline{CS_2}$	A	DQ_B	DQ_B
B	DQ_G	DQ_G	$\overline{BW_C}$	$\overline{BW_G}$	NC	$\overline{WE}$	A	$\overline{BW_B}$	$\overline{BW_F}$	DQ_B	DQ_B
C	DQ_G	DQ_G	$\overline{BW_H}$	$\overline{BW_D}$	NC	$\overline{CS_1}$	NC	$\overline{BW_E}$	$\overline{BW_A}$	DQ_B	DQ_B
D	DQ_G	DQ_G	V_{SS}	NC	NC	$\overline{OE}$	NC	NC	V_{SS}	DQ_B	DQ_B
E	DQP_G	DQP_C	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_F	DQP_B
F	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
G	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
H	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
J	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
K	NC	NC	CLK	NC	V_{SS}	$\overline{CKE}$	V_{SS}	NC	NC	NC	NC
L	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
M	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
N	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
P	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
R	DQP_D	DQP_H	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_A	DQP_E
T	DQ_D	DQ_D	V_{SS}	NC	NC	$\overline{LBO}$	NC	NC	V_{SS}	DQ_E	DQ_E
U	DQ_D	DQ_D	NC	A	NC	A	A	A	NC	DQ_E	DQ_E
V	DQ_D	DQ_D	A	A	A	A_1	A	A	A	DQ_E	DQ_E
W	DQ_D	DQ_D	RFU	RFU	A	A_0	A	RFU	RFU	DQ_E	DQ_E

BLOCK DIAGRAM



FUNCTION DESCRIPTION

The W2Z512K72SJ is an NBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of $\overline{\text{OE}}$, $\overline{\text{LBO}}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable ($\overline{\text{CKE}}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{\text{CKE}}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE and ADV are driven low at the rising edge of the clock.

Output Enable ($\overline{\text{OE}}$) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE is driven low, the write enable input signals $\overline{\text{WE}}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation $\overline{\text{OE}}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{\text{WE}}$ is driven low at the rising edge of the clock. $\overline{\text{BW}}$[d:a] can be used for byte write operation. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, $\overline{\text{WE}}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{\text{LBO}}$ pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{\text{LBO}}$ = High)

		Case 1		Case 2		Case 3		Case 4	
$\overline{\text{LBO}}$ Pin	High	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{\text{LBO}}$ = Low)

		Case 1		Case 2		Case 3		Case 4	
$\overline{\text{LBO}}$ Pin	High	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE 1: LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{\text{CEx}}$	ADV	$\overline{\text{WE}}$	$\overline{\text{BWx}}$	$\overline{\text{OE}}$	$\overline{\text{CKE}}$	CLK	Address Accessed	Operation
H	L	X	X	X	L	↑	N/A	Deselect
X	H	X	X	X	L	↑	N/A	Continue Deselect
L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	H	X	X	H	L	↑	Next Address	Dummy Read
L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	H	↑	Current Address	Ignore Clock

NOTES:
1. *X means "Don't Care."*
2. *The rising edge of clock is symbolized by (↑)*
3. *A continue deselect cycle can only be entered if a deselect cycle is executed first.*
4. *$\overline{\text{WRITE}}$ = L means Write operation in WRITE TRUTH TABLE.*
   $\overline{\text{WRITE}}$ = H means Read operation in WRITE TRUTH TABLE.
5. *Operation finally depends on status of asynchronous input pins (ZZ and $\overline{\text{OE}}$).*
6. *$\overline{\text{CE}}$x refers to the combination of $\overline{\text{CE}}$1, CE2 and $\overline{\text{CE}}$2.*

WRITE TRUTH TABLE

$\overline{\text{WE}}$	$\overline{\text{BWa}}$	$\overline{\text{BWb}}$	$\overline{\text{BWc}}$	$\overline{\text{BWd}}$	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

NOTES:
1. *X means "Don't Care."*
2. *All inputs in this table must meet setup and hold time around the rising edge of CLK (↑).*

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS}	-0.3V to +3.6V
V_{IN} (DQx)	-0.3V to +3.6V
V_{IN} (Inputs)	-0.3V to +3.6V
Storage Temperature (BGA)	-55°C to +125°C
Short Circuit Output Current	100mA

**Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect reliability.*

ELECTRICAL CHARACTERISTICS

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}		1.7	V_{DD} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.7	V	1
Input Leakage Current	I_{LI}	$0V \leq V_{IN} \leq V_{DD}$	-5	5	µA	2
Output Leakage Current	I_{LO}	Output(s) Disabled, $0V \leq V_{IN} \leq V_{DD}$	-5	5	µA	
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.0	—	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA	—	0.4	V	1
Supply Voltage	V_{DD}		2.375	2.625	V	1

NOTES:
1. *All voltages referenced to V_{SS} (GND)*
2. *ZZ pin has an internal pull-up, and input leakage is higher.*

DC CHARACTERISTICS

Description	Symbol	Conditions	Typ	225 MHz	200 MHz	166 MHz	150 MHz	Units	Notes
Power Supply Current: Operating	I_{DD}	Device Selected; All Inputs $\leq V_{IL}$ or $\geq V_{IH}$; Cycle Time = t_{CYC} MIN; V_{DD} = MAX; Output Open		830	775	725	665	mA	1, 2
Power Supply Current: Standby	I_{SB2}	Device Deselected; V_{DD} = MAX; All Inputs $\leq V_{SS}$ + 0.2 or V_{DD} - 0.2; All Inputs Static; CLK Frequency = 0; ZZ $\leq V_{IL}$	30	60	60	60	60	mA	3
Power Supply Current: Current	I_{SB3}	Device Selected; All Inputs $\leq V_{IL}$ or $\geq V_{IH}$; Cycle Time = t_{CYC} MIN; V_{DD} = MAX; Output Open; ZZ $\geq V_{DD}$ - 0.2V	20	40	40	40	40	mA	2
Clock Running Standby Current	I_{SB4}	Device Deselected; V_{DD} = MAX; All Inputs $\leq V_{SS}$ + 0.2 or V_{DD} - 0.2; Cycle Time = t_{CYC} MIN; ZZ $\leq V_{IL}$		165	155	145	130	mA	2

NOTES:
1. *IDD is specified with no output current and increases with faster cycle times.*
2. *Typical values are measured at 2.5V, 25°C, and 10ns cycle time.*
3. *Typical values are measured at 2.5V, 25°C.*

BGA CAPACITANCE

Description	Symbol	Conditions	Typ	Max	Units	Notes
Control Input Capacitance	C_I	T_A = 25°C; f = 1MHz	5	7	pF	1
Input/Output Capacitance (DQ)	C_O	T_A = 25°C; f = 1MHz	6	8	pF	1
Address Capacitance	C_A	T_A = 25°C; f = 1MHz	5	7	pF	1
Clock Capacitance	C_{CK}	T_A = 25°C; f = 1MHz	3	5	pF	1

NOTES:
1. *This parameter is sampled.*

AC Characteristics

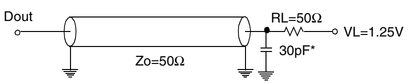
Parameter	Symbol	225MHz Min	225MHz Max	200MHz Min	200MHz Max	166MHz Min	166MHz Max	150MHz Min	150MHz Max	Units
Clock Time	t_{CYC}	4.4		5.0		6.0		6.7		ns
Clock Access Time	t_{CD}	—	2.8	—	3.0	—	3.5	—	3.8	ns
Output enable to Data Valid	t_{OE}	—	2.8	—	3.0	—	3.5	—	3.8	ns
Clock High to Output Low-Z	t_{LZC}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Output Hold from Clock High	t_{OH}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Output Enable Low to output Low-Z	t_{LZOE}	0.0	—	0.0	—	0.0	—	0.0	—	ns
Output Enable High to Output High-Z	t_{HZOE}	—	2.5	—	2.5	—	3.0	—	3.0	ns
Clock High to Output High-Z	t_{HZC}	—	2.5	—	2.5	—	3.0	—	3.0	ns
Clock High Pulse Width	t_{CH}	1.8	—	2.0	—	2.2	—	2.5	—	ns
Clock Low Pulse Width	t_{CL}	1.8	—	2.0	—	2.2	—	2.5	—	ns
Address Setup to Clock High	t_{AS}	1.5	—	1.5	—	1.5	—	1.5	—	ns
CKE Setup to Clock High	t_{CES}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Data Setup to Clock High	t_{DS}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Write Setup to Clock High	t_{WS}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Address Advance to Clock High	t_{ADVS}	1.5		1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t_{CSS}	1.5		1.5		1.5		1.5		ns
Address Hold to Clock high	t_{AH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
CKE Hold to Clock High	t_{CEH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Data Hold to Clock High	t_{DH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Write Hold to Clock High	t_{WH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Address Advance to Clock High	t_{ADVH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Chip Select Hold to Clock High	t_{CSH}	0.5	—	0.5	—	0.5	—	0.5	—	ns

NOTES:
1. *All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and $\overline{CE}$x is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.*
2. *Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.*
3. *A WRITE cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low.*
   A READ cycle is defined by $\overline{WE}$ High with ADV Low. Both cases must meet setup and hold times.

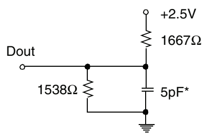
AC Test Conditions
(V_{DD} = 2.5V ± 5%, Unless Otherwise Specified)

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A)

Output Load (A)



Output Load (B)
(for t_{LZC}, t_{LZOE}, t_{HZOE}, and t_{HZC})



**Including Scope and Jig Capacitance*

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	ZZ ≥ VIH	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		2(t_{KC})	ns	1
ZZ inactive to input sampled		t_{RZZ}	2(t_{KC})		ns	1
ZZ active to snooze current		t_{ZZI}		2(t_{KC})	ns	1
ZZ inactive to exit snooze current		t_{RZZI}			ns	1

FIG. 2 SNOOZE MODE TIMING DIAGRAM

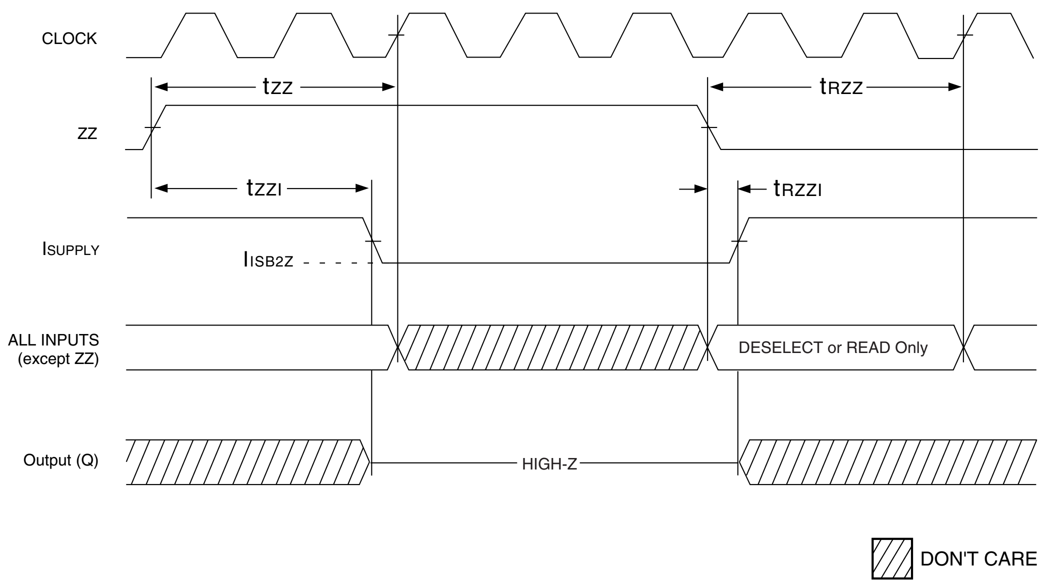
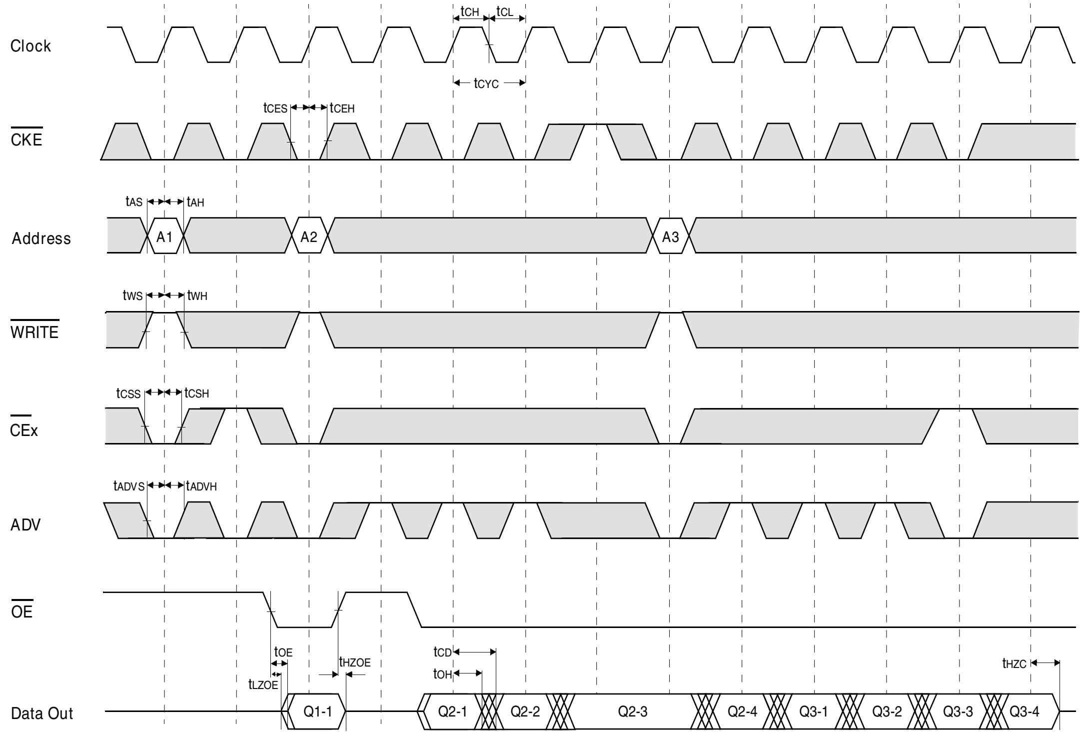
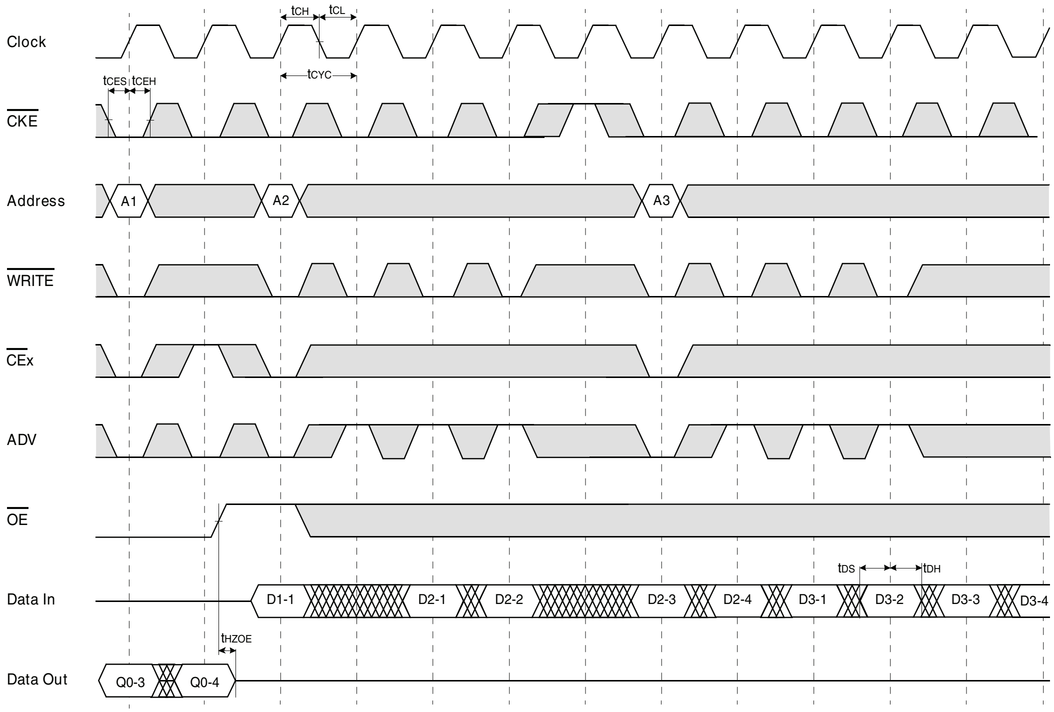


FIG. 3 TIMING WAVEFORM OF READ CYCLE



NOTES: $\overline{\text{WRITE}}$ = L means $\overline{\text{WE}}$ = L, and $\overline{\text{BWx}}$ = L
$\overline{\text{CEx}}$ refers to the combination of $\overline{\text{CE1}}$, CE2 and $\overline{\text{CE2}}$.

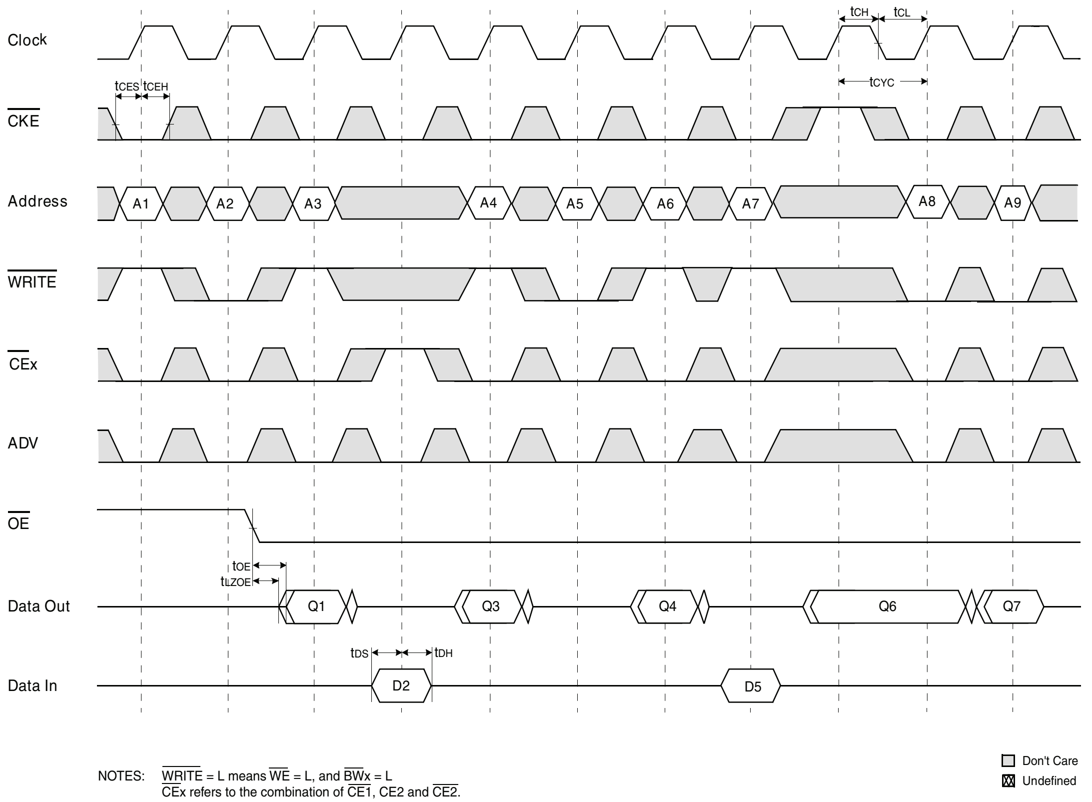
FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



NOTES: $\overline{\text{WRITE}}$ = L means $\overline{\text{WE}}$ = L, and $\overline{\text{BWx}}$ = L
$\overline{\text{CEx}}$ refers to the combination of $\overline{\text{CE1}}$, CE2 and $\overline{\text{CE2}}$.

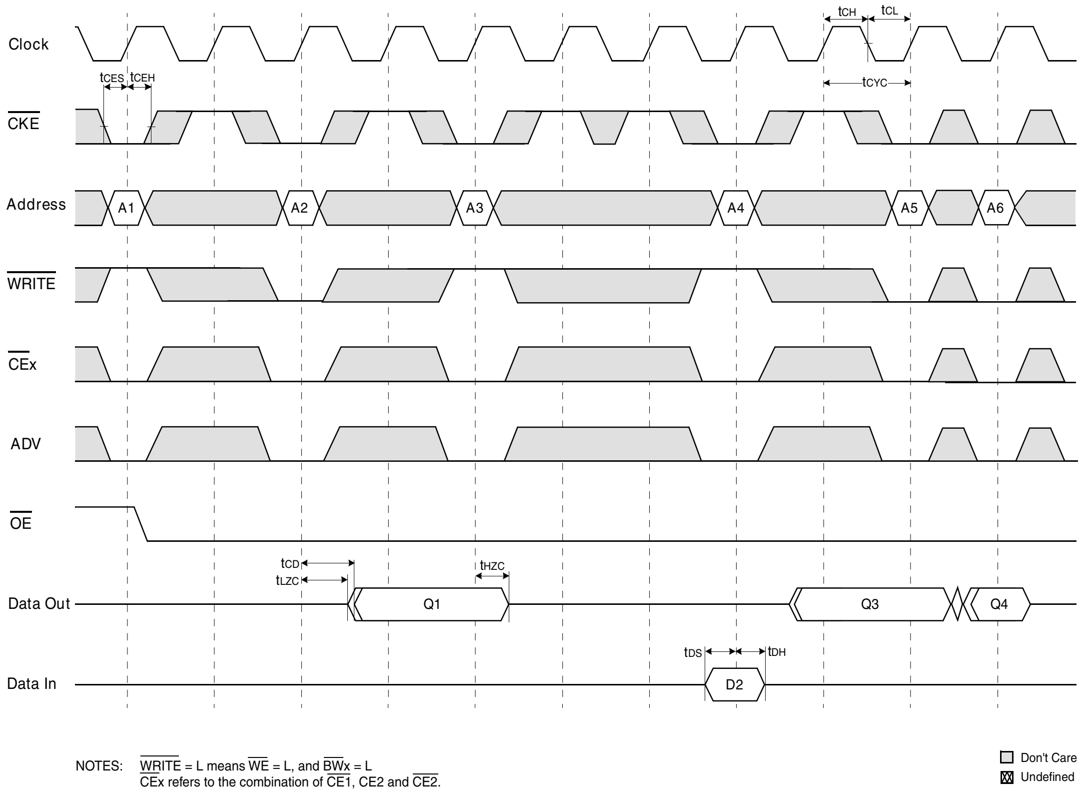
Don't Care
Undefined

FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE



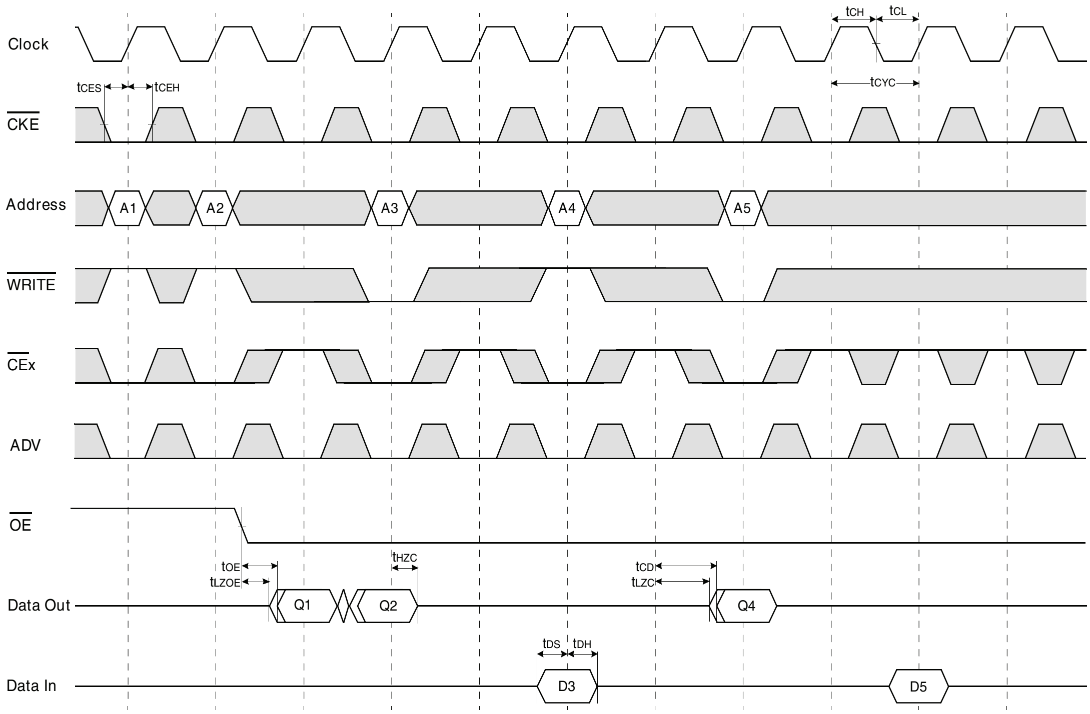
NOTES: WRITE = L means WE = L, and BWx = L
CEx refers to the combination of CE1, CE2 and CE2.

FIG. 6 TIMING WAVEFORM OF $\overline{CKE}$ OPERATION



NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CEx}$ refers to the combination of $\overline{CE1}$, CE2 and $\overline{CE2}$.

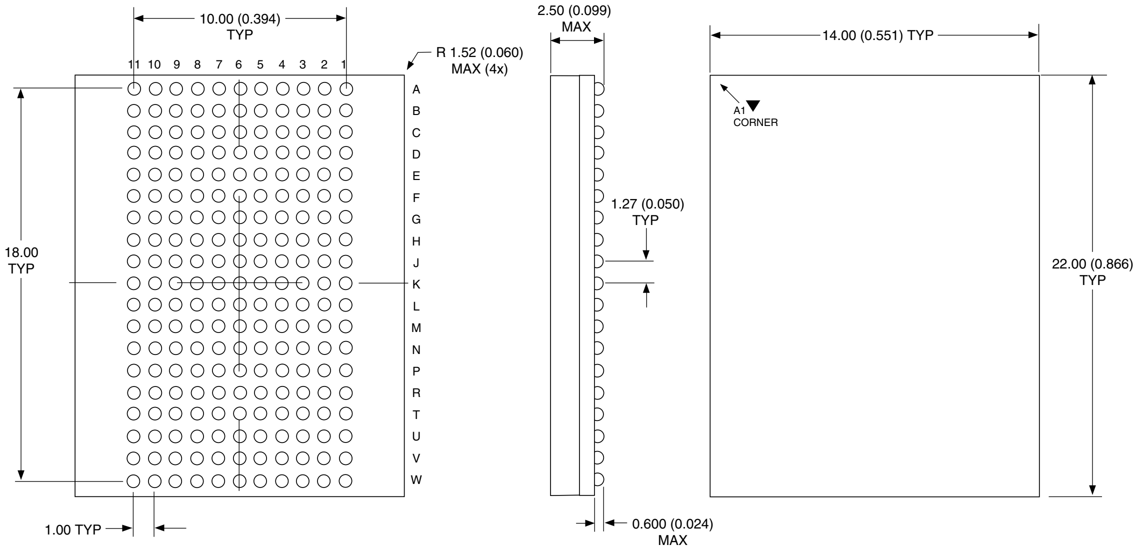
FIG. 7 TIMING WAVEFORM OF $\overline{CE}$ OPERATION



NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CEx}$ refers to the combination of $\overline{CE1}$, CE2 and $\overline{CE2}$.

Don't Care
Undefined

PACKAGE DIMENSION: 209 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: *Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.*

ORDERING INFORMATION

Commercial Temp Range (0°C to 70°C), Industrial Temp. Range (-40° to 85°C)

Part Number	Configuration	t_{CD} (ns)	Clock (MHz)	Operating Range
W2Z512K72SJ35ES	512K x 72	3.5	166	Engineering Samples
W2Z512K72SJ38ES	512K x 72	3.8	150	Engineering Samples
W2Z512K72SJ28BC	512K x 72	2.8	225	Commercial
W2Z512K72SJ30BC	512K x 72	3.0	200	Commercial
W2Z512K72SJ35BC	512K x 72	3.5	166	Commercial
W2Z512K72SJ38BC	512K x 72	3.8	150	Commercial
W2Z512K72SJ30BI	512K x 72	3.0	200	Industrial
W2Z512K72SJ35BI	512K x 72	3.5	166	Industrial
W2Z512K72SJ38BI	512K x 72	3.8	150	Industrial