

16MB (4x512Kx72) SYNC / SYNC BURST, DUAL KEY DIMM SRAM MODULE

FEATURES

- 4x512Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Module Enable (EM#)
- Clock Controlled Registered Bank Enables (E1#, E2#, E3#, E4#)
- Clock Controlled Byte Write Mode Enable (BWE#)
- Clock Controlled Byte Write Enables (BW1# - BW8#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Asynchronous Output Enable (G#)
- Internally Self-Timed Write
- Individual Bank Sleep Mode Enables (ZZ1, ZZ2, ZZ3, ZZ4)
- Gold Lead Finish
- 3.3V $\pm$ 10% Operation
- Frequency(s): 100, 83, 67, 50MHz
- Access Speed(s): t_{KH}QV = 7.5, 9, 10, 12, 15ns
- Common Data I/O
- High Capacitance (30pF) Drive, at Rated Access Speed
- Single Total Array Clock

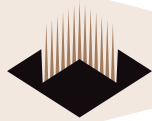
DESCRIPTION

The WED2CG472512V is a Synchronous/Synchronous Burst SRAM, 84 position Dual Key; Double High DIMM (168 contacts) Module, organized as 4x512Kx72. The Module contains sixteen (16) Synchronous Burst RAM devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The Module Architecture is defined as a Sync/SyncBurst, Flow-Through, with support for either linear or sequential burst. This Module provides high performance, 2-1-1-1 accesses when used in Burst Mode, and when used in Synchronous Only Mode, provides a high performance cost advantage over BiCMOS asynchronous device architectures.

Synchronous Only operations are performed via strapping ADSC# Low, and ADSP#/ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output Enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

**FIG. 1 PIN CONFIGURATION****PIN IDENTIFIER**

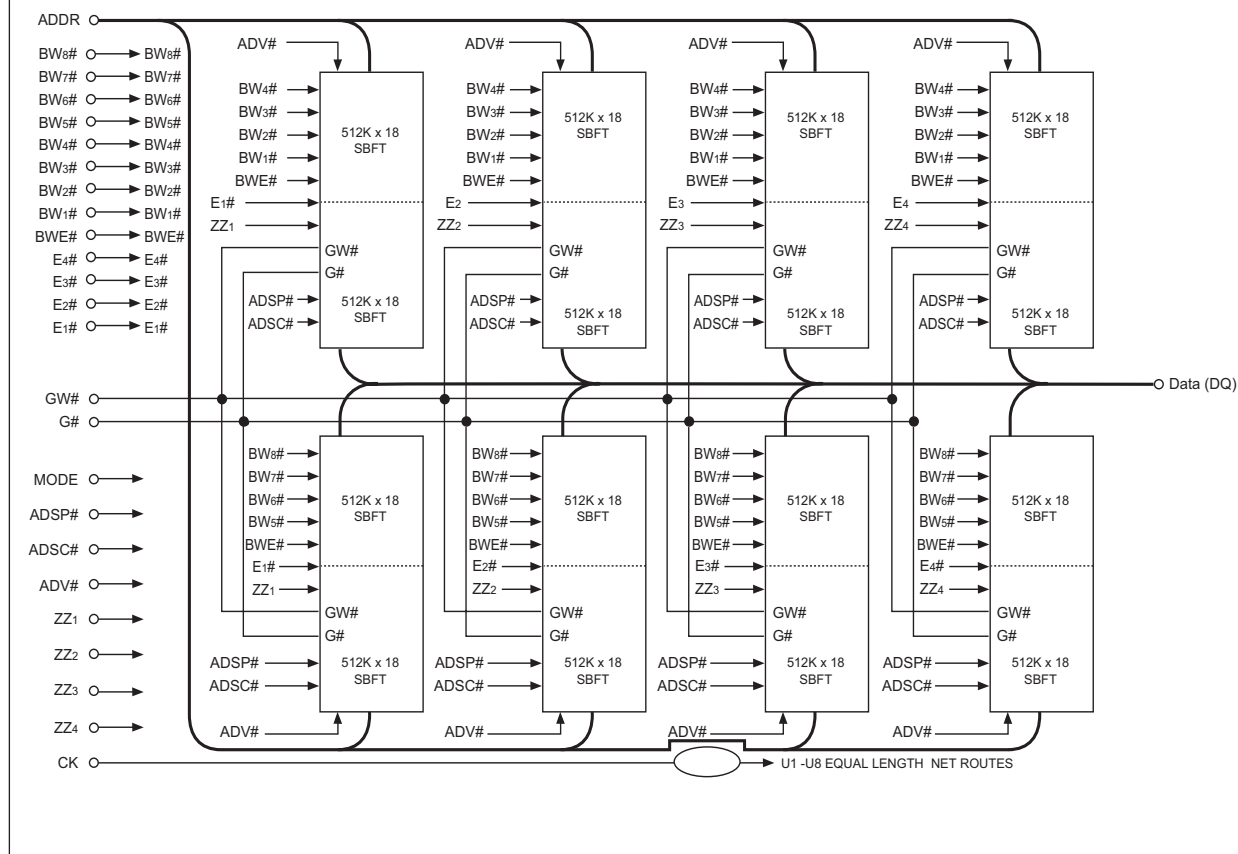
VSS	1	85	VSS	NC	43	127	DQP2
A0	2	86	A17	VCC	44	128	VCC
A16	3	87	A1	DQ16	45	129	DQ23
A2	4	88	A15	DQ17	46	130	DQ22
A14	5	89	A3	DQ18	47	131	DQ21
VCC	6	90	VCC	DQ19	48	132	DQ20
A4	7	91	A13	VSS	49	133	VSS
A12	8	92	A5	ZZ2	50	134	DQP3
A6	9	93	A11	VCC	51	135	VCC
A10	10	94	A7	DQ24	52	136	DQ31
VSS	11	95	VSS	DQ25	53	137	DQ30
A8	12	96	A9	DQ26	54	138	DQ29
RFU	13	97	A18	DQ27	55	139	DQ28
E4#	14	98	E1#	VSS	56	140	VSS
E2#	15	99	E3#	NC	57	141	DQP4
VSS	16	100	VSS	VCC	58	142	VCC
MODE	17	101	CK	DQ32	59	143	DQ39
EM#	18	102	VSS	DQ33	60	144	DQ38
GW#	19	103	G#	DQ34	61	145	DQ37
RFU	20	104	BWE#	DQ35	62	146	DQ36
VCC	21	105	VCC	VSS	63	147	VSS
BW4#	22	106	BW2#	ZZ3	64	148	DQP5
BW3#	23	107	BW1#	VCC	65	149	VCC
BW8#	24	108	BW6#	DQ40	66	150	DQ47
BW7#	25	109	BW5#	DQ41	67	151	DQ46
ADSC#	26	110	VSS	DQ42	68	152	DQ45
ADSP#	27	111	ADV#	DQ43	69	153	DQ44
VSS	28	112	VSS	VSS	70	154	VSS
NC	29	113	DQP0	NC	71	155	DQP6
VCC	30	114	VCC	VCC	72	156	VCC
DQ0	31	115	DQ7	DQ48	73	157	DQ55
DQ1	32	116	DQ6	DQ49	74	158	DQ54
DQ2	33	117	DQ5	DQ50	75	159	DQ53
DQ3	34	118	DQ4	DQ51	76	160	DQ52
VSS	35	119	VSS	VSS	77	161	VSS
ZZ1	36	120	DQP1	ZZ4	78	162	DQP7
VCC	37	121	VCC	VCC	79	163	VCC
DQ8	38	122	DQ15	DQ56	80	164	DQ63
DQ9	39	123	DQ14	DQ57	81	165	DQ62
DQ10	40	124	DQ13	DQ58	82	166	DQ61
DQ11	41	125	DQ12	DQ59	83	167	DQ60
VSS	42	126	VSS	VSS	84	168	VSS

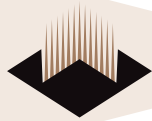
PIN DESCRIPTION

DQ0 - DQ63	Input/Output Bus
DQP0 - DQP7	Parity Bits
A0 - A18	Address Bus
EM#	Module Enable
E1#, E2#, E3#, E4#	Synchronous Bank Enables
BWE#	Byte Write Mode Enable
BW1# - BW8#	Byte Write Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
ZZ1, ZZ2, ZZ3, ZZ4	Bank Sleep Mode Enables
Vcc	3.3V Power Supply
Vss	Gnd



FUNCTIONAL BLOCK DIAGRAM





SYNC BURST – TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	*	*	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	*	*	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	L	X	L-H	D	Current

Note A: All truth Table Functions Repeat for Bank 3 (E3#) and Bank 4 (E4#).

SYNCHRONOUS ONLY – TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	GW#	G#	ZZ	CK	DQ
Synchronous Write - Bank 1	L	H	H	H	L	H	L	↑	High-Z
Synchronous Read - Bank 1	L	H	H	H	H	L	L	↑	
Synchronous Write - Bank 2	H	L	H	H	L	H	L	↑	High-Z
Synchronous Read - Bank 2	H	L	H	H	H	L	L	↑	
Synchronous Write - Bank 3	H	H	L	H	L	H	L	↑	High-Z
Synchronous Read - Bank 3	H	H	L	H	H	L	L	↑	
Synchronous Write - Bank 4	H	H	H	L	L	H	L	↑	High-Z
Synchronous Read - Bank 4	H	H	H	L	H	L	L	↑	
Snooze Mode	X	X	X	X	X	X	H	X	High-Z

**ABSOLUTE MAXIMUM RATINGS***

Voltage on V_{CC} Relative to V_{SS}	-0.3V to +4.6V
V_{IN}	-0.3V to $V_{CC} + 0.5V$
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	100mA

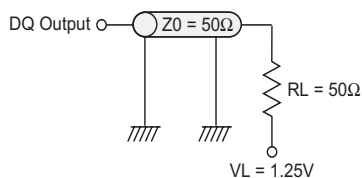
*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.3	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High	V_{IH}	2.0	3.0	$V_{CC} + 0.3$	V
Input Low	V_{IL}	-0.3	0	0.3	V
Input Leakage	I_{LI}	-2	1	2	mA
Output Leakage	I_{LO}	-2	1	2	mA

DC ELECTRICAL CHARACTERISTICS READ CYCLE

Description	Sym	Typ	Max				Units
			8.5	10	12	15	
Power Supply Current	I_{CC1}	2.0	2.9	2.7	2.7	2.5	A
Power Supply Current Device Selected, No Operation	I_{CC}	875	1.8	1.8	1.3	1.3	A
Snooze Mode	I_{CCZZ}	270	350	350	350	350	mA
CMOS Standby	I_{CC3}	500	700	700	700	700	mA
Clock Running-Deselect	I_{CCK}	900	1.1	1.1	1.0	1.0	A

AC TEST LOAD**OUTPUT TEST EQUIVALENCIES****AC TEST CONDITIONS**

Input Pulse Levels	V_{SS} to 3.0V
Input and Output Timing Ref.	1.25V
Output Test Equivalencies	See figure at left

**READ CYCLE TIMING PARAMETERS**

Description	Sym	9ns		10ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	f _{MAX}		100		83		67		50	MHz
Clock Cycle Time	t _{KHKH}	10		12		15		20		ns
Clock High Time	t _{KHKL}	4		5		5		6		ns
Clock Low Time	t _{KLKH}	4		5		5		6		ns
Clock to Output Valid	t _{KHQV}		9		10		12		15	ns
Clock to Output Invalid	t _{KHQX1}	3		3		3		3		ns
Clock to Output Low-Z	t _{KHQX}	4		4		4		4		ns
Output Enable to Output Valid	t _{GLQV}		4		5		5		5	ns
Output Enable to Output Low-Z	t _{GLQX}	0		0		0		0		ns
Output Enable to Output High-Z	t _{GHQZ}		4		5		5		5	ns
Address Setup	t _{AVKH}	2.5		2.5		2.5		2.5		ns
Bank Enable Setup	t _{EVKH}	2.5		2.5		2.5		2.5		ns
Address Hold	t _{KHAX}	1.0		1.0		1.0		1.0		ns
Bank Enable Hold	t _{KHEX}	1.0		1.0		1.0		1.0		ns

WRITE CYCLE TIMING PARAMETERS

Description	Sym	9ns		10ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	f _{MAX}		100		83		67		50	MHz
Clock Cycle Time	t _{KHKH}	12		12		15		20		ns
Clock High Time	t _{KHKL}	4		5		5		6		ns
Clock Low Time	t _{KLKH}	4		5		5		6		ns
Address Setup	t _{AVKH}	2.5		2.5		2.5		2.5		ns
Address Hold	t _{KHAX}	1.0		1.0		1.0		1.0		ns
Bank Enable Setup	t _{EVKH}	2.5		2.5		2.5		2.5		ns
Bank Enable Hold	t _{KHEX}	1.0		1.0		1.0		1.0		ns
Global Write Enable Setup	t _{WVKH}	2.5		2.5		2.5		2.5		ns
Global Write Enable Hold	t _{KHWX}	1.0		1.0		1.0		1.0		ns
Data Setup	t _{DVKH}	2.5		2.5		2.5		2.5		ns
Data Hold	t _{KHDX}	1.0		1.0		1.0		1.0		ns

FIG. 3

SYNCHRONOUS ONLY READ CYCLE

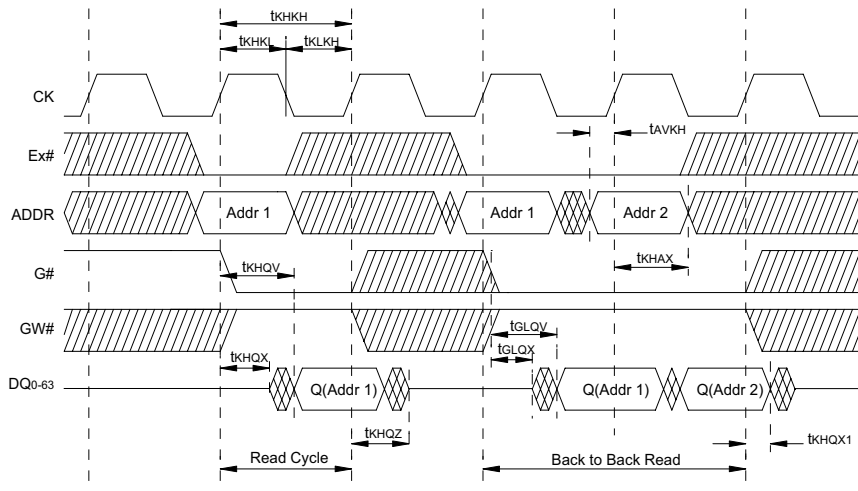


FIG. 4

SYNC-BURST READ CYCLE

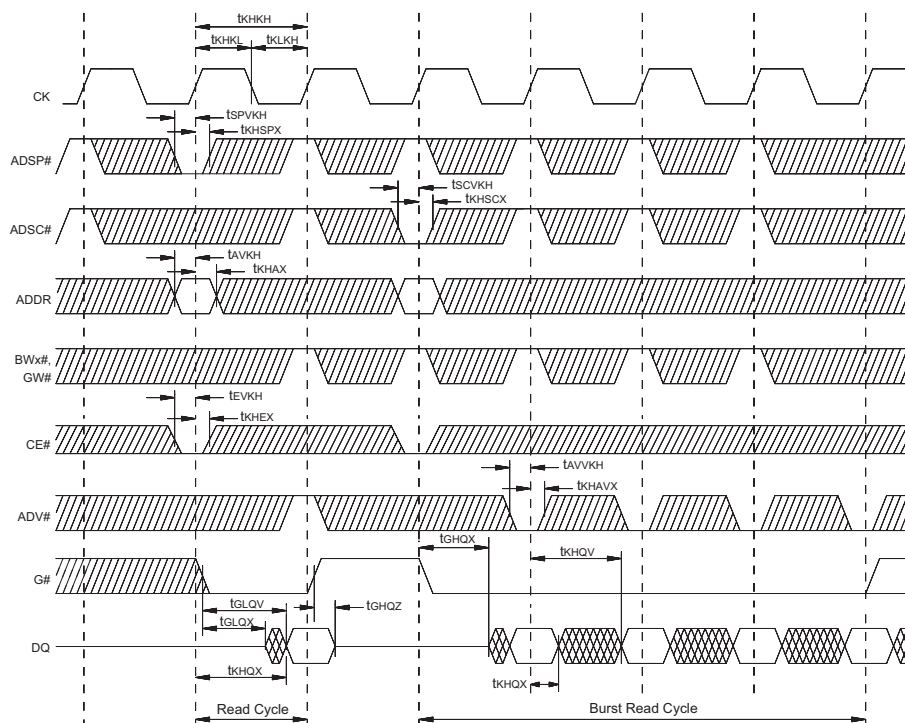




FIG. 5

SYNC (NON-BURST) WRITE CYCLE

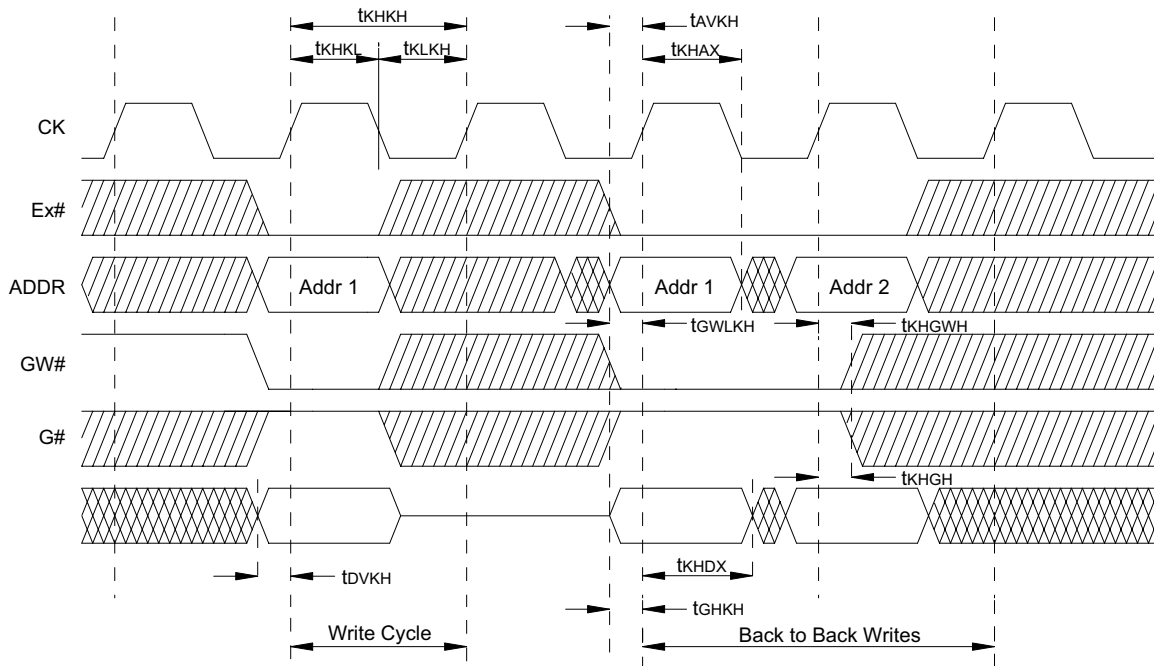
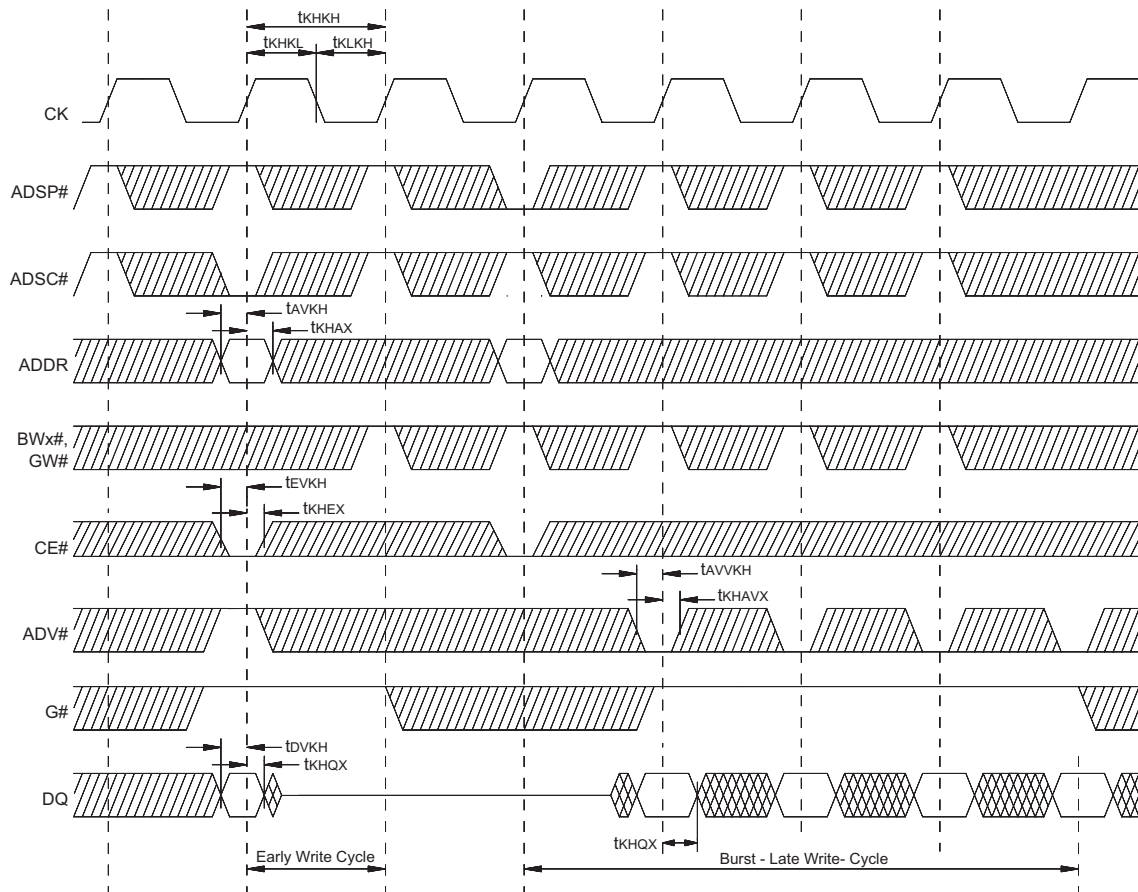




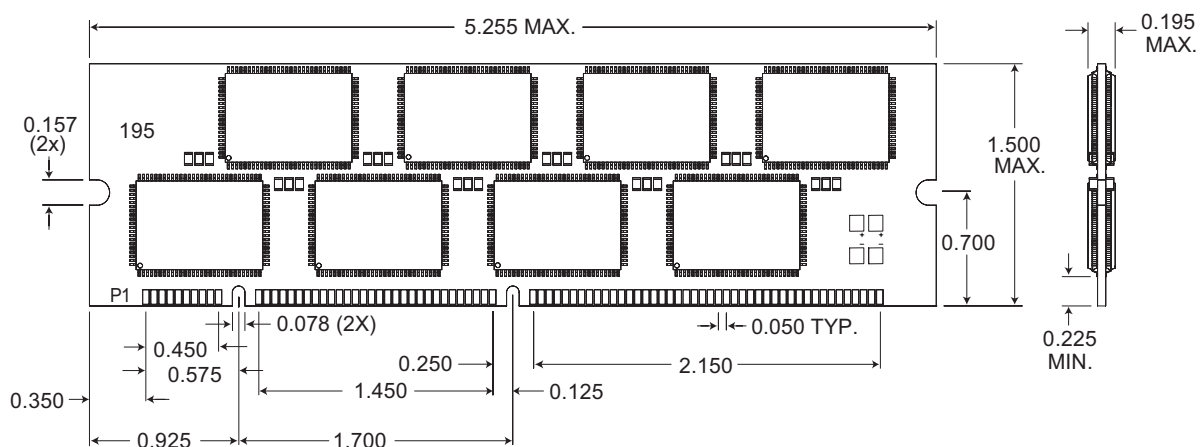
FIG. 6

SYNC-BURST WRITE CYCLE





PACKAGE DIMENSION: 168 GOLD LEAD DIMM



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Part Number	Configuration	Voltage (V)	Data	Package Access Time
WED2CG472512V9D2	4 x 512K x 72	3.3VDC	9ns	168 Gold Lead DIMM
WED2CG472512V10D2	4 x 512K x 72	3.3VDC	10ns	168 Gold Lead DIMM
WED2CG472512V12D2	4 x 512K x 72	3.3VDC	12ns	168 Gold Lead DIMM
WED2CG472512V15D2	4 x 512K x 72	3.3VDC	15ns	168 Gold Lead DIMM