



2Mx16 FLASH MODULE, SMD 5962-97610 PRELIMINARY*

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
 - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207).
 - Fits standard 56 SSOP footprint.
 - 44 pin Ceramic SOJ (Package 102)**
 - 44 lead Ceramic Flatpack (Package 208)**
- Sector Architecture
 - 32 equal size sectors of 64KBytes each
 - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx16; User Configurable as 2 x 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V $\pm$ 10% Supply.
- Low Power CMOS

- Data Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation.
- RESET pin resets internal state machine to the read mode.
- Ready/Busy (RY/BY) output for detection of program or erase cycle completion.
- Multiple Ground Pins for Low Noise Operation

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

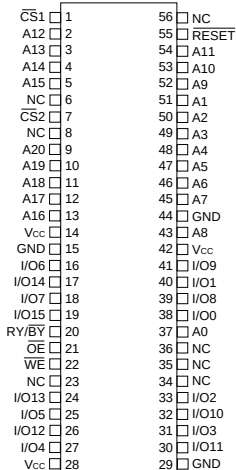
** Package to be developed.

Note: For programming information refer to Flash Programming 16M5 Application Notes.

FIG. 1 PIN CONFIGURATIONS

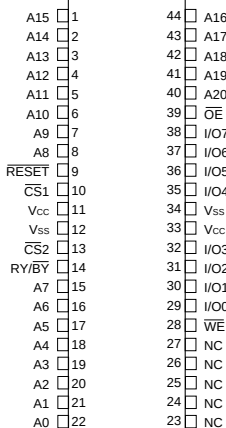
WF2M16-XDAX5 56 CSOP

TOP VIEW



WF2M16-XXX5 44 CSOJ (DL)** 44 FLATPACK (FL)**

TOP VIEW

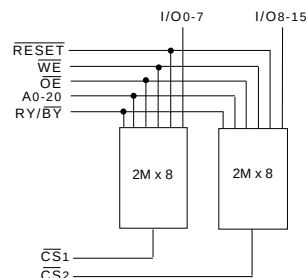


** Package to be developed.

PIN DESCRIPTION

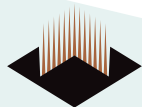
I/O0-15	Data Inputs/Outputs
A0-20	Address Inputs
WE	Write Enable
CS1-2	Chip Select
OE	Output Enable
Vcc	Power Supply
Vss	Ground
RY/BY	Ready/Busy
RESET	Reset

BLOCK DIAGRAM



NOTE:

1. RY/BY is an open drain output and should be pulled up to Vcc with an external resistor.
2. Address compatible with Intel 2M8 56 SSOP.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{stg}	-65 to +125	°C
Short Circuit Output Current	I _{OS}	100	mA
Data Retention (Mil Temp)		20	years
Endurance - write/erase cycles (Mil Temp)		100,000 min.	cycles

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	25	pF
$\overline{WE}$ capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	25	pF
$\overline{CS}$ capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	15	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	25	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T _A	-55	-	+125	°C
Operating Temperature (Ind.)	T _A	-40	-	+85	°C

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz		80	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH}		120	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, $\overline{CS}$ = V _{IH} , f = 5MHz, $\overline{RESET}$ = V _{CC} ± 0.3V		4.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85xV _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	90		120		150		ns
Chip Select Setup Time	tELWL	tCS	0		0		0		ns
Write Enable Pulse Width	tWLWH	tWP	45		50		50		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
Data Setup Time	tDVWH	tDS	45		50		50		ns
Data Hold Time	tWHDX	tDH	0		0		0		ns
Address Hold Time	tWLAX	tAH	45		50		50		ns
Write Enable Pulse Width High	tWHWL	tWPH	20		20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300		300	μs
Sector Erase (2)	tWHWH2			15		15		15	sec
Read Recovery Time before Write	tGHWL		0		0		0		μs
VCC Setup Time	tVCS		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		tOEHL	10		10		10		ns
RESET Pulse Width		tRP	500		500		500		ns

NOTES:

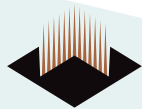
1. Typical value for tWHWH1 is 7μs.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	90		120		150		ns
Address Access Time	tAVQV	tACC		90		120		150	ns
Chip Select Access Time	tELQV	tCE		90		120		150	ns
Output Enable to Output Valid	tGLQV	tOE		40		50		55	ns
Chip Select High to Output High Z (1)	tEHQZ	tDF		20		30		35	ns
Output Enable High to Output High Z (1)	tGHQZ	tDF		20		30		35	ns
Output Hold from Addresses, CS or OE Change, whichever is First	tAXQX	tOH	0		0		0		ns
RESET Low to Read Mode (1)		tReady		20		20		20	μs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

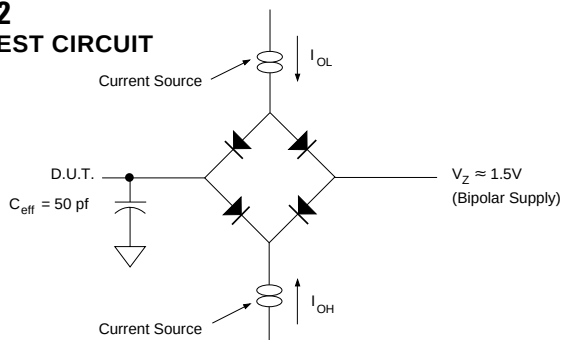
($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^\circ C$ to $+125^\circ C$)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	twc	90		120		150		ns
Write Enable Setup Time	twLEL	tws	0		0		0		ns
Chip Select Pulse Width	teLEH	tcp	45		50		50		ns
Address Setup Time	tAVEL	tAS	0		0		0		ns
Data Setup Time	tDVEH	tDS	45		50		50		ns
Data Hold Time	teHDX	tDH	0		0		0		ns
Address Hold Time	teLAX	tAH	45		50		50		ns
Chip Select Pulse Width High	teHEL	tcpH	20		20		20		ns
Duration of Byte Programming Operation (1)	twHWH1			300		300		300	μs
Sector Erase Time (2)	twHWH2			15		15		15	sec
Read Recovery Time	tgHEL		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		toEH	10		10		10		ns

NOTES:

1. Typical value for twHWH1 is 7 μs .
2. Typical value for twHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

FIG. 3
RESET TIMING DIAGRAM

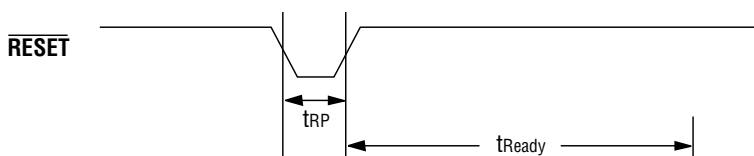




FIG. 3
AC WAVEFORMS FOR READ OPERATIONS

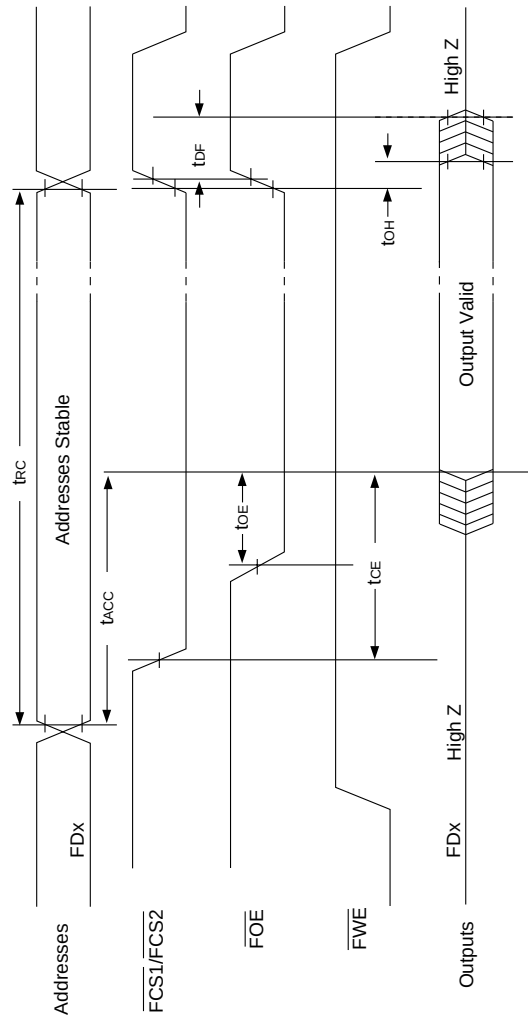
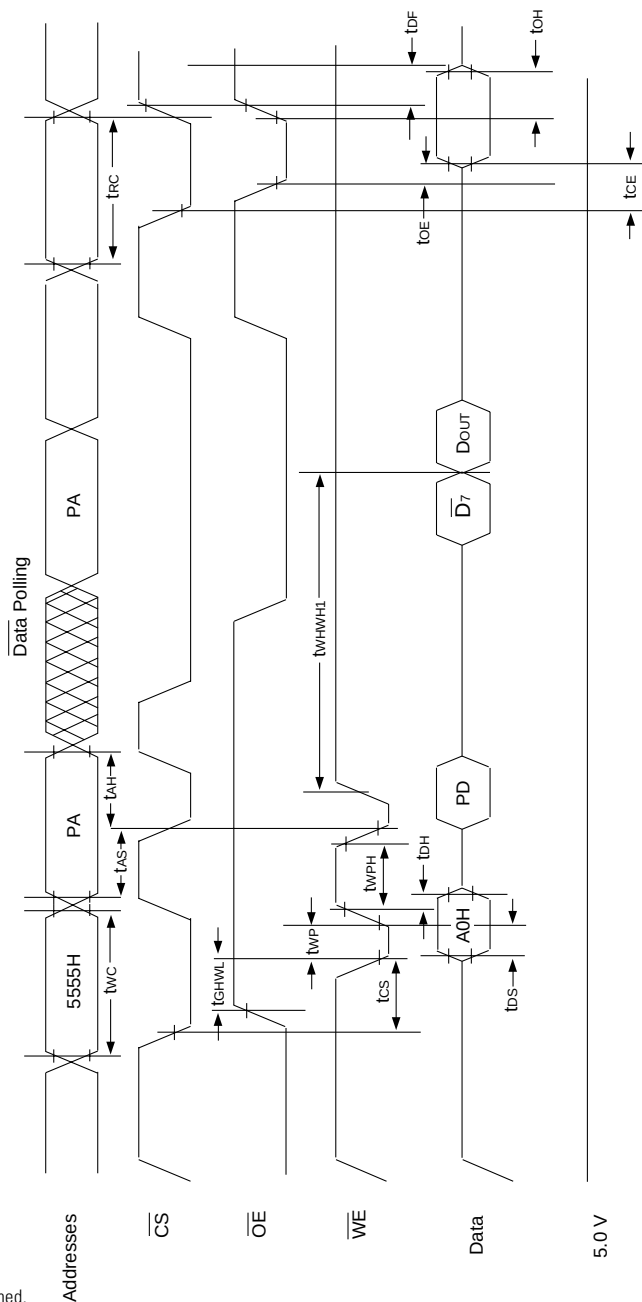




FIG. 4
WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED

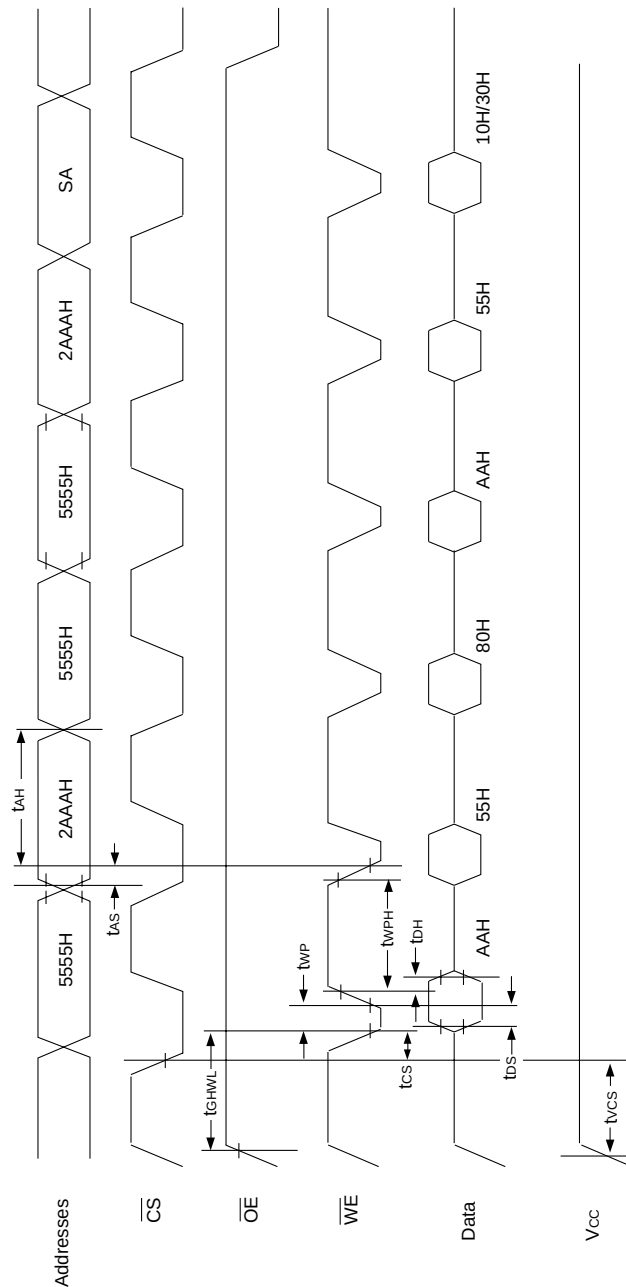


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. Dour is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 5
AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.



FIG. 6
AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS

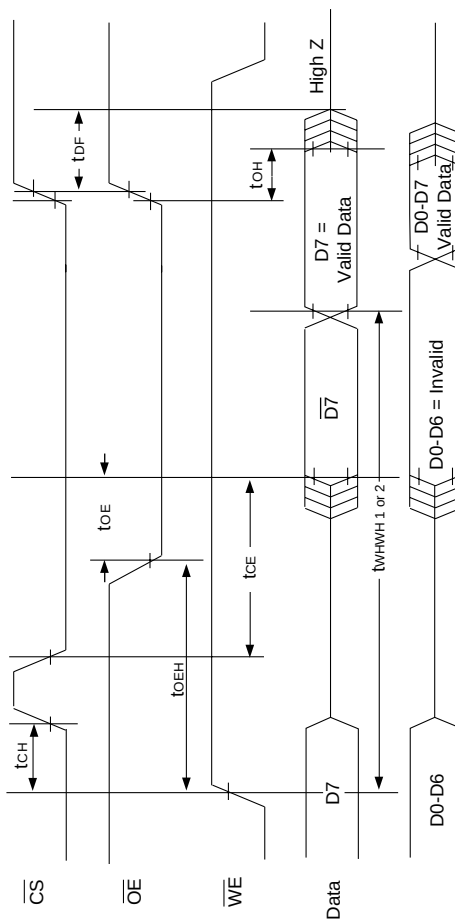
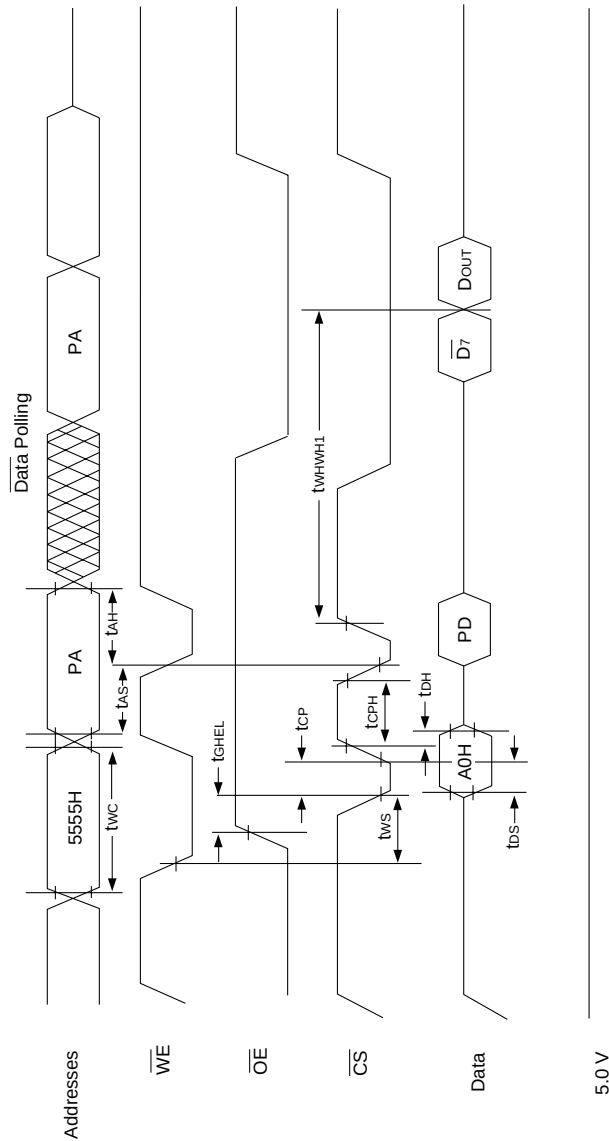




FIG. 7
ALTERNATE $\overline{CS}$ CONTROLLED
PROGRAMMING OPERATION TIMINGS

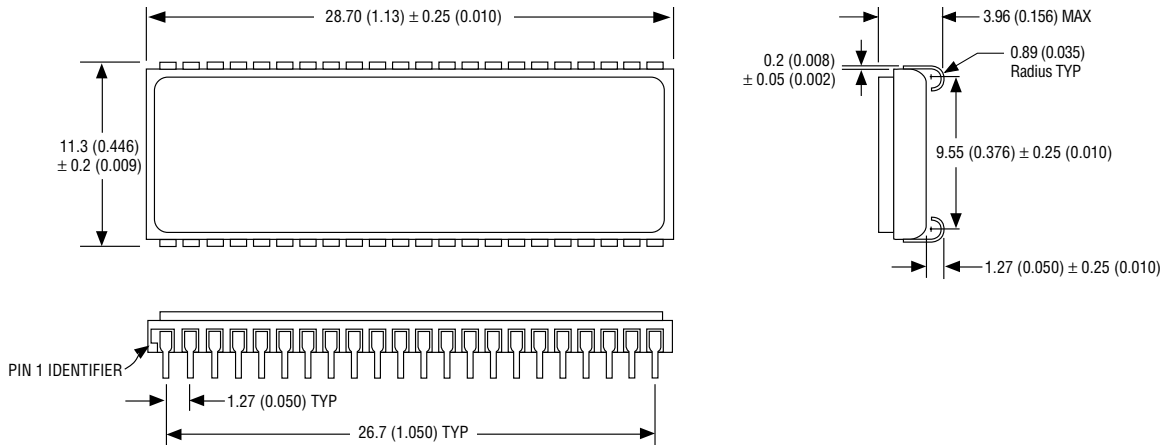


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. D_{out} is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



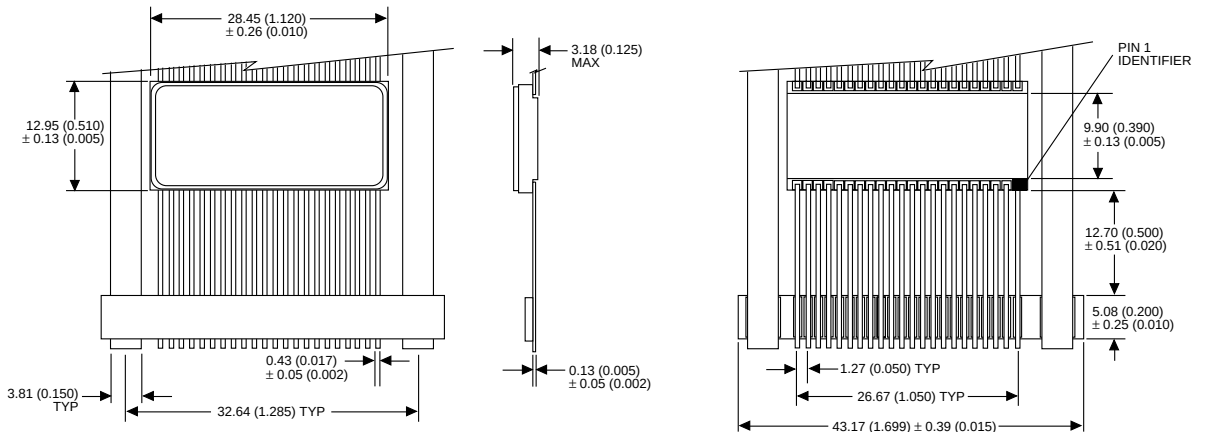
PACKAGE 102: 44 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.

PACKAGE 208: 44 LEAD, CERAMIC FLAT PACK**

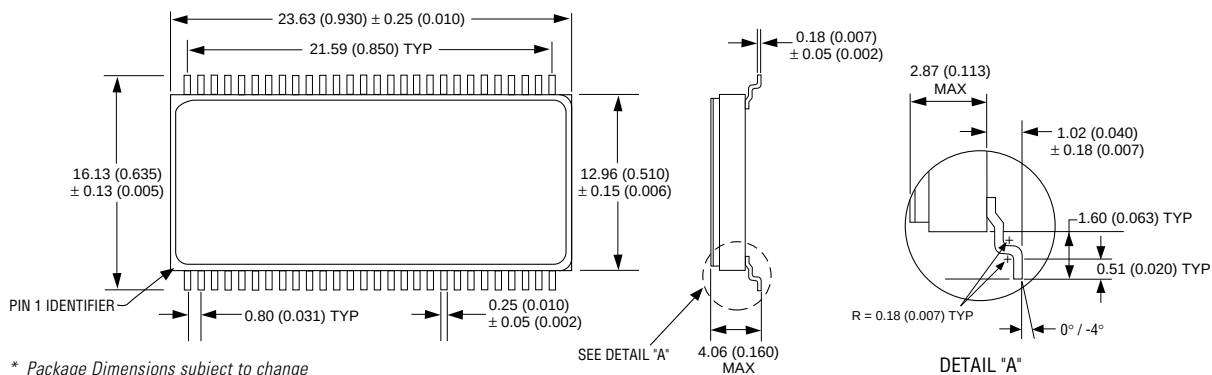


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.



PACKAGE 207: 56 LEAD, CERAMIC SOP*

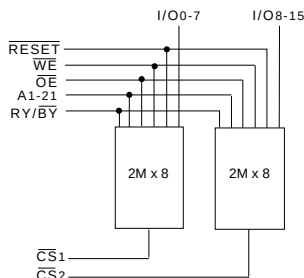


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 8 ALTERNATE PIN CONFIGURATION FOR WF2M16W-XDAX5

56 CSOP	
TOP VIEW	
CS1	1
A12	2
A13	3
A14	4
A15	5
NC	6
CS2	7
A21	8
A20	9
A19	10
A18	11
A17	12
A16	13
Vcc	14
GND	15
I/O6	16
I/O14	17
I/O7	18
I/O15	19
RY/BY	20
OE	21
WE	22
NC	23
I/O13	24
I/O5	25
I/O12	26
I/O4	27
Vcc	28
NC	29
RESET	30
A11	31
A10	32
A9	33
A1	34
A2	35
A3	36
A4	37
A5	38
A6	39
A7	40
GND	41
A8	42
Vcc	43
I/O9	44
I/O1	45
I/O8	46
I/O0	47
NC	48
NC	49
NC	50
NC	51
NC	52
NC	53
NC	54
NC	55
NC	56

BLOCK DIAGRAM



NOTE:

1. RY/BY is an open drain output and should be pulled up to Vcc with an external resistor.
2. Address compatible with Intel 1M16 56 SSOP.

PIN DESCRIPTION

I/O0-15	Data Inputs/Outputs
A1-21	Address Inputs
WE	Write Enable
CS1-2	Chip Select
OE	Output Enable
Vcc	Power Supply
Vss	Ground
RY/BY	Ready/Busy
RESET	Reset



ORDERING INFORMATION

W F 2M16 X - XXX X X 5 X

LEAD FINISH:

Blank = Gold plated leads
A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE

5 = 5V

DEVICE GRADE:

M = Military, 883 Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

DA = 56 Lead CSOP (Package 207)
fits standard 56 SSOP footprint
DL = 44 Lead Ceramic SOJ (Package 102)*
FL = 44 Lead Ceramic Flatpack (Package 208)*

ACCESS TIME (ns)

IMPROVEMENT MARK:

• *Address Pinout for 56 CSOP Package*
W = Word Wide Applications

ORGANIZATION of 2M x 16

User configurable as 2 x 2M x 8

Flash

WHITE ELECTRONIC DESIGNS CORP.

* Package to be developed.

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 16 5V Flash Module	64KByte	150ns	56 lead CSOP (DA)	5962-97610 01HXX
2M x 16 5V Flash Module	64KByte	120ns	56 lead CSOP (DA)	5962-97610 02HXX
2M x 16 5V Flash Module	64KByte	90ns	56 lead CSOP (DA)	5962-97610 03HXX